EC8691 MICROPROCESSORS AND MICROCONTROLLERS L T P C
3 0 0 3

OBJECTIVES:

- To understand the Architecture of 8086 microprocessor.
- To learn the design aspects of I/O and Memory Interfacing circuits.
- To interface microprocessors with supporting chips.
- To study the Architecture of 8051 microcontroller.
- To design a microcontroller based system

UNIT I THE 8086 MICROPROCESSOR 9

Introduction to 8086 – Microprocessor architecture – Addressing modes - Instruction set and assembler directives – Assembly language programming – Modular Programming - Linking and Relocation - Stacks - Procedures – Macros – Interrupts and interrupt service routines – Byte and String Manipulation.

UNIT II 8086 SYSTEM BUS STRUCTURE 9

8086 signals – Basic configurations – System bus timing –System design using 8086 – I/O programming – Introduction to Multiprogramming – System Bus Structure – Multiprocessor configurations – Coprocessor, Closely coupled and loosely Coupled configurations – Introduction to advanced processors.

UNIT III I/O INTERFACING 9

Memory Interfacing and I/O interfacing - Parallel communication interface – Serial communication interface – D/A and A/D Interface - Timer – Keyboard /display controller – Interrupt controller – DMA controller – Programming and applications Case studies: Traffic Light control, LED display , LCD display, Keyboard display interface and Alarm Controller.

UNIT IV MICROCONTROLLER 9

Architecture of 8051 – Special Function Registers(SFRs) - I/O Pins Ports and Circuits - Instruction set - Addressing modes - Assembly language programming.

UNIT V INTERFACING MICROCONTROLLER 9

Programming 8051 Timers - Serial Port Programming - Interrupts Programming – LCD & Keyboard Interfacing - ADC, DAC & Sensor Interfacing - External Memory Interface- Stepper Motor and Waveform generation - Comparison of Microprocessor, Microcontroller, PIC and ARM processors

TOTAL: 45 PERIODS OUTCOMES:

At the end of the course, the students should be able to:

- Understand and execute programs based on 8086 microprocessor.
- Design Memory Interfacing circuits.
- Design and interface I/O circuits.
- Design and implement 8051 microcontroller based systems.

TEXT BOOKS:

1. Yu-Cheng Liu, Glenn A.Gibson, ―Microcomputer Systems: The 8086 / 8088 Family - Architecture, Programming and Design‖, Second Edition, Prentice Hall of India, 2007. (UNIT I- III)
2. Mohamed Ali Mazidi, Janice Gillispie Mazidi, Rolin McKinlay, ―The 8051 Microcontroller and Embedded Systems: Using Assembly and C‖, Second Edition, Pearson education, 2011. (UNIT IV,V)

Subject Code: EC8691 **Year/Semester: III /05**
Subject Name: MICROPROCESSORS AND MICROCONTROLLERS **Subject Handler: A.PARIMALA**

Unit 1 THE 8086 MICROPROCESSOR	
Introduction to 8086 – Microprocessor architecture – Addressing modes - Instruction set and assembler directives – Assembly language programming – Modular Programming - Linking and Relocation - Stacks - Procedures – Macros – Interrupts and interrupt service routines – Byte and String Manipulation.	
Q. No.	**Questions & Answers**
1	**What are the types of instruction sets of 8086 microprocessor? BTL 1** There are eight types of instructions. They are • Data copy/Transfer instructions • Arithmetic & Logical instructions • Branch instructions • Loop instructions • Machine control instructions • Flag manipulation instructions • Shift & rotate instructions String instructions
2	**What are flag manipulation instructions? BTL 1** The instructions that directly modify the flags of 8086 are called as the flag manipulation instructions. E.g.: CLC --- clear carry flag, CMC --- complement carry flag, STC --- set carry flag , CLD --- clear direction flag
3	**Explain the instructions LODS & STOS. BTL 2** a)LODS: Load String Byte or String Word • The LODS instruction loads the AL/AX register by the content of a string pointed to by DS: SI registers pair. • The SI is modified automatically depending on direction flag. If it is a byte transfer (LODSB), the SI is modified by one & if it is a word transfer (LODSW), the SI is modified by two. • No other flags are affected by this instruction. b)STOS: Store String Byte or String Word • The STOS instruction stores the AL/AX register contents to a location in the string pointed by ES: DI register pair. • The DI is modified accordingly. • No flags are modified by this instruction.
4	**Define control transfer instruction & explain their types. BTL 1** The instructions that transfer the flow of execution of the program to a new address specified in the instruction directly or indirectly are called the control transfer or branching instructions. They are of two types. **Unconditional control transfer instructions**: In these types of instructions, the execution control is transferred to the specified location independent of any status or condition. **Conditional control transfer instructions**: In these instructions, The control is transferred to the specified location provided the result of the previous operation satisfies a particular condition, otherwise, the execution continues in normal flow sequence.
5	**What are assembler directives? Give example. BTL 1**

	The assembler is a program used to convert an assembly language program into the equivalent machine code modules that may be further converted to executable codes. Therefore the hints given to the assembler to complete all these tasks in some predefined alphabetical strings is called an assembler directive. E.g.: DB------define byte, END----end of program, EQU----- equate
6	**What is the function of parity flag? (Nov 2013) BTL 1** The parity flag is set, if the result of the byte operation or lower byte of the word operation contains an even number of ones.
7	**Define a MACRO. BTL 1** A number of instructions appearing again & again in the main program can be assigned as a macro definition (i.e.) a label is assigned to the repeatedly appearing string of instructions. The process of assigning a label or macro name to the string is called defining a macro. A macro within a macro is called a nested macro.
8	**Which interrupt has got the highest priority among all the external interrupts? BTL 1** The Non-Maskable Interrupt pin of 8086 has got the highest priority among the external Interrupts.
9	**What are the segment registers present in 8086? BTL 1** There are four segment registers in 8086.They are i. Code Segment register (CS) ii. Data Segment register (DS) iii. Extra Segment register (ES) iv. Stack Segment register (SS)
10	**What do you mean by instruction pipelining? BTL 1** While the execution unit executes the previously decoded instruction, the Bus Interface Unit fetches the next instruction and places it in the pre fetched instruction byte queue. This forms a pipeline.
11	**What is the use of the Trap flag in the flag register of 8086? BTL 1** When the Trap flag is set, the processor enters the single step execution mode. A trap interrupt is generated after execution of each instruction. The processor executes the current instruction and the control is transferred to the Trap interrupt service routine.
12	**List the instruction formats in 8086 instruction set. BTL 1** There are six general formats of instruction in 8086.They are • One byte instruction. • Register to Register. • Register to/from Memory with no Displacement. • Register to/from memory with Displacement. • Immediate operand to Register. • Immediate operand to Memory with 16-bit Displacement.
13	**List the various addressing modes of 8086?(May 2018)What are the addressing modes of sequence control transfer instructions in 8086? Give example. BTL 1** • Immediate eg: Mov AX,0005H. • Direct eg:Mov AX,[5000H]. • Register eg:Mov BX,AX. • Register Indirect eg:Mov AX,[Bx]. • Indexed eg:Mov AX,[SI].

- Register Relative eg:Mov AX,50H[BX].
- Based Indexed eg:Mov AX,[Bx] [SI].
- Relative Based Indexed eg: Mov AX,50H [BX] [SI].

14 **What are the differences between 8085 and 8086? (Nov 2013)** BTL1

8-bit microprocessor	16-bit microprocessor
It is capable of addressing 28 memory locations	It is capable of addressing 2^{16} memory locations
Low speed	High speed
It can be configured only in single processor mode	It can be configured in single processor mode and multiprocessor mode

15 **How is the physical address generated in 8086? (or) How 16 bit address is converted into 20 bit address in 8086? (Nov 2013) (Apr/May 2017) BTL 1**

The content of the segment register called as segment address is shifted Left bit-wise four times and to this result, content of an offset register also called as offset address is added, to produce a 20-bit physical address.

eg:
segment address 1005H
Offset address 5555H
Segment address 0001 0000 0000 0101
Shifted by 4 bit positions 0001 0000 0000 0101 0000
+
Offset address 0101 0101 0101 0101
Physical address 0001 0101 0101 1010 0101
1 5 5 A 5

16 **Explain XLAT instruction. BTL 2**

- The XLAT (Translate) instruction replaces a byte in the AL register with a byte from a 256-byte, user coded translation table.
- XLAT is useful for translating characters from one code to another like ASCII to EBCDIC and ASCII to HEX etc.

17 **Draw the PSW format for 8086.(May/June 2016) BTL 2**

B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
U	U	U	U	OF	DF	IF	TF	SF	ZF	U	AF	U	PF	U	CF

U: Undefined; CF : Carry flag - Set by carry out of MSB
PF: Parity flag- set if result has even parity; AF : Auxiliary carry flag - used for BCD operation; ZF : Zero flag - set if result = 0; SF : Sign flag - set if result is –ve.
TF : Trap flag - set to enable single step execution mode. IF: Interrupt flag- set to enable interrupt ;DF : Direction flag - set to enable auto decrement mode for string operation ;OF: Overflow flag - used for signed arithmetic operation

18 **Explain the function of TEST pin in 8086 BTL 2**

This input is examined by a "WAIT" instruction. When the processor executes WAIT instruction, it enters into wait state (Idle state). If the TEST pin goes low, the processor will come out from the idle state and continues the execution; otherwise it remains in an idle state.

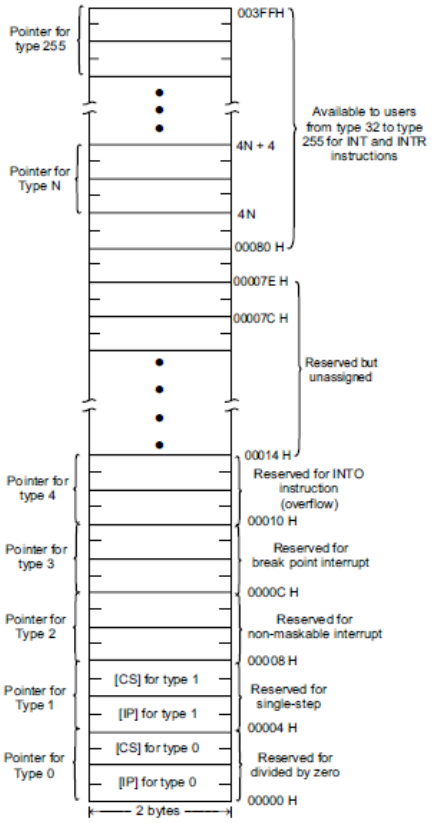
19 **Give the operation of CBW and TEST instructions of 8086? (Nov 2013) BTL 1**

CBW instruction converts the byte in AL to word value in AX by extending the sign of AL throughout the register AH. TEST instruction performs logical AND operation of the two operands updating the flag registers without saving the result

20 **What do you mean by addressing modes? (May 2014) BTL 1**

	The addressing modes clearly specify the location of the operand and also how its location may be determined.
21	**What is meant by a vectored interrupt? (May 2014) BTL 1** There is an interrupt vector table which stores the information regarding the location of interrupt service routine (ISR) of various interrupt. Whenever an interrupt occurs the memory location of ISR is determined using the vector table and the program control branches to ISR after saving the flags and the program location.
22	**Write about the different types of interrupts supported in 8086. . (May 2015) BTL1** Interrupts in 8086 are classified into three. They are: i) Pre defined interrupt - Type 0 to Type 4 interrupts. ii) Hardware interrupt - Mask able interrupt and Non Mask able interrupt iii) Software interrupt(INT n) - 256 types of software interrupt.
23	**Define Stack. (May/June 2016) (Apr/May 2017) BTL 1** A **stack** pointer is a small register that stores the address of the last program request in a **stack**. A **stack** is a specialized buffer which stores data from the top down. As new requests come in, they "push down" the older ones.
24	**What are Macros .MAY 2018,APRIL/ MAY 2019 BTL 1** When procedure is called within the main program by an assembler, the program control will be transferred to the procedures starting address and starts execution of a group of instructions available in the procedure. In macros, whenever macro is called by its name, each time the assembler will insert the defined group of instructions in the main program itself i.e., program control is not transferred anywhere.
25	**Given that (BX=0158. (D I)=10A5 Displacement =1B57 (DS)=2100 .Determine the effective address and physical address for the following addressing modes. (a) Register In direct (b).Relative based indexed. April/may 2019 BTL 1** segment address 1005H Offset address 5555H Segment address 0001 0000 0000 0101 Shifted by 4 bit positions 0001 0000 0000 0101 0000 + Offset address 0101 0101 0101 0101 Physical address 0001 0101 0101 1010 0101 1 5 5 A 5
26	**What is the need for interrupts in microprocessor operations?(DECEMBER 2018) BTL 1** • To perform subtask and subprogram • To increase system speed • During execution of certain task with the program has to transfer to other program operation. • To halt the processor

27	**What are Byte and string manipulation? (DECEMBER 2018) BTL 1** In byte manipulation , the arithmetic and logical operations are performed on byte data . Eg: AND & OR operation. When same arithmetic or logical operation is performed on multiple bytes one by one ,the operation is called string manipulation. Eg: MOVSB ,STOSB
	PART B/ UNIT I
1	**Discuss in detail the three types of interrupt system of Intel 8086. (May 2014) (Apr/May 2016, 2017) (13M) APRIL/ MAY 2019 BTL 6** **Ans: Refer** Yu-Cheng Liu, Glenn A.Gibson, "Microcomputer systems: The 8086 / 8088 Family -Architecture, Programming and Design", Second Edition, Prentice Hall of India, 2007.**PG.NO:169-173** • 8086 can implement seven different types of interrupts. • NMI and INTR are external interrupts implemented via *Hardware*. • INT n, INTO and INT3 (breakpoint instruction) are software interrupts implemented through *Program.* • The 'divide-by-0' and 'Single-step' are interrupts *initiated by CPU.*

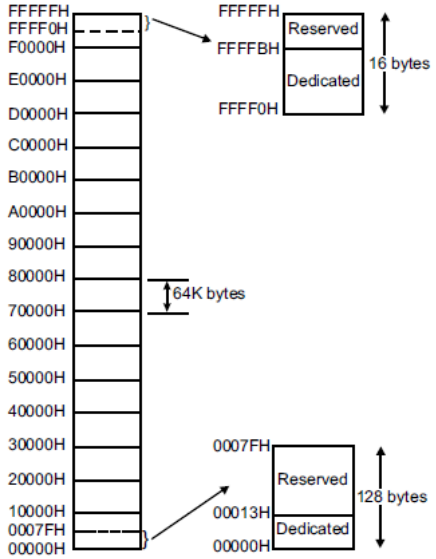


(13M)

2 **Explain the memory concepts of Intel 8086 and explain how data transfer takes place. (13M) BTL 5**

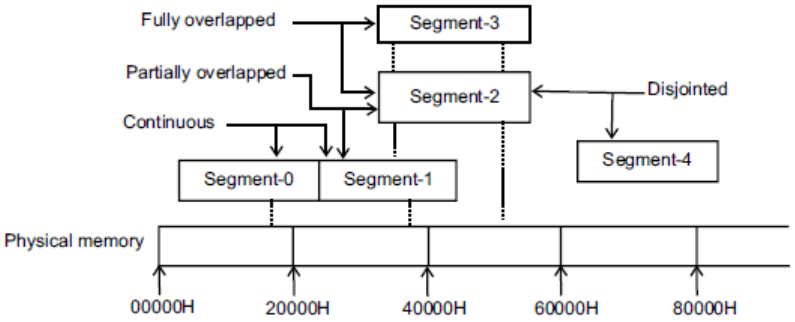
Ans: Refer Yu-Cheng Liu, Glenn A.Gibson, "Microcomputer systems: The 8086 / 8088 Family -Architecture, Programming and Design", Second Edition, Prentice Hall of India, 2007.**PG.NO:26-35**

8086, via its 20-bit address bus, can address 220 = 1,048,576 or 1 MB of different memory locations. Thus the memory space of 8086 can be thought of as consisting of 1,048,576 bytes or 524,288 words. The memory map of 8086 is shown in Figure, where the whole memory space starting from 00000 H to FFFFF H is divided into 16 blocks—each one consisting of 64 KB. This division is arbitrary but at the same time a convenient one—because the most significant hex digit increases by 1 with each additional block. Thus, 30000 H memory location is 65,536 bytes higher in memory than the memory location 20000 H. (3M)



(2M)

The lower and upper ends of the memory map are shown separately—earmarking some spaces

	as reserved and some as 'dedicated'. The reserved locations are meant for future hardware and software needs while the dedicated locations are used for processing of specific system interrupts and reset functions. (2M) The different memory segmentations done in case of 8086 are • Continuous • partially overlapped • fully overlapped and • disjointed This is shown in Fig.12.2.  **Fig. 12.2:** Depiction of different types of segments In the figure, Segments-0 and 1 ⟶ Continuous Segments-1 and 2 ⟶ Partially overlapped Segments-2 and 3 ⟶ Fully overlapped and Segments-2 and 4 ⟶ Disjointed (4M) The 20-bit physical (real) address is generated by combining the offset (residing in IP, BP, SP, BX, SI or DI) and the content of one of the segment registers CS, DS, ES or SS. The process of combination is as follows: The content of the segment register is internally appended with 0 H (0000 H) on its right most end to form a 20-bit memory address—this 20-bit address points to the start of the segment. The offset is then added to the above to get the physical address. (2M)
3	**Describe the addressing modes 8086 with examples from instruction set of 8086. (Apr/May 2016)(November/December 2018) (13M) BTL 6** **Ans: Refer** Yu-Cheng Liu, Glenn A.Gibson, "Microcomputer systems: The 8086 / 8088 Family -Architecture, Programming and Design", Second Edition, Prentice Hall of India, 2007.**PG.NO:35-39** • Register operand addressing. (1M) • Immediate operand addressing. (1M) • Memory operand addressing. (1M) • Direct Addressing (1M) • Register Indirect Addressing (1M) • Based Addressing (2M) • Indexed Addressing (2M) • Based Indexed Addressing and (2M) • Based Indexed with displacement. (2M)
4	**What is a 'REP' instruction? Discuss. (3M)** **Write an 8086 ALP to find the sum of numbers in an array of 10 elements.(7M) (Apr/May 2016) BTL 3** **Ans: Refer Notes**

'REP' stands for repeat and is used for repeating basic string operations—required for processing arrays of data.

There are a number of repeat instructions available and are used as a prefix in string instructions. The prefixes for use with the basic string instructions are shown in Fig. 14.19.

Prefix	Used with	Meaning
REP	MOVS STOS	Repeat while not end of string CX ≠ 0
REPE/REPZ	CMPS SCAS	Repeat while not end of string and strings are equal CX ≠ 0 and ZF = 1
REPNE/REPNZ	CMPS SCAS	Repeat while not end of string and strings are not equal CX ≠ 0 and ZF = 0

(3M)

```
DATA SEGMENT
ARR DB 5,3,7,1,9,2,6,8,4,10
LEN DW $-ARR
SUM DW ?
DATA ENDS
CODE SEGMENT
ASSUME DS:DATA CS:CODE
START:
MOV AX,DATA
MOV DS,AX
LEA SI,ARR
MOV AX,0
MOV CX,LEN
REPEAT:
MOV BL,ARR[SI]
MOV BH,0
ADD AX,BX
INC SI
LOOP REPEAT
MOV SUM,AX
MOV AH,4CH
INT 21H
CODE ENDS
END START
```

(7)

5	**List the basic string instructions and the operations they perform. (3M) BTL 3** **Write an 8086 ALP for Multiplication of two 8-bit numbers. BTL 3** **Ans: Refer Notes**

Mnemonic	Meaning	Format	Operation
LOOP	Loop	LOOP Short-label	(CX)←(CX) – 1 Jump is initiated to location defined by short-label if (CX) ≠ 0; otherwise, execute next sequential instruction.
LOOPE/LOOPZ	Loop while equal/loop while zero	LOOPE/LOOPZ Short-label	(CX)←(CX) – 1 Jump to the location by short-label if (CX) ≠ 0 and (ZF) = 1; otherwise execute next sequential instruction.
LOOPNE/ LOOPNZ	Loop while not equal/ loop while not zero	LOOPNE/LOOPNZ Short-label	(CX)←(CX) – 1 Jump to the location defined by short label if (CX) ≠ 0 and (ZF) = 0; otherwise execute next sequential instruction

(3M)

```
DATA SEGMENT
VAR1 DB 0EDH
VAR2 DB 99H
RES DW?
DATA ENDS
ASSUME CS: CODE, DS:DATA
CODE SEGMENT
START: MOV AX, DATA
MOV DS, AX
MOV AL, VAR1
MOV BL, VAR2
MUL BL
MOV RES, AX
MOV AH, 4CH
INT 21H
CODE ENDS
END START
```

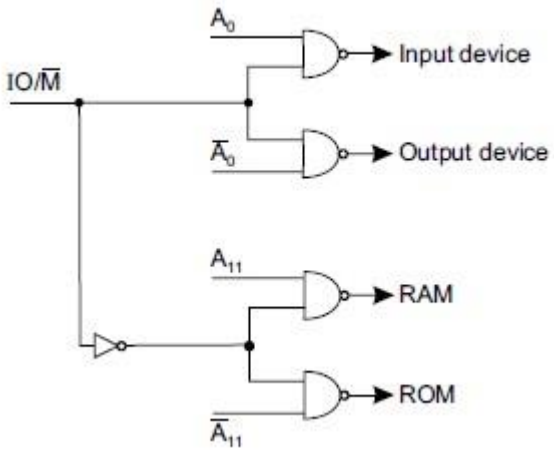
(7M)

6 **Explain the different instruction used for input and output operation in I/O mapped I/O mode of 8086. (13M) BTL 5**

Ans: Refer. Doughlas V.Hall, "Microprocessors and Interfacing, Programming and Hardware:,TMH, 2012 **PG.NO:B**3 &B5

- In this scheme, there is only one address space. This address space is allocated to both memory and I/O devices. Some addresses are assigned to memories and some to I/O devices.
- The address for I/O devices is different from the addresses which have been assigned to memories. An I/O device is also treated as a memory location. In this scheme one address is assigned to each memory location and one address is assigned to each I/O device.
- In this scheme, all data transfer instructions of the microprocessor can be used for transferring data from and to either memory or I/O devices.
- For example, MOV D,M instruction would transfer one byte of data from a memory location or an input device to the register D, depending on whether the address in the H-L register pair is assigned to a memory location or to an input device.
- If H-L contains address of a memory location, data will be transferred from that memory location to register D, while if H-L pair contains the address of an input device, data will be transferred from that input device to register D.
- This scheme is suitable for small systems. In this scheme, IO/ M signal is not used to distinguish between memory and I/O devices. An I/O device is interfaced in the same

manner as a memory device. (10M)



(3M)

9 **i) Write an 8086 ALP to sort out any given ten numbers in ascending and descending order. (Nov 2013) (10M) Ans: Refer Notes**

ii) Give the functions of NMI, BHE and TEST pins of 8086. (3) (Nov 2013) BTL 3

Ans: Refer Yu-Cheng Liu, Glenn A.Gibson, "Microcomputer systems: The 8086 / 8088 Family -Architecture, Programming and Design", Second Edition, Prentice Hall of India, 2007.**PG.NO:26**

Ascending Order

```
DATA SEGMENT
STRING1 DB
99H,12H,56H,45H,36H
DATA ENDS
 CODE SEGMENT
ASSUME CS:CODE,DS:DATA
START: MOV AX,DATA
MOV DS,AX
 MOV CH,04H
 UP2: MOV CL,04H
LEA SI,STRING1
 UP1: MOV AL,[SI]
MOV BL,[SI+1]
CMP AL,BL
JC DOWN
MOV DL,[SI+1]
XCHG [SI],DL
MOV [SI+1],DL
 DOWN: INC SI
DEC CL
JNZ UP1
DEC CH
JNZ UP2
 INT 3
CODE ENDS
END START
```

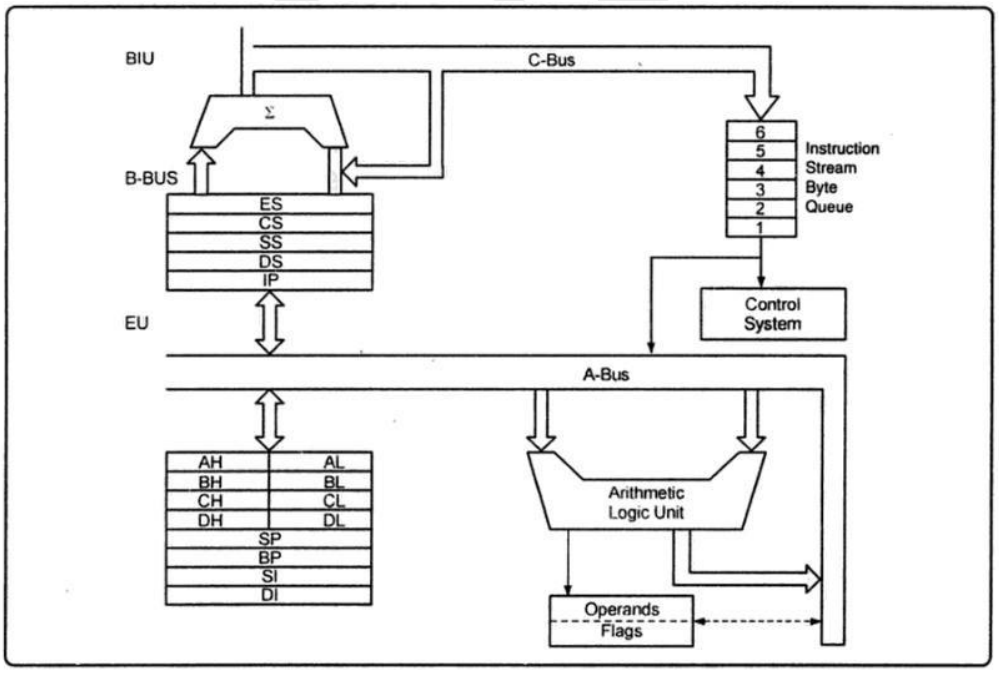
```
DATA SEGMENT
STRING1 DB
99H,12H,56H,45H,36H
DATA ENDS
CODE SEGMENT
ASSUME
CS:CODE,DS:DATA
START: MOV AX,DATA
MOV DS,AX
MOV CH,04H
UP2: MOV CL,04H
LEA SI,STRING1
 UP1:MOV AL,[SI]
MOV BL,[SI+1]
CMP AL,BL
JNC DOWN
MOV DL,[SI+1]
XCHG [SI],DL
MOV [SI+1],DL
 DOWN: INC SI
DEC CL
JNZ UP1
DEC CH
JNZ UP2
INT 3
CODE ENDS
END START
```

(10M)

Non Maskable Interrupt

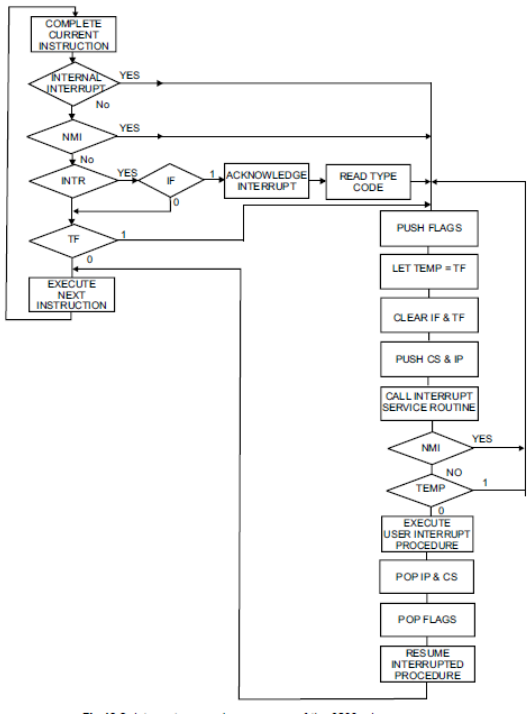
Interrupt cannot be disabled by any software instruction. This interrupt is activated by low to high transition on 8086 NMI input pin. (1M)

BHE : The bus high enable is used to indicate the transfer of data over the higher order (D15-D8) data bus. It goes low for the data transfer over D15-D8 and is used to derive chip selects of odd address memory bank or peripherals. (1M)

	TEST : This input is examined by a 'WAIT' instruction. If the TEST pin goes low, execution will continue, else the processor remains in an idle state. The input is synchronized internally during each clock cycle on leading edge of clock. (1M)
10	**i) Explain briefly about internal hardware architecture of 8086 microprocessor with a neat diagram.(10M) ii) Write a 8086 assembly language program to convert BCD data - Binary data.(3M) (May 2015) (Apr/May 2017). APRIL/MAY 2019,NOV /DEC 2019. BTL 5** **Ans: Refer** Yu-Cheng Liu, Glenn A.Gibson, "Microcomputer systems: The 8086 / 8088 Family -Architecture, Programming and Design", Second Edition, Prentice Hall of India, 2007.**PG.NO:26-33** • It is a 16-bit Microprocessor (μp).It's ALU, internal registers works with 16bit binary word. • 8086 has a 20 bit address bus can access up to 220= 1 MB memory locations. • 8086 has a 16bit data bus. It can read or write data to a memory/port either 16bits or 8 bit at a time. • It can support up to 64K I/O ports. • It provides 14, 16 -bit registers. • Frequency range of 8086 is 6-10 MHz • It has multiplexed address and data bus AD0- AD15 and A16 – A19. • It requires single phase clock with 33% duty cycle to provide internal timing. • It can prefetch upto 6 instruction bytes from memory and queues them in order to speed up instruction execution. • It requires +5V power supply. • A 40 pin dual in line package. • 8086 is designed to operate in two modes, Minimum mode and Maximum mode. • The minimum mode is selected by applying logic 1 to the MN / MX# input pin. This is a single microprocessor configuration. • The maximum mode is selected by applying logic 0 to the MN / MX# input pin. This is a multi micro processors configuration.  (10M) DATA SEGMENT BCD DW 27H BIN DW ? DATA ENDS CODE SEGMENT

	ASSUME CS:CODE,DS:DATA
	START: MOV AX,DATA
	MOV DS,AX
	MOV AX,BCD
	AND AX,07H
	MOV BX,AX
	MOV AX,BCD
	AND AX,0F0H
	MOV CX,0AH
	MUL CX
	ADD AX,BX
	MOV BIN,AX
	MOV AH,4CH
	INT 21H
	CODE ENDS
	END START (3M)

11	**i) Explain about ASSUME, EQU, DD assembler directives.(6)** **ii) Explain briefly about interrupt handling process in 8086.(7) (May 2015) BTL 5** **Ans: Refer**. Doughlas V.Hall, "Microprocessors and Interfacing, Programming and Hardware:,TMH, 2012 **PG.NO:6.31-6.32** **ASSUME : assume logical segment name** It is used to assign the names of the logical segments used in the program. ***Syntax : ASSUME segment register : name*** Eg) ASSUME CS : CODE ASSUME DS : DATA (2M) **DD : Define Double Word** It is used to reserve four bytes ***Syntax : Name of the variable DD Initial values*** Eg) number DD 12345678 (2M) **EQU : Equate** It is used to assign a label with a value or a symbol. The use of this directive is to reduce the recurrence of the numerical values or constants in a program. ***Syntax : name EQU expression/text*** Eg) label EQU 0500H Addition EQU ADD (2M) When an interrupt occurs (hardware or software), the following things happen: The contents of flags register, CS and IP are pushed on to the stack.TF and IF are cleared which disable single step and INTR interrupts respectively. Program jumps to the starting address of ISS. At the end of ISS, when IRET is executed in the last line, the contents of flag register, CS and IP are popped out of the stack and placed in the respective registers. When the flags are restored, IF and TF get back their previous values.



(7M)

12 **What is Interrupt and Interrupt routine. Explain interrupt sequence for 8086 Microprocessor and interrupt pointers? (13M)April/May 2019 BTL 2**

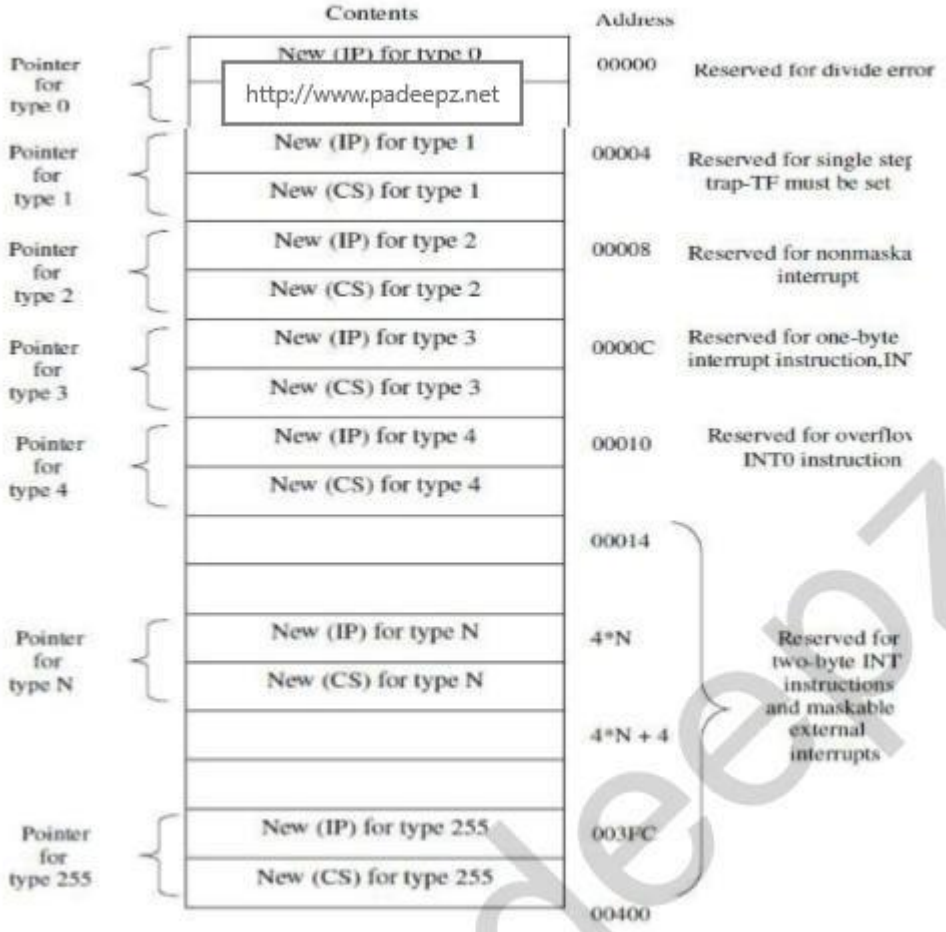


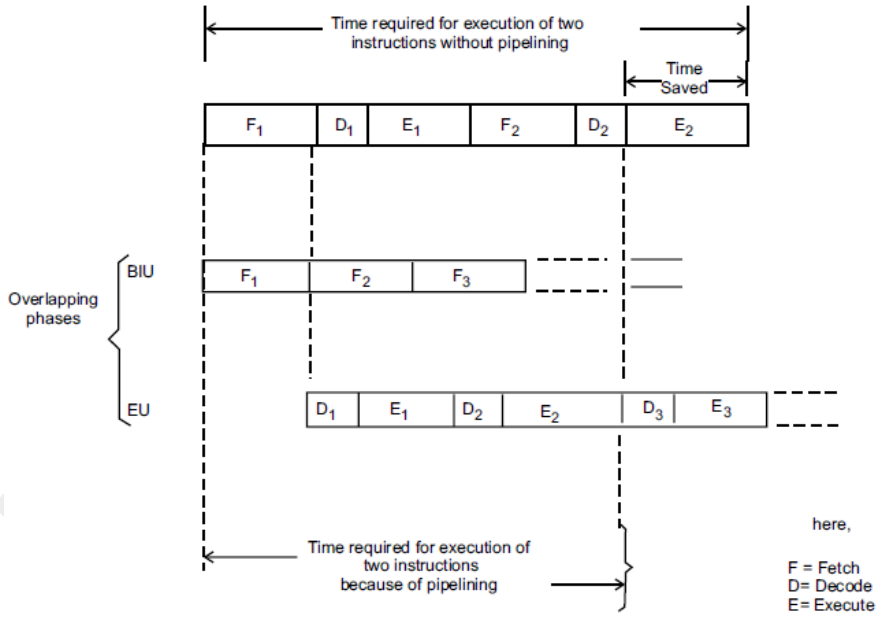
Fig. 1.12 Organization of Interrupt vector table in 8086

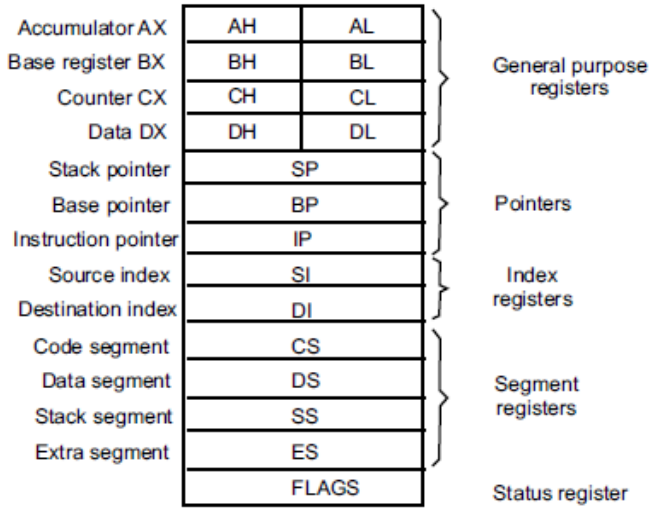
Only the first five types have explicit definitions; the other types may be used by interrupt instructions or external interrupts. From the figure it is seen that the type associated with a division error interrupt is 0. Therefore, if a division by 0 is attempted, the processor will push the current contents of CS and IP into the stack, fill the IP and CS registers from the addresses 00000 to 00003, and continue executing at the address indicated by the new contents of IP and CS.

A division error interrupt occurs any time a DIV or IDIV instruction is executed with the quotient exceeding the range, regardless of the IF (Interrupt flag) and TF (Trap flag) status.

The type 1 interrupt is the single-step interrupt (Trap interrupt) and is the only interrupt controlled by the TF flag. If the TF flag is enabled, then an interrupt will occur at the end of the next instruction that will cause a branch to the location indicated by the contents of 00004H to 00007H.The single step interrupt is used primarily for debugging which gives the programmer a snapshot of his program after each instruction is executed

	PART * C
1	**Explain Complete arithmetic operation, (15M) BTL 5** **AAA: ASCII Adjust After Addition** The AAA instruction is executed after an ADD instruction that adds two ASCII coded operands to give a byte of result in AL. The AAA instruction converts the resulting contents of AL to unpacked decimal digits. After the addition, the AAA instruction examines the lower 4 bits of AL to check whether it contains a valid BCD number in the range 0 to 9. If it is between 0 to 9 and AF is zero, AAA sets the 4 high order bits of AL to 0. The AH must be cleared before addition. If the lower digit of AL is between 0 to 9 and AF is set, 06 is added to AL. The upper 4 bits of AL are cleared and

	AH is incremented by one. If the value in the lower nibble of AL is greater than 9 than the AL is incremented by 06, AH is incremented by 1, the AF and CF flags are set to 1, and the higher 4 bits of AL are cleared to 0. The remaining flags are unaffected. The AH is modified as sum of previous contents (usually 00) and the carry from the adjustment. This instruction does not gives exact ASCII codes of the sum, but they can be obtained by adding 3030H to AX. (3M) **AAS: ASCII Adjust AL After Subtraction** AAS instruction corrects the result in AL register after subtracting two unpacked ASCII operands. The result is in unpacked decimal format. If the lower 4 bits of AL register are greater than 9 or if the AF flag is 1, the AL is decremented by 6 and AH register is decremented by 1, the CF and AF are set to 1. Otherwise, the CF and AF are set to 0, the result needs no correction. As a result, the upper nibble of AL is 00 and the lower nibble may be any number from 0 to 9. The procedure is similar to the AAA instruction. AH is modified as difference of the previous contents (usually zero) of AH and the borrow for adjustment.
2	**Explain the operations of instructions queue residing in BIU (May 2017) (15M) BTL 6** • The instruction queue is 6-bytes in length, operates on FIFO basis, and receives the instruction codes from memory. • BIU fetches the instructions meant for the queue ahead of time from memory. • In case of JUMP and CALL instructions, the queue is dumped and newly formed from the new address.  (15M)
3	**Explain the Programmers model of 8086 (May 2018) (15M) BTL 5** • Data group, pointers and index group, status and control flag group and segment group. • The data group consists of AX (accumulator), BX (base), CX (count) and DX (data). • Pointer and Index group consist of SP (Stack pointer), BP (Base pointer), SI (Source Index), DI (Destination index) and IP (Instruction pointer). • Segment group consists of ES (Extra Segment), CS (Code Segment), DS (Data Segment) and SS (Stack Segment). • Control flag group consists of a single 16-bit flag register.

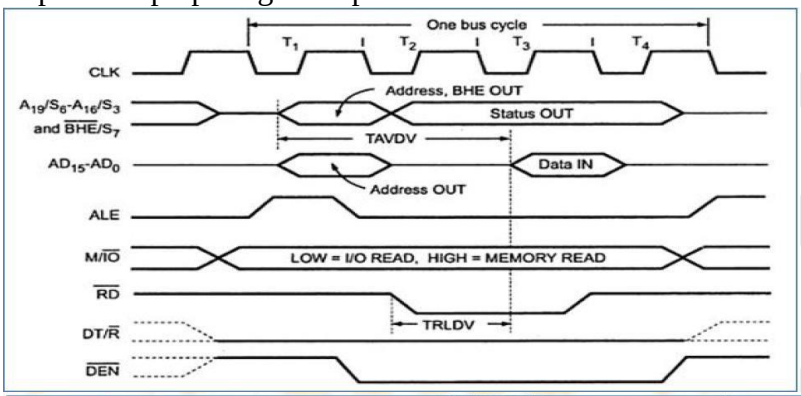
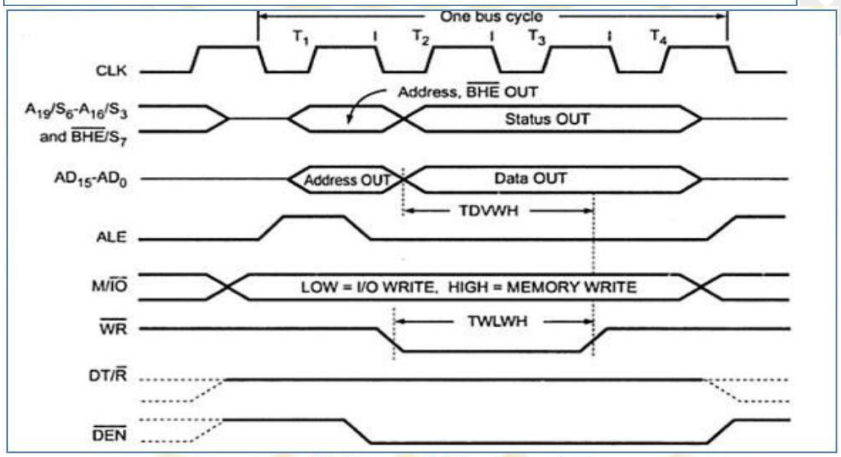


UNIT II

8086 signals – Basic configurations – System bus timing –System design using 8086 – I/O programming – Introduction to Multiprogramming – System Bus Structure – Multiprocessor configurations – Coprocessor, Closely coupled and loosely Coupled configurations – Introduction to advanced processors.	
Q. No.	**Questions & Answers**
1	**What is meant by multiprocessor system? BTL 1** If a microprocessor system contains two or more components that can execute instructions independently then the system is called as multiprocessor system.
2	**What is meant by multiprogramming? (Apr/May 2017) BTL 1** Multitasking has the same meaning of multiprogramming but in a more general sense, as it refers to having multiple (programs, processes, tasks, threads) running at the same time. This term is used in modern operating systems when multiple tasks share a common processing resource (e.g., CPU and Memory). Multiprogramming is a rudimentary form of parallel processing in which several programs are run at the same time on a uniprocessor. Since there is only one processor, there can be no true simultaneous execution of different programs.
3	**What is closely coupled configuration BTL 1** If the processor supporting processor, clock generator, bus control logic, memory and I/O System, communicate shared memory then it is called closely coupled system.
4	**What the advantages are of loosely coupled? BTL 1 APRIL/ MAY 2019 BTL 1** • Better system throughput by having more than one processor. • A greater degree of parallel processing can be achieved. • System structure is more flexible. • A failure in one module does not cause any breakdown of the system.
5	**What is meant by memory contention & hot spot contention? BTL 1** • A memory module can handle only one access request at a time. Hence when several processors request the same memory module it gives rise to memory contention. • When several processors repeatedly across the same memory location, it gives rise to hot spot contention.
6	**What is meant by bus arbitration? BTL 1** The mechanism which decides the selection of current master to access bus is known as bus arbitration.
7	**What are the advantages of Daisy Chaining? BTL 1** • It is simple and cheaper method • It requires the least number of lines and this number is independent of the number of masters in the system.
8	**What is meant by bus arbitration? BTL 1** The mechanism which decides the selection of current master to access bus ia called bus arbitration.
9	**What is meant by Numeric processor? BTL 1** The numeric processor 8087 is a coprocessor which has been specially designed to work under the control of the processor 8086 and to support additional numeric processing capabilities.
10	**On which data types can memory operands operate? BTL 1** 1. Word integer, 2.Short integer, 3.Long integer, 4.Packed BCD, 5.Short real, 6Long Real 7. Temporary real
11	**What is the use of TC STOP Mode? BTL 1** If the TC Stop bit is set the channel is disabled after the TC output goes high, thus automatically preventing further DMA Operation on that channel.
12	**What are advantages of coprocessor? (May 2014) BTL 1** The co-processors & supplementary processors which can fetch operands & execute it**.** It can

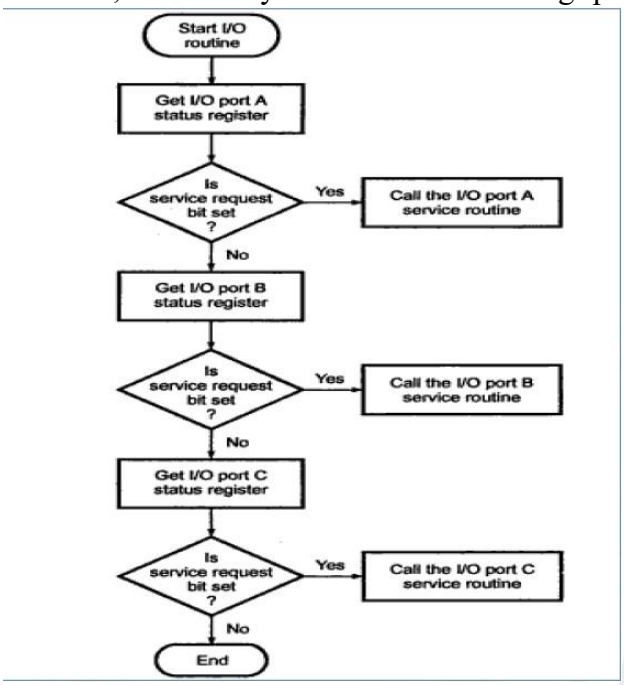
	read CPU status & queue status, make bus and interrupt request, receive reset & ready signals, receive bus grants, maintain an instruction queue decode the external op code.
13	**What is co-processor? (Nov 2013) BTL 1** The 8086/8088 must be supplemented with co-processors that extends the instruction set to allow the necessary special computations to be accomplished more efficiently. Eg: 8087 Numeric Data Processor.
14	**What is a Floating point Coprocessor? (Nov 2013) BTL 1** The floating point coprocessor uses real data types or floating point types of the following format: Real data $X=\pm 2^{exp} \times$mantissa, which may vary from extremely small to extremely large values.
15	**What is meant by loosely coupled configuration? (May 2014) (Apr/May 2016) BTL 1** In a loosely coupled multiprocessor system each CPU has its own bus control logic and bus arbitration is resolved by extending this logic and adding external logic that is common to all the modules.
16	**Differentiate external vs. internal bus. (Apr/May 2016) BTL 4** The internal data bus is the one responsible for transferring the data between the data registers and each other or between the data registers and the CPU. The external data bus transfers the data between the internal registers and the external memory or directly to the output.
17	**Define Bus. Why Bus request and cycle stealing are required? (May 2015) BTL 1** Bus is a group of parallel conductors which carries data, address and control signals from one unit to another unit. Bus request and Cycle stealing are required to access the RAM without interfering with the CPU. It is similar to DMA for allowing I/O controllers to read or write RAM without CPU intervention.
18	**Draw the read cycle timing diagram for minimum mode. (May 2015) BTL 2**
19	**Write some example for advanced processor. (Apr/May 2017) BTL 1** ARM Processor AMD Processor
20	**What is the function of BHE signal in 8086? BTL 1** BHE signal means Bus High Enable signal. The BHE signal is made low when there is some read or write operation is carried out. ie .When ever the data bus of the system is busy i.e. whenever there is some data transfer then the BHE signal is made low.
21	**State the significance of LOCK signal in 8086? BTL 1** If 8086 is working at maximum mode, there are multiprocessors are present. If the system bus is given to a processor then the LOCK signal is made low. That means the system bus is busy and it cannot be given of any other processors. After the use of the system bus again the LOCK signal is made high. That means it is ready to give the system bus to any processor.
22	**What are the functions of status pins in 8086? BTL 1** S2 S1 S0 0 0 0 ---- Interrupt acknowledge 0 0 1 ---- Read I/O

	0 1 0 ---- Write I/O 0 1 1 ---- Halt 1 0 0 -----Code access 1 0 1 ---- Read memory 1 1 0 ---- Write memory 1 1 1 -----inactive S4 S3 0 0 --I/O from extra segment 0 1 --I/O from Stack Segment 1 0 --I/O from Code segment 1 1 --I/O from Data segment S5 --Status of interrupt enable flag S6 --Hold acknowledge for system bus S7 --Address transfer
23	**Give the functions of coprocessor. BTL 1** Coprocessors cannot fetch instructions from memory, execute program flow control instructions, do input/output operations, manage memory, and so on. The coprocessor requires the host (main) processor to fetch the coprocessor instructions and handle all other operations aside from the coprocessor functions. In some architecture, the coprocessor is a more general-purpose computer, but carries out only a limited range of functions under the close control of a supervisory processor.
24	**What is the need for multi processor system? BTL 1** Due to the limited data width and lack of floating point arithmetic instructions, 8086 requires many instructions for computing even single floating point operation. For this NDP (8087) is used.Some processor like DMA controllers can help 8086 with low level operations while the CPU can take care of high level operations.
25	**What is Multiprocessing? NOV/DEC 2018 BTL 1** Multiprocessing is the use of two or more central processing units (CPUs) within a single computer system. The term also refers to the ability of a system to support more than one processor and/or the ability to allocate tasks between them.
30	**Define system bus timing. BTL 1** Timing diagram of 8086 bus cycles includes general bus operation, memory & I/O read cycle and memory & I/O write cycle in minimum mode operation. memory & I/O read cycle and memory & I/O write cycle in maximum mode operation. Interrupt acknowledgement, bus request, bus grant timing in minimum and maximum mode operation.
31	**Draw the format of the Flag register. APRIL/ MAY 2019 BTL 1**

32	**When is coprocessor used? NOV 2018 BTL 1** Coprocessor are deployed whenever several I/O operations to be serviced (8089) and to handle floating point operations (8087).
	Part B/Unit II
1.	**Explain system bus timings in 8086. (13M) (Apr/May 2016) (Apr/May 2017) BTL 5** **Ans: Refer** Yu-Cheng Liu, Glenn A.Gibson, "Microcomputer systems: The 8086 / 8088 Family –Architecture, Programming and Design", Second Edition, Prentice Hall of India, 2007.**PG.NO:324-329** When processor is ready to initiate the bus cycle, BHE, M/IO, DEN and DT/R must be stable i.e. DEN = high and DT/R = 0 for input or DT/R = 1 for output. 2. At the trailing edge of ALE, ICs 74LS373 or 8282 latches the address. 3. During T2 the address signals are disabled and S3-S7 are available on AD16/S3-AD19/S6 and BHE/S7. In case of Input operation, is activated during T2 and AD0 to AD15 go in high impedance preparing for input.   **(b) Output (Write Operation)** (13M)
2.	**Explain in detail about IO programming. (May 2014) BTL 2** **Input port:** • It is used to read data from the input device such as keyboard. The simplest form of input port is a buffer. The input device is connected to the microprocessor through buffer. This buffer is a tri-state buffer and its output is available only Enable when enable signal is active. When microprocessor wants to read data from the input device (keyboard), the control signals from the microprocessor activates the buffer by asserting enable Input of the buffer, once the buffer is enabled, data train the Input device is available on the data bus. Microprocessor reeds this data by Initiating reed command. **Output port:** • It is used to send data to the output device such as display from the microprocessor. The simplest form of output port is a latch. The output device is connected *to* the microprocessor through latch. When microprocessor wants to send data to the output device, it puts the data on the data bus and activates the clock signal of the latch.

Programmed I/O:

• I/O operations will mean a data transfer between an I/O device and memory or between an I/O device and the CPU. If any computer system I/O operations are completely controlled by the CPU, then that system is said to be using 'programmed I/O'.



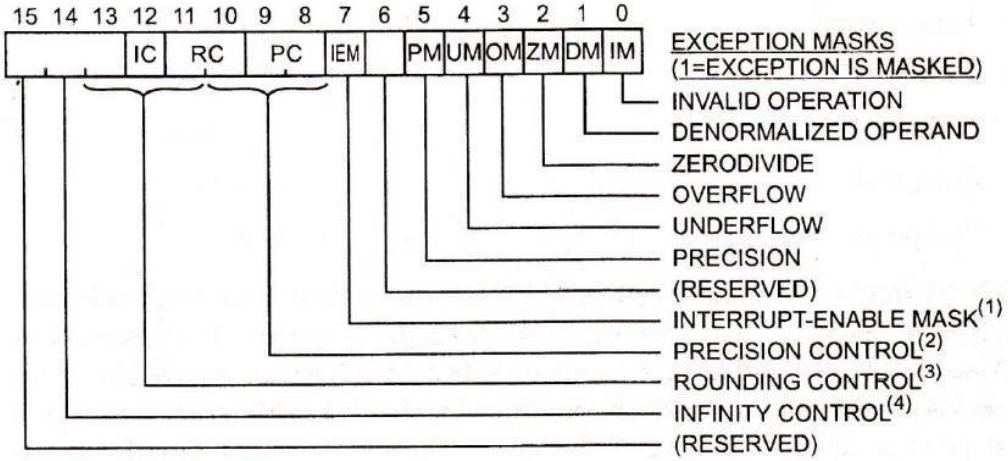
(13M)

3. **Explain the execution steps of 8087 coprocessor. (8) (May 2014) (Apr/May 2016) BTL 4**

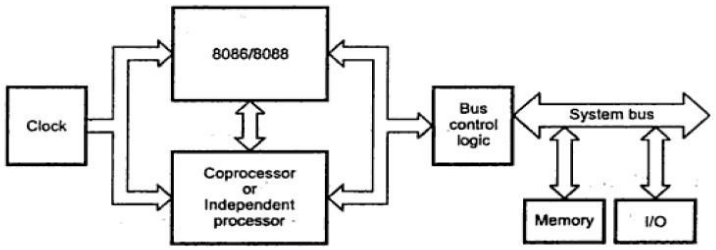
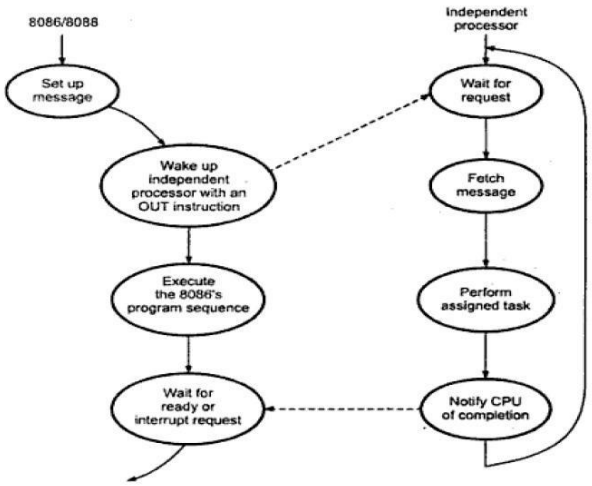
Ans: Refer Yu-Cheng Liu, Glenn A.Gibson, "Microcomputer systems: The 8086 / 8088 Family –Architecture, Programming and Design", Second Edition, Prentice Hall of India, 2007.**PG.NO:456-460**

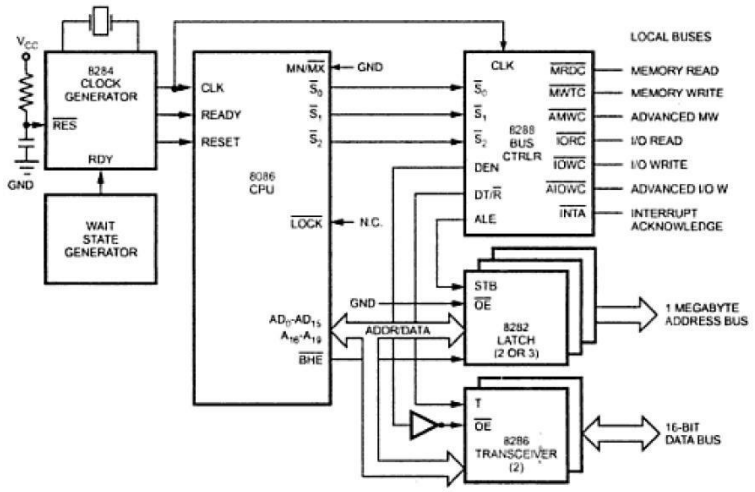
Features of 8087:

1. It can operate on data of the integer, decimal, and real types, with lengths ranging from 2 to 10 bytes.
2. Its instruction set not only includes various forms of addition and subtraction, but also provides many useful functions such as square root, exponential, tangent, and so on.
3. It is high performance numeric data processor. It can multiply two 64-bit real numbers in about 27 μs and calculate square root in about 36 μs.
4. It follows IEEE floating point standard.
5. It is multibus compatible.



(13M)

4.	**Explain the closely coupled configuration of multi-processor configuration with Suitable diagram. (May 2015) (Apr/May 2016) (Apr/May 2017) BTL 4** **Ans: Refer** Yu-Cheng Liu, Glenn A.Gibson, "Microcomputer systems: The 8086 / 8088 Family –Architecture, Programming and Design", Second Edition, Prentice Hall of India, 2007.**PG.NO:460-467** It has P processors, M memory modules and C I/O channels. They are connected through a set of 3 interconnection networks. – PMIN (Processor Memory Interconnection Network) – IOPIN (I/O Processor Interconnection Network) – ISIN (Interrupt Signal Interconnection Network)   **(13M)**
5.	**Discuss the maximum mode configuration of 8086 with a neat diagram. Mention the functions of various signals. (16) (May 2015) APRIL/ MAY 2019 BTL 6** **Ans: Refer** Yu-Cheng Liu, Glenn A.Gibson, "Microcomputer systems: The 8086 / 8088 Family –Architecture, Programming and Design", Second Edition, Prentice Hall of India, 2007.**PG.NO:314-324**

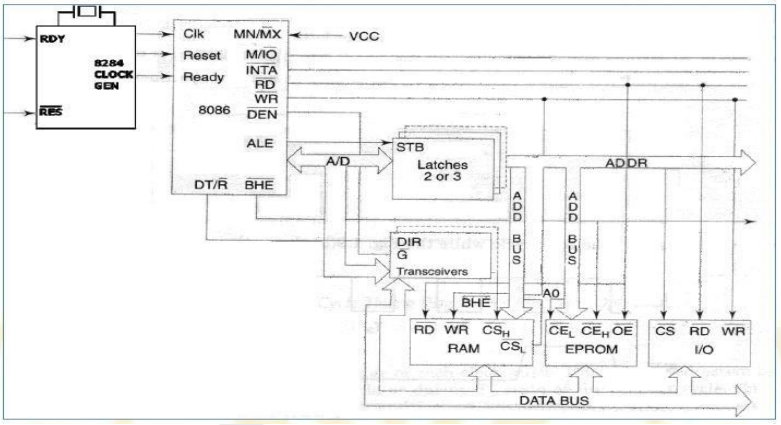


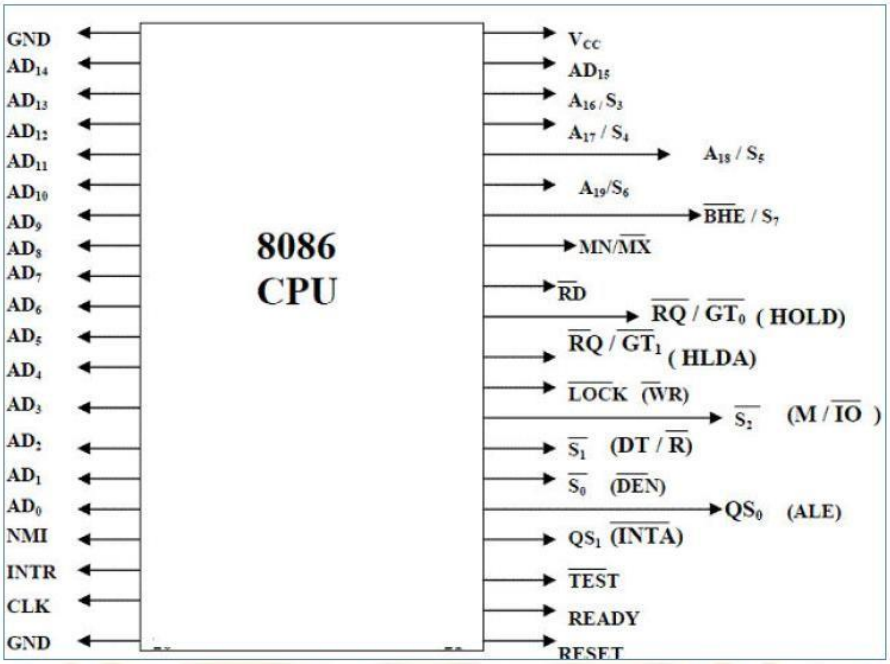
(13M)

6. **Write an 8086 assembly language program to check whether the given string is palindrome. BTL 3**

Ans: Refer Notes

```
DATA SEGMENT
BLOCK1 DB 'MALAYALAM'
MSG1 DB "IT IS PALINDROME $"
MSG2 DB "IT IS NOT PALINDROME $"
PAL DB 00H
DATA ENDS
PRINT MACRO MSG
MOV AH,09H
LEA DX,MSG
INT 21H
INT 3H
ENDM
EXTRA SEGMENT
BLOCK2 DB 9 DUP(?)
EXTRA ENDS
CODE SEGMENT
ASSUME CS:CODE,DS:DATA,ES:EXTRA
START: MOV AX,DATA
MOV DS,AX
MOV AX,EXTRA
MOV ES,AX
LEA SI,BLOCK1
LEA DI,BLOCK2+8
MOV CX,00009H
BACK: CLD
LODSB
STD
STOSB
LOOP BACK
LEA SI,BLOCK1
LEA DI,BLOCK2
MOV CX,0009H
CLD
REPZ CMPSB
JNZ SKIP
PRINT MSG1
```

	SKIP: PRINT MSG2 CODE ENDS END START (13M)
7	**With neat block diagram explain the architecture of 8086 in minimum mode configuration. Also explain the bus timing diagram for input and output transfer on a maximum mode. APRIL/ MAY 2019 BTL 3** 1.A minimum mode of 8086 configuration depicts a standalone system of computer where no other processor is connected. This is similar to 8085 block diagram with the following difference. 2. The Data transceiver block which helps the signals traveling a longer distance to get boosted up. Two control signals data transmit/ receive are connected to the direction input of transceiver (Transmitter/Receiver) and DEN* signal works as enable for this block. **Steps:** • For interfacing memory module to 8086, it is necessary to have odd and even memory banks. This is implemented by using two EPROMs and two RAMs. Data lines DI5-D8 are connected to odd bank of EPROM and RAM,, and data lines D7 - D0 are connected to even bank of EPROM and RAM. • Address lines are connected to EPROM and RAM as per their capacities. • RD signal is connected to the output enable (0E) signals of EPROMs and RAMs. • WR signal is connected to WR signal of RAMs. • Two separate decoders are used to Generate chip select signals for memory and I/O devices. These chip select signals are logically ORed with either BHE or to generate final chip select signals. • RD and WR signals are connected to the RD and WR signals of I/O device. • Data lines D15-D0 are connected to the data lines of I/O device  (13M)
8	**Explain the pin details of 8086 APRIL/ MAY 2018 BTL 3 (13M)**



(3M)

Functional Description (10)

9. **Explain in detail about IO programming. BTL 4 (13M)**

The transfer of data between keyboard and microprocessor, and microprocessor and display device is called input /output data transfer or I/O data transfer. This data transfer is done by using

I/O ports.

Input port:

- It is used to read data from the input device such as keyboard. The simplest form of input port is a buffer. The input device is connected to the microprocessor through buffer. This buffer is a tri-state buffer and its output is available only Enable when enable signal is active. When microprocessor wants to read data from the input device (keyboard), the control signals from the microprocessor activates the buffer by asserting enable Input of the buffer, once the buffer is enabled, data train the Input device is available on the data bus. Microprocessor reeds this data by Initiating reed command.

Output port:

- It is used to send data to the output device such as display from the microprocessor. The simplest form of output port is a latch. The output device is connected *to* the microprocessor through latch. When microprocessor wants to send data to the output device, it puts the data on the data bus and activates the clock signal of the latch.

a. Programmed I/O:

- I/O operations will mean a data transfer between an I/O device and memory or between an I/O device and the CPU. If any computer system I/O operations are completely controlled by the CPU, then that system is said to be using 'programmed I/O'.

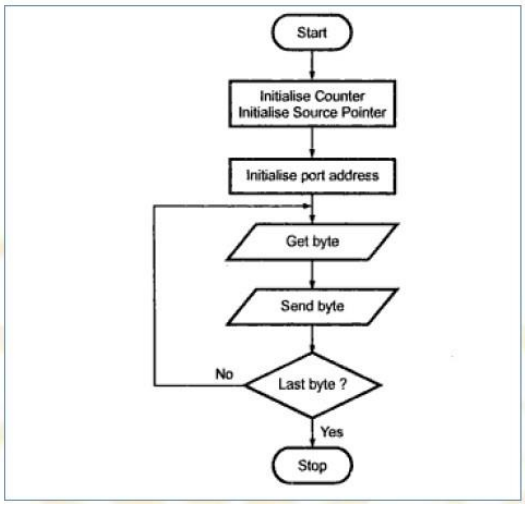
b. Interrupt Driven I/O

- The moat common method of servicing such device is the polled approach. This is where the processor must test each device in sequence. It needs communication with the processor. It is easy to see that a large portion of the main program is looping through this continuous polling cycle. Allows the processor to execute its main program and only stop to service peripheral devices when it is told to do so by the device itself.
- The method would provide an external asynchronous input to the processor. Instruction that is currently being executed and fetch a new routine that will service the requesting device. Once this servicing is completed, the processor would resume exactly where it left off.
- This method of servicing I/O request is called Interrupt driven I/O. When a processor is

interrupted, It stops executing its current program and calls a special routine which services the Interrupt. Interruption is called Interrupt and the special routine executed to service the Interrupt is called Interrupt Service routine (ISR).

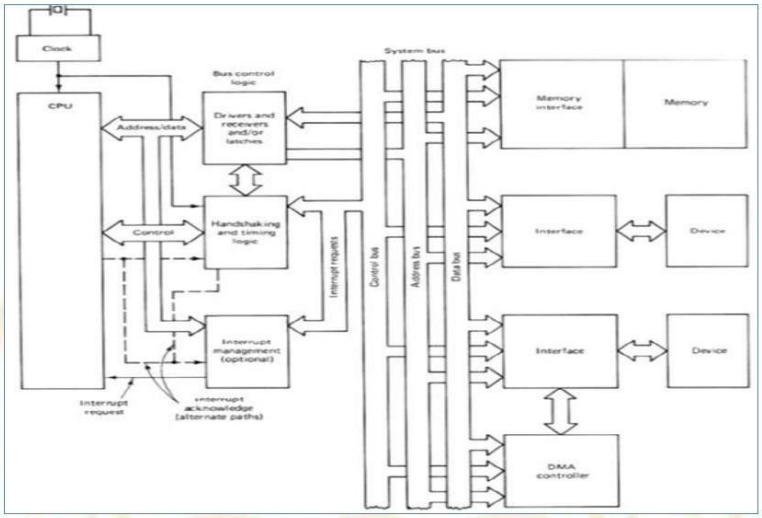
c. Direct Memory Access (DMA) Transfer

• In software control data transfer, processor executes a series of instructions to carry out data transfer. For each instruction execution fetch, decode arid execute phases are required. Fig. gives the flowchart to transfer data from memory to I/O device. So this method of data transfer is not suitable for large data transfers.



(13M)

10 **Write short notes on System Bus Structure. BTL 3 (13M)**



Typical System bus Architecture

(3M)

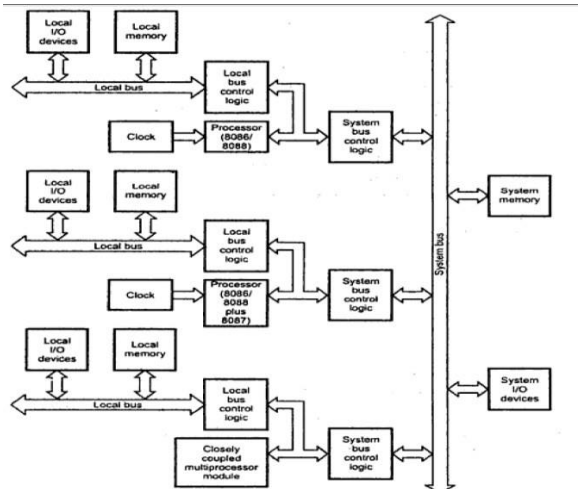
The complexity of the bus control logic depends in the amount of translation needed between the system bus and the pins on the CPU. All of the address and data lines and most of the control lines use are capable of being logically disconnected from the CPU or bus control logic. The timing of the signals within the CPU and bus control logic is controlled by a clock. The bus cycles and CPU activity are controlled by ground of clock pulses. The CPU on put is transaction would processed by outputting the address of the data during first clock cycle.

• Read is to take place during the second clock cycle. Waiting an intermediate number of clock cycles for the addressed device to put the data on the data lines, inputting the data and signaling the device that the transfer is complete during the last clock cycle. (10M)

Part C/ Unit II

1 **Explain the loosely coupled architecture of 8086. (15M) BTL 3 (May 2016)**

The Fig. shows nonhierarchical loosely coupled multiprocessor system. In loosely coupled systems, each processor has a set of input-output devices and a large local memory where it accesses most of the instructions and data. The processor, its local memory and input-output interfaces are together called **computer module**. Processes which execute on different computer modules communicate by exchanging messages through a **Message Transfer System (MTS)**. The coupling in such a system is very loose. Hence, such systems are also referred to as a **distributed systems**.



(15M)

2 **Discuss Multiprogramming concept in detail (15M) BTL 3 (May 2015)**

Multiprogramming:

A process can be defined as a programming unit which performs an independent task. A processor that process (execute) serially, because it can process one task at a time that's why it is called **uniprogramming system. In a multiprogramming** environment, the codes for two 'or' more processes are in memory at the same time and are executed by time-multiplexing.

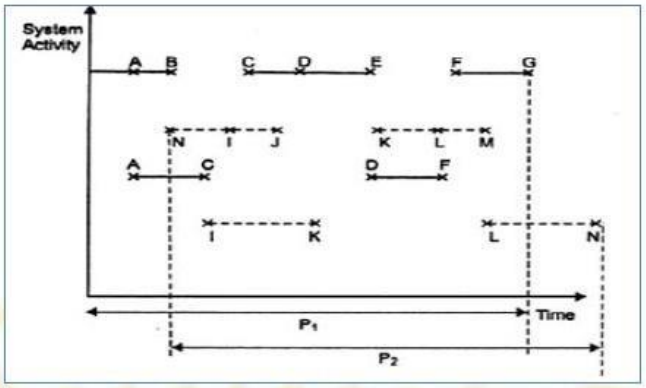
The performance of a system is generally measured in terms of the number of jobs completed in a time period (that is referred as **system through put**).

The following Figure presents completion of a task consisting two processes P1 and P2 by using

uniprogramming.

1) The P1 starts and continue until F/O is required (Point A), then FÍO is initialized and the processing continues in parallel with 1/0 until the processing requires the input data. At this time it should wait until I/O is finished (Point B).

The 110 in finished (Point C) the processing is resumed and the same description applies to point D, E and F. At the end of P1, P2 can start which has the same operation as that P1.



Multiprogramming Approach

(15M)

3 **List the Features of advanced Microprocessor. (15M) BTL 3**

Features (80286)

1) The 80286 is a 16-bit processor. The 16-bit ALU allows to process 16-bit data.
2) It has 24-bit address bus. It can access up to 16 Mbytes (224) of physical memory or 1 Gigabyte (2°) of virtual memory.
3) The 80286 can be operated at three different clock speeds. These are 4 MHz(80286-4), 6 MHz (80286-6), and 8 MHz (80286).
4) The 80286 includes special instructions to support operating systems.
5) The 80286 is housed in a 68-pin leadless flat package.
6) It contains four separate processing units. These are the Bus Unit (BU), the Instruction Unit (lii), the Address Unit (AU) and the Execution Unit (EU
7) The 80286 microprocessor is compatible with their earlier 8086, 8088, 80186 and 80188 chips.
8) It has virtual memory-management circuitry and protection circuitry.

80386 Features:

1) The 80386 is a 32-bit processor. The 32-bit ALU allows to process 32-bit data.
2) It has 32-bit address bus.
3) The 80386 runs with speed up to20 MHz instructions per second.
4) The pipelined architecture of the 80386, allows simultaneous instruction fetching, decoding, execution and memory management.
5) It allows programmers to switch between different operating systems
6) It can operate on 7 different data types:
a. Bit b. Byte c. Word d. Double word e. word f. Quad word g. Ten byte.
7) The 80386 can operate in real mode, protected mode or a variation of protected mode called virtual 8086 mode.

8) The 80386 microprocessor is compatible with their earlier 8086, 8088. (15M)

UNIT III I/O INTERFACING

Memory Interfacing and I/O interfacing - Parallel communication interface – Serial communication interface – D/A and A/D Interface - Timer – Keyboard /display controller – Interrupt controller – DMA controller – Programming and applications Case studies: Traffic Light control, LED display , LCD display, Keyboard display interface and Alarm Controller.

Part A

Q. No.	Questions & Answers

1	**Name the Command word to set bit PC, using BSR mode. BTL 1** 0 | D6 | D5 | D4 | D3 | D2 | D1 | D0 D6,D5,D4 – Don't Care D3,D2,D1- Bit Select Do- Bit set. Reset
2	**Why the 8255A is designed so that only the bits in PORT C can be set/reset? BTL 1** Since the pins are designed to activate for selecting Port A and Port B.
3	**What is the use of BSR mode in 8255 BTL 1** It is used for setting and Reset the Bits
4	**List the advantages and disadvantages of parallel communication over serial communication. (Apr/May 2016) BTL 1** For transferring data between computers, laptops two methods are used, namely, Serial Transmission and Parallel Transmission. There are some similarities and dissimilarities between them. One of the primary differences is that; in Serial Transmission data is sent bit by bit whereas, in Parallel Transmission a byte (8 bits) or character is sent.
5	**What is key bouncing? (Apr/May 2016) BTL 1** When a key is pressed the contact bounce back and forth and settle down only after a small time delay (about 20ms). Even though a key is actuated once, it will appear to have been actuated several times. This problem is called Key Bouncing
6	**How does 8255 PPI discriminate between the memory section data and I/O section data BTL 1** The 8255 PPI discriminate between memory section data and I/O Section by use of the Address lines and by use of the decoder.
7	**What is the function of STB and OBF signal in the 8255 when programmed for mode –1 operation? BTL 1** The input device activates this signal to indicate CPU that the data to be read is already sent on the port lines of 8255 port.
8	**Name the major block of 8259 Programmable Interrupt Controller. BTL 1** There are three major blocks 1.Interrupt service register , 2.Priority resolver, 3.Interrrupt Request Register, 4.Interrupt Mask Register
9	**What are the modes of operation of 8259 Interrupt Controller? BTL 1** 1. Fully Nested Mode, 2.Special Fully Mode, 3.Rotating Priority Mode, 4.Special masked Mode, 5.Polled Mode.
10	**What is the maximum number of devices that can be connected to interrupt mode BTL 1** We can connect 8 Devices in the interrupt mode
11	**Mention the function of SP/EN signal in the 8259 PIC. BTL 1** With the help of SP/EN signal it can either be operated in Master mode and Salve Mode
12	**Why CAS2-CAS0 lines on 8259 PIC are bi-directional? BTL 1** CAS2-CAs0 is used for selecting one of the possible slaves that can be connected.
13	**What is the use of address enable (AEN) pin of 8257 DMA Controller? BTL 1** ALE is used to differentiate between the Address and Data Signals.
14	**What are the operating modes of 8255? (Nov/Dec 2013) BTL 1** Mode-0, Mode-1 and Mode-2.
15	**What is bus stealing? (Nov/Dec 2013) BTL 1** During DMA data transfer, the I/O component connected to the system bus is given control of the system bus for a bus cycle. This is called bus stealing or cycle stealing.

16 **What are the advantages of Programmable Interval Timer/Counter IC? (May/Jun 2014) BTL 1**

- Interrupt a time sharing operating system at evenly spaced intervals.
- Output precisely timed signals with programmed period to an I/O device.
- Count the number of times an event occurs in an external experiment.

Cause the processor to be interrupted after a programmable number of external events have occurred.

17 **List the features of Memory Mapped I/O. (May/Jun 2014) BTL 1**

- The device registers can be accessed and manipulated with any instruction or addressing mode.

The maximum number of available memory locations is reduced.

18 **Give the Various modes and Applications of 8254. (May/Jun 2015) BTL 1**

- MODE 0 : Interrupt on terminal Count (can be used as Interrupt).
- MODE 1 : Hardware re trigger able One shot (For generating One shot Pulse)

MODE 2 : Rate Generator (The mode is used to generate a pulse equal to given clock period at a given interval.)

- MODE 3: Square wave generator (For generating continuous square wave)
- MODE 4: Software triggered strobe (To trigger after a specific count)

MODE 5: Hardware triggered strobe (To Trigger by a hardware event)

19 **Draw the format of read back command register of 8254. (Apr/May 2017) BTL 1**

This register is accessed when lines A0 & A1 are at logic 1. It is used to write a command word, which specifies the counter to be used, its mode, and either a read or write operation. Following table shows the result for various control inputs.

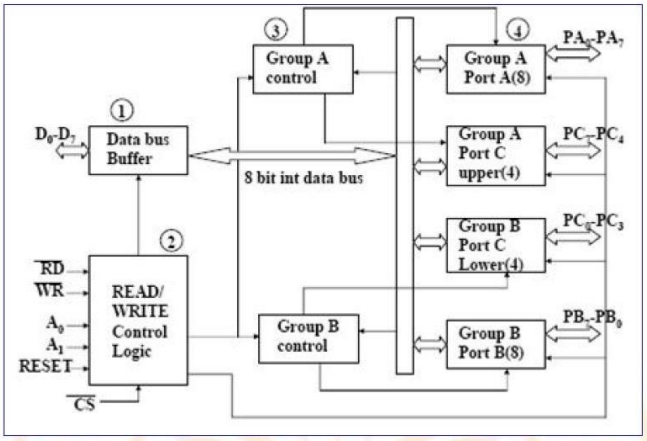
A1	A0	RD	WR	CS	Result
0	0	1	0	0	Write Counter 0
0	1	1	0	0	Write Counter 1
1	0	1	0	0	Write Counter 2
1	1	1	0	0	Write Control Word
0	0	0	1	0	Read Counter 0
0	1	0	1	0	Read Counter 1
1	0	0	1	0	Read Counter 2
1	1	0	1	0	No operation
X	X	1	1	0	No operation
X	X	X	X	1	No operation

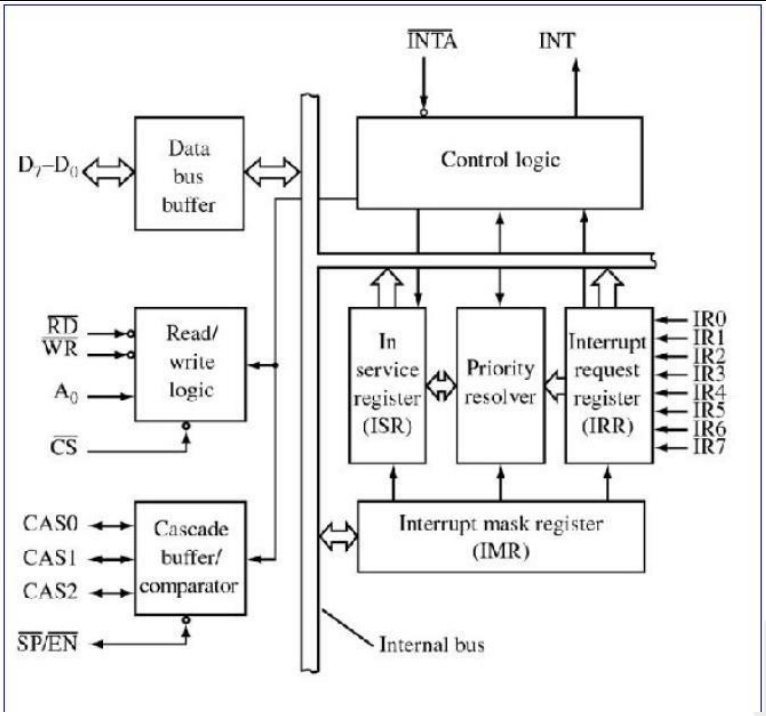
20 **What is meant by Direct Memory Access? BTL 1**

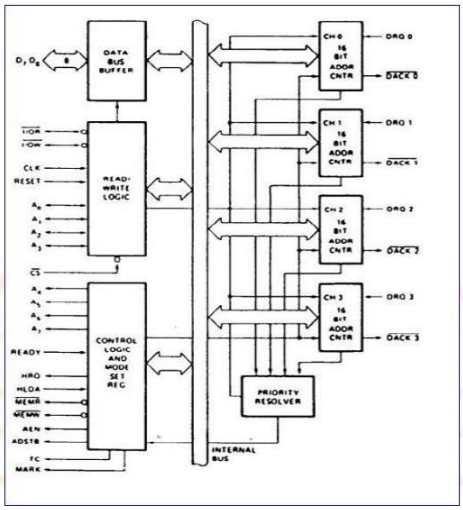
Direct Memory Access (DMA) is a capability provided by some computer bus architectures that allows data to be sent directly from an attached device (such as a disk drive) to the memory on the allows data to be sent directly from an attached device (such as a disk drive) to the memory on the computer's motherboard. The microprocessor is freed from involvement with the data transfer, thus speeding up the overall computer.

21 **What is meant by control register? BTL 1**

	A control register is a processor register which changes or controls the general behavior of a CPU or other digital device. Common tasks performed by control registers include interrupt control, switching the addressing mode, paging control, and coprocessor control.
22	**Write a 16 bit delay program in 8086 (Apr/May 2017) BTL 1** LOOP1: MOV DI, 01ADH LOOP: MOV BP, FFFFH NOP NOP NOP DEC BP JNZ LOOP1 DEC DI JNZ LOOP
23	**Give the applications of I/O interface BTL 1** 1. Traffic Light Control 2. LED and LCD Display Alarm Controller
24	**List the applications of D/A interface. BTL 1** The DAC find applications in areas like Digitally controlled gains Motor speed controls Programmable gain amplifiers etc.
25	**What is mode o operation of 8255? BTL 1** **APRIL /MAY 2019.** Two 8-bit ports (port A and port B) and two 4-bit ports (port C upper and lower) are available. The two 4-bit ports can be combined used as a third 8-bit port. 2. Any port can be used as an input or output port. 3. Output ports are latched. Input ports are not latched. 4. A maximum of four ports are available so that overall 16 I/O configurations are possible.
26	**What are the operating modes in 8279? APRIL /MAY 2019. BTL 1** 8279 provides two output modes for selecting the display options. **1.Display Scan:** In this mode, 8279 provides 8 or 16 character-multiplexed displays those can be organized as dual 4-bit or single 8-bit display units. **2. Display Entry:**8279 allows options for data entry on the displays. The display data is entered for display from the right side or from the left side.
	Part B/Unit III
1	**With a block diagram of internal structure of 8255 PPI and explain the functions of each block Illustrate the 8255 mode 1 output and input port timings. (Apr/May 2017) BTL 5 (13M)** **Ans: Refer** Yu-Cheng Liu, Glenn A.Gibson, "Microcomputer systems: The 8086 / 8088 Family -Architecture, Programming and Design", Second Edition, Prentice Hall of India, 2007.**PG.NO:369-377** The parallel input-output port chip 8255 is also called as programmable peripheral input-output port. The Intel's 8255 is designed for use with Intel's 8-bit, 16-bit and higher capability microprocessors. It has 24 input/output lines which may be individually programmed in two groups of twelve lines each, or three groups of eight lines. The two groups of I/O pins are named as Group A and Group B. Each of these two groups contain a subgroup of eight I/O lines called as 8-bit port and another subgroup of four lines or a 4-bit port. Thus group A contains an 8-bit port A along with

	a 4-bit port, C upper. The port A lines are identified by symbols PA0 – PA7 while the port C lines are identified as PC4 – PC7. Similarly, Group B contains an 8-bit port B, containing lines PB0 – PB7 and a port C with lower bits PC0 – PC3. The port C upper and port C lower can be used in combination as an port 8-bit port C.  (13M)
2	**With a neat block diagram explain the function of each block of a programmable interrupt controller**. **BTL 5 (13M)** **Ans: Refer** Yu-Cheng Liu, Glenn A.Gibson, "Microcomputer systems: The 8086 / 8088 Family -Architecture, Programming and Design", Second Edition, Prentice Hall of India, 2007.**PG.NO:361-369** **Interrupt Request Register (IRR):** The interrupts at IRQ input lines are handled by Interrupt Request Register internally. IRR stores all the interrupt requests in it in order to serve them one by one on the priority basis. **IN-service Register (ISR):**This stores all the interrupt requests those are being served, i.e. ISR keeps track of the requests being served. **Priority Resolver:** This unit determines the priorities of the interrupt requests appearing simultaneously. The highest priority is selected and stored into the corresponding bit of ISR during INTA pulse. The IR_0 has the highest priority while the IR_7 has the lowest priority, normally in fixed priority mode. The priorities however may be altered by programming the 8259A in rotating priority mode. **Interrupt Mask Register (IMR):** This register stores the bits required to mask the interrupt inputs. IMR operates on IRR at the direction of the Priority resolver. **Interrupt Control Logic**:This block manages the interrupt and interrupt acknowledge signals to be sent to the CPU for serving one of the eight interrupt requests. This also accepts the interrupt acknowledge (INTA) signal from CPU that causes the 8259A to release vector address on to the data bus. **Data Bus Buffer:** This tristate bi-directional buffer interfaces internal 8259A bus to the microprocessor system data bus. Control words, status and vector information pass through data buffer during read/write operations.

	 **(13M)**
3	**Draw the block diagram of DMA controller IC and explain the function of each block. (May 2015) & (May 2014) (Apr/May 2016) (Apr/May 2017) BTL 5** (13M) **Ans: Refer** Yu-Cheng Liu, Glenn A.Gibson, "Microcomputer systems: The 8086 / 8088 Family -Architecture, Programming and Design", Second Edition, Prentice Hall of India, 2007.**PG.NO:395-402** The direct memory access or DMA mode of data transfer is the fastest amongst all the modes of data transfer. In this mode, the device may transfer data directly to/from memory without any interference from the CPU. The device requests the CPU (through a DMA controller) to hold its data, address and control bus, so that the device may transfer data directly to/from the memory. Intel's 8257 is a four channel DMA controller designed to be interfaced with their family of microprocessors. The 8257, on behalf of the devices, request the CPU for bus access using local bus request input I.e. HOLD in minimum mode. In maximum mode of the microprocessor RQ/GT pin is used as bus request input. On receiving the HLDA signal or RQ/GT signal from the CPU, the requesting device gets the access of the bus, and it completes the required number of DMA cycles for the data transfer and then hands over the control of the bus back to the CPU. The chip supports four DMA channels, i.e. four peripherals can be independently request for DMA data transfer through these channels at a time. The DMA controller has 8-bit internal data buffer, a read/write unit, a control unit, a priority resolving unit along with a set of registers. **Register organization of 8257**: The 8257 performs the DMA operation over four independent DMA channels. Each of the four channels of 8257 has a pair of two 16-bit registers, namely, DMA address register and terminal count register. Also, there are two common registers for all the channels namely mode set register and status register. The CPU selects one of these registers using A0 – A3.



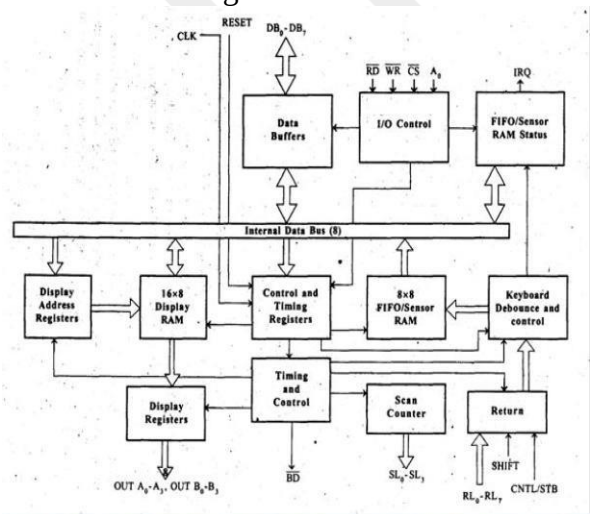
(13M)

4 **With a block schematic explain how a (4x4) matrix hex keyboard can be interfaced to a CPU using 8279 keyboard display controller? (Nov 2013) BTL 5 (13M)**

Ans: Refer Yu-Cheng Liu, Glenn A.Gibson, "Microcomputer systems: The 8086 / 8088 Family -Architecture, Programming and Design", Second Edition, Prentice Hall of India, 2007.**PG.NO:383-395**

Intel's 8279 is a general purpose keyboard display controller that simultaneously drives the display of a system and interfaces a keyboard with the CPU leaving the CPU free for its routine task. The keyboard display interface scans the keyboard to identify if any key has been pressed and sends the code if the pressed key to the CPU. This also transmits the data received from the CPU to the display device. The controller performs both of these operations without involving the CPU.

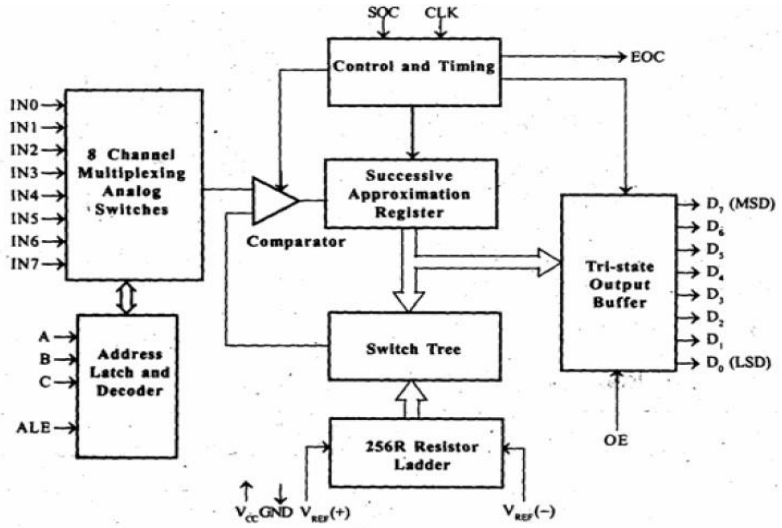
The 8279 is a 40 pin drive with two major segments, Keyboard and Display. The keyboard can be connected to a max of 64 – contact ky matrix. Keyboard entries are denounced and stored in the internal FIFO RAM and an interrupt signal is generated with each entry. The display segment can provide a 16 character (byte) scanned display. This segment contains 16 x 8 R/w memory (RAM), which can be used to read or write information for the display purposes. This 16-byte display RAM can be used either as an integrated block of 16 x 8 bits or 16 x 4 bits of 2 blocks. The internal architecture of 8279 is shown in the fig.



(13M)

5 **Interface a D/A converter and A/D convertor with a microprocessor. Explain with a Program, how to generate a sine wave using this. (May 2015) BTL 6 (13M)**

Ans: Refer Yu-Cheng Liu, Glenn A.Gibson, "Microcomputer systems: The 8086 / 8088 Family -Architecture, Programming and Design", Second Edition, Prentice Hall of India,

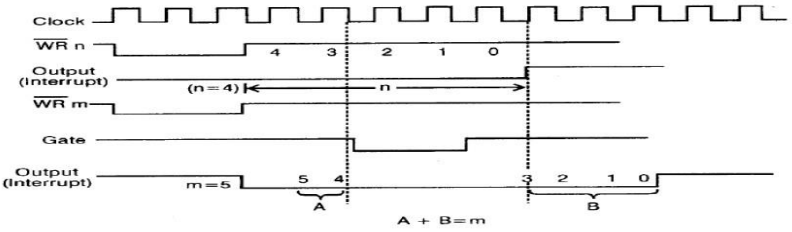
	2007.**PG.NO:374-377** • ADC0809 is an 8-bit successive approximation type ADC with inbuilt 8-channel multiplexer. • The ADC0809 is suitable for interface with 8086 microprocessor. • The ADC0809 is available as a 28 pin IC in DIP (Dual Inline Package). • The ADC0809 has a total unadjusted error of ±1 LSD (Least Significant Digit). • The ADC0808 is also same as ADC0809 except the error. The total unadjusted error in ADC0808 is ± 1/2 LSD.  • To convert the digital signal to analog signal a Digital-to-Analog Converter (DAC) has to be employed. • The DAC will accept a digital (binary) input and convert to analog voltage or current. • Every DAC will have "n" input lines and an analog output. • The DAC require a reference analog voltage (Vref) or current (Iref) source. • The smallest possible analog value that can be represented by the n-bit binary code is called resolution. • The resolution of DAC with n-bit binary input is 1/2nof reference analog value. • Every analog output will be a multiple of the resolution. (13M)
6	**Describe with MODE 0 and MODE 3 configurations of 8254 timer in detail.(13M)** **BTL 6** **Ans: Refer** Yu-Cheng Liu, Glenn A.Gibson, "Microcomputer systems: The 8086 / 8088 Family -Architecture, Programming and Design", Second Edition, Prentice Hall of India, 2007.**PG.NO:380-382**

Mode 0: Interrupt On Terminal Count

- Mode 0 is typically used for event counting.
- After the Control Word is written, OUT is initially low, and will remain low until the Counter reaches zero. OUT then goes high and remains high until a new count or a new Mode 0 Control Word is written into the Counter.

  GATE = 1 enables counting;

  GATE = 0 disables counting. GATE has no effect on OUT.
- After the Control Word and initial count (say, n =4, m = 5) are written to a Counter, the initial count will be loaded on the next CLK pulse.
- This mode can be used as an interrupt.



Mode 3: Square Wave Mode

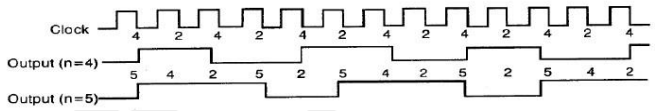
- Mode 3 is typically used for Baud rate generation.
- Mode 3 is similar to Mode 2 except for the duty cycle of OUT. OUT will initially be high. When half the initial count has expired, OUT goes low for the remainder of the count.
- Mode 3 is periodic; the sequence above is repeated indefinitely. An initial count of N results in a square wave with a period of N CLK cycles.
- Mode 3 is implemented as follows:

Even counts:

OUT is initially high. The initial count is loaded on one CLK pulse and then is decremented by two on succeeding CLK pulses. When the count expires OUT changes value and the Counter is reloaded with the initial count. The above process is repeated indefinitely.

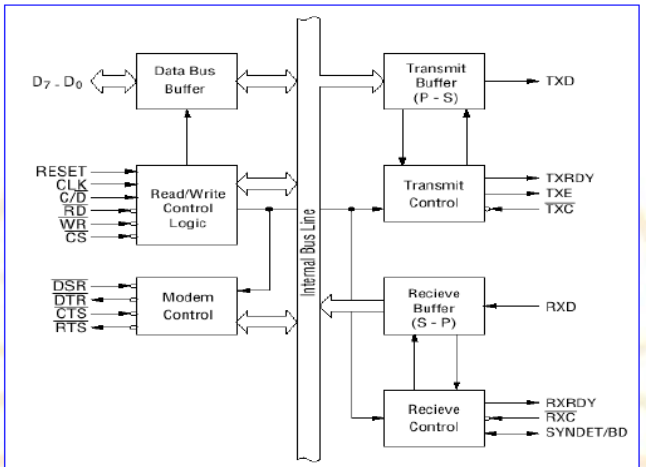
Odd counts:

For odd counts, OUT will be high for (N +1)/2 counts and low for (N - 1)/2 counts.



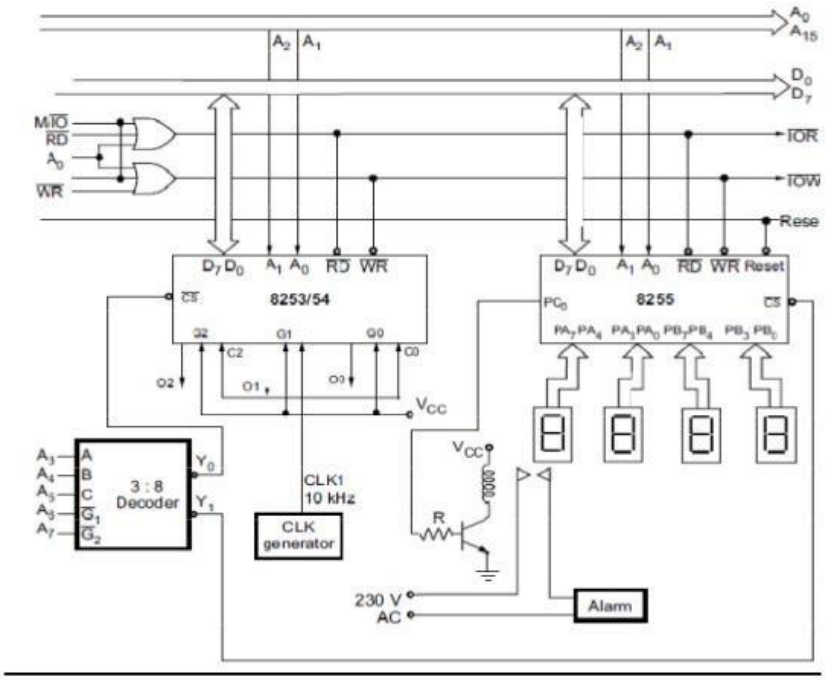
(13M)

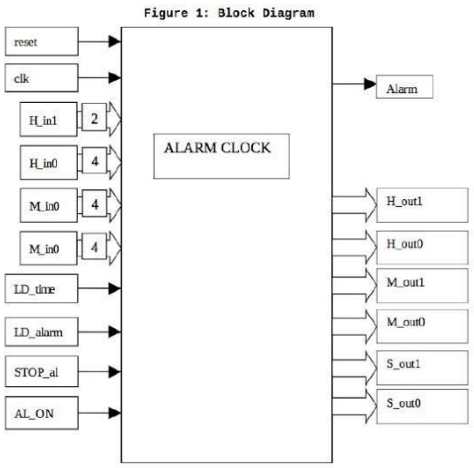
7 **(i) Bring about the features of 8251. (6) (Nov 2013)**
(ii) Discuss how 8251 is used for serial data communication. (6). **APRIL /MAY 2019.**
(iii) **Explain the advantages of using the USART chips in microprocessor based systems. (7) BTL 6** (13M)
Ans: Refer Yu-Cheng Liu, Glenn A.Gibson, "Microcomputer systems: The 8086 / 8088 Family -Architecture, Programming and Design", Second Edition, Prentice Hall of India, 2007.**PG.NO:361-369**
Architecture of 8251:
The data buffer interfaces the internal bus of the circuit with the system bus. The read write logic controls the operation of the peripheral depending upon the operations initiated by the CPU. This unit also selects one of the two internal addresses those are control address and data address at the behest of the c/d SIGNAL. The modem control unit handles the modem handshake signals to coordinate the communication between the modem and the USART. The transmit control unit transmits the data byte received by the data buffer from the CPU for further serial communication.



(13M)

8 **Draw and explain the block diagram of alarm controller. (Apr/May 2016) BTL 6**
Ans: Refer Notes (13M)

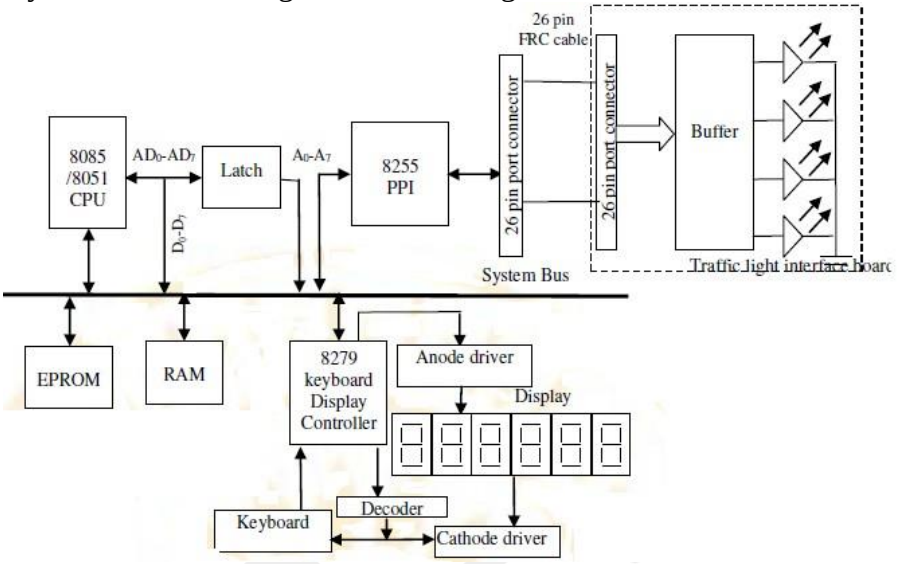




(13M)

9 **Explain design of Traffic Light Controller using 8086 microprocessor in detail. BTL 5 (May 2015)** (13M)
Ans: Refer Notes
The 8085'8051 Microprocessor/ Microcontroller is a popular Microprocessor/Microcontroller

used in Industries for various applications. Such as traffic light control, temperature control, stepper motor control, etc. The traffic lights are interfaced to Microprocessor/ Microcontroller system through buffer and ports of programmable
peripheral Interface 8255. So the traffic lights can be automatically switched ON/OFF in desired sequence. The Interface board has been designed to work with parallel port of Microprocessor/ Microcontroller system. The hardware of the system consists of two parts. The first part is Microprocessor / Microcontroller based system. Microprocessor/ Microcontroller as CPU and the peripheral devices like EPROM, RAM, Keyboard & Display Controller 8279, Programmable as Peripheral Interface 8255, 26 pin parallel port connector, 21 keys Hexa key pad and six number of seven segment LED's. The second part is the traffic light controller interface board, which consist of 36 LED's in which 20 LED's are used for vehicle traffic and they are connected to 20 port lines of 8255 through Buffer. Remaining LED's are used for pedestrian traffic. The traffic light interface board is connected to Main board using 26 core flat cables to 26-pin Port connector. The LED's can be switched ON/OFF in the specified sequence by the Microprocessor/ Microcontroller. The block diagram of the system is shown in fig.1. The layout of the traffic light is shown in fig 2.



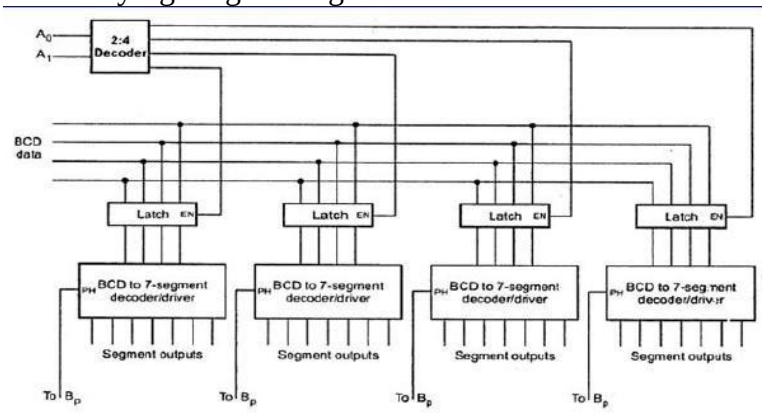
(13M)

10 **Explain in detail about interfacing of four LCD digits to 8086. APRIL /MAY 2019. BTL 5 (13M)**

LED displays are available in two very common formats.
1. 7 segment displays
2. 5 by 7 dot-matrix displays.

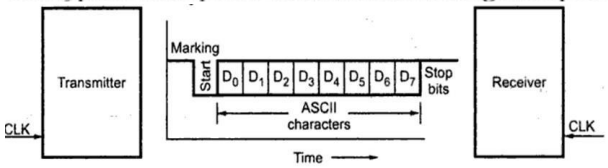
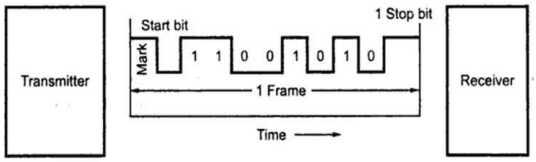
Seven-Segment display

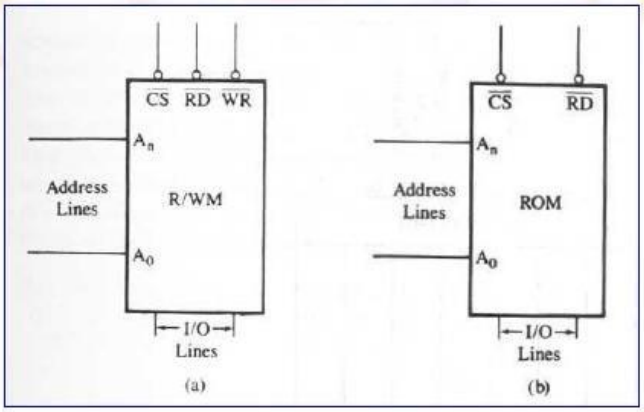
Seven segment displays are generally used as numerical indicators. Any number between O and 9 can be indicated by lighting the Segments.



(13M)

Part C

1	With block diagram explain the serial communication interface. **(16)** ***Dec 03,04,07,11, May 07,08,10,11,13.*** **BTL 5 (15M)** **Classification** Serial data transmission can be classified on the basis of how transmission occurs. 1. Simplex 2. Half duplex 3. Full duplex **Simplex** In simplex, the hardware exists such that data transfer takes place only in one direction. There is no possibility of data transfer in the other direction. A typical example is transmission from a computer to the printer. **Half Duplex** The half duplex transmission allows the data transfer in both directions, but not simultaneously. A typical example is a walkie-talkie. **Full Duplex** The full duplex transmission allows the data transfer in both direction simultaneously. The typical example is transmission through telephone lines.  **Transmission format for asynchronous transmission**  **Asynchronous format with data byte CAH** (15M)
2	**Explain the Memory Interfacing in detail. BTL 5 (15M)** **Interfacing:** An interface is a shared boundary between the devices which involves sharing information. Interfacing is the process of making two different systems communicates with each other. Memory is an essential component of microcomputer system; it stores binary instructions and data for the microprocessor. They can be classified in two groups: prime (or main) memory and storage memory. The R/W memory is made up of registers, and each register can use this memory to hold programs and store data. On the other hand, the ROM stores information permanently in the form of diodes. **Memory mapping:** The assignment of memory addresses to various registers in a memory chip is called as memory mapping. **The requirements of a memory chip.** 1. A memory chip requires address lines to identify a memory register, a chip select CS signal. 2. The number of address lines required is determined by the number of registers in a chip (2_n) 3. If additional address lines are available in a system, chip select signal is used. 4. The control signal Read (RD) enables the output buffer. The control signal Write (WR) enables the input buffer.



Memory Map and Address (15M)

3 **Explain the mode of operation of 8255 BTL 5 (15M) May 15**

MODES OF OPERATION OF 8255

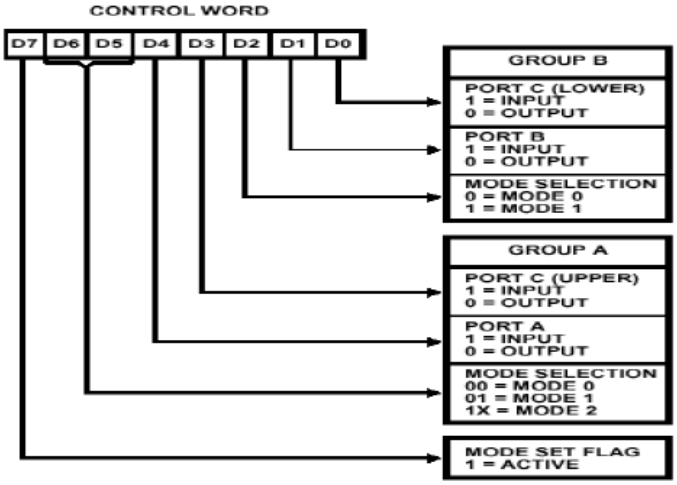
There are two basic modes of operation of 8255 viz. I/O mode and Bit Set-Reset mode (BSR). In I/O mode, the 8255 ports work as programmable I/O ports, while in the BSR mode only port C ($PC_0 – PC_7$) can be used to set or reset its individual port bits.

If D7=1,bits D6-D0 determines i/o functions in various mode.

If bit D7=0, port C operates in the bit Set , Reset mode. BSR control word does not affect the functions of port A and B.

To communicate with peripherals through the 8255A, three steps are necessary:

1.Determine the address of port A,B and C and of the control register according to the chip select logic and address lines A0 and A1.



(15M)

UNIT IV MICROCONTROLLER	
Architecture of 8051 – Special Function Registers(SFRs) - I/O Pins Ports and Circuits - Instruction set - Addressing modes - Assembly language programming.	
PART A	
Q. No.	**Questions & Answers**

1	**Discuss the salient features of 8051 family of controllers? BTL 6** Eight-bit CPU with registers A (the accumulator) and B. Sixteen-bit program counter (PC) Data pointer (DPTR). Eight-bit program status word (PSW) Eight-bit stack pointer (SP). Internal ROM or EPROM (4 KB) Internal RAM (128 bytes) 1. Four register banks (each 8 registers) 2. 16 bytes, which may be addressed at bit level 3. Eighty bits of general purpose data memory Two 16-bit timer / counters: T0 & T1 Full duplex serial data receivers / transmitter (SBUF) Control registers: TCON, TMOD, SCON, PCON, IP and IE.
2	**What is the size of RAM in 8051? BTL 1** The size of the RAM is **128 bytes** 1. Four register banks (each 8 registers) 2. 16 bytes, which may be addressed at bit level Eighty bits of general purpose data memory
3	**How many ports are available in 8051 micro controller? BTL 1** There are mainly four ports available in this 8051 micro controller. They are **Port0:** serve as inputs, outputs, or, when used together, as a bi-directional low order address and as data bus for external memory. **Port1:** has got no dual functions. **Port2:** may be used as an input / output port similar in operation to port 1. The alternate use of port2 is to supply a high-order address byte in conjunction with the Port0 low-order byte to address external memory. **Port3:** is an input / output pin similar to the Port 1. In this case each and every pin has an additional function.
4	**How to select the register bank of Intel 8051. (May 2015) BTL 1** RS0 and RS1 are the D3 and D4 bits present in the 8-bit register of the PSW
	0 BANK 0 is selected from Internal ROM 1 BANK 1 is selected from Internal ROM 2 BANK 2 is selected from Internal ROM 3 BANK 3 is selected from Internal ROM
5	**List the flags of 8051 and give their usage. BTL 1** Status flags: These flags are modified according to the result of arithmetic and logical operations. 1. Carry flag, 2. Auxiliary carry flag, 3. Overflow flag, 4. Parity flag and General purpose user flags: These flags can be set or cleared by the programmer as desired 1. Flag 0, 2. GF0, 3. GF1
6	**What is the difference between microprocessor and microcontroller? (May 2014) BTL 1**

It has only CPU	It has CPU, memory, I/O, Timer, AD converter	
It has more number of instructions for	It has less number of instructions for transferring data from external	

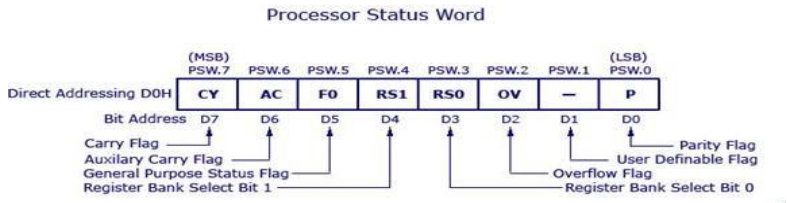
	transferring data from external memory.	memory.	
	No special function registers are available	special function registers are available	
7	**What is the function of DPTR register? BTL 1** The data pointer (DPTR) is the 16-bit address register that can be used to fetch any 8 bit data from the data memory space. When it is not being used for this purpose, it can be used as two eight bit registers, DPH and DPL		
8	**What is the significance of EA line of 8051 microcontroller? (May/Jun 2014) BTL 1** When there is no on-chip ROM in microcontroller and EA pin is connected to GND, it indicates that the code is stored in external ROM.		
9	**What is the difference between MOVX and MOV ? (Nov/Dec 2013) BTL 1** The MOV instruction is used to access code space of on-chip ROM and MOVX instruction is used to access data space or external memory.		
10	**What are the different ways of operand addressing in 8051? (Apr/May 2016) BTL 1** Different ways of addressing modes are**1)** Immediate addressing mode **2)** Direct addressing mode **3)** Register direct addressing mode **4)** Register indirect addressing mode **5)** Indexed addressing mode.		

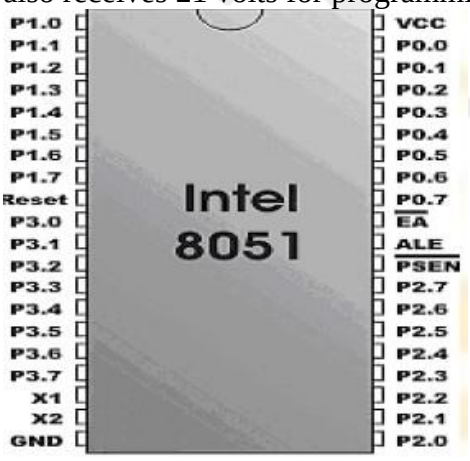
11	**Write an 8051 ALP to toggle P1 a total of 200 times. Use RAM location 32H to hold your counter value instead of registers R0-R7. (Apr/May 2016) BTL 1**
	MOV P1,#55H ;P1=55H
	MOV 32H,#200 ;load counter value into RAM loc 32H
	LOP1: CPL P1 ;toggle P1
	ACALL DELAY
	DJNZ 32H,LOP1 ;repeat 200 times		

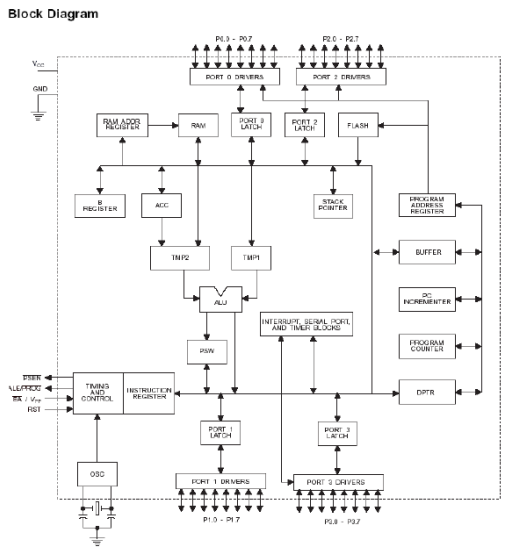
12	**Mention some of the 8051 special function register. BTL 1** ACC: Accumulator, B: B-Register, PSW: Program Status Word, SP: Stack Pointer, DPTR: Data Pointer, IE: Interrupt Enable, SCON: Serial Control, PCON: Power Control.		
13	**What is the function of XTAL 1 and XTAL 2 pins? BTL 1** 8051 internal clock circuit. In this crystal of proper frequency can be connected to these two pins. XTAL 1 is connected to GND and oscillator signal is connected to XTAL 2.		
14	**Write an ALP to add the values ABH and 47H. Store the result in R1. BTL 1** MOV A, #AB H ADD A, #47 H MOV R1, A L1: SJMP L1		
15	**How is RAM memory space allocated in 8051? BTL 1** 1. 32 bytes from 00 to 1F H is for register bank and stack. 2. 16 bytes from 20H to 2FH is for bit addressable read/write memory 80 byte 30H to 7FH is for scratch pad		
16	**What is the purpose of overflow flag? BTL 1** The overflow flag is usually a single bit in a system status register used to indicate when an arithmetic overflow has occurred in an operation, indicating that the signed two's-complement result would not fit in the number of bits used for the operation (the ALU width).		
17	**What is the difference between LCALL and ACALL instructions? BTL 1** The ACALL instruction calls a subroutine located at the specified address. The PC is incremented twice to obtain the address of the following instruction. The 16-bit PC is then stored on the stack (low-order byte first) and the stack pointer is incremented twice. No flags are affected. The LCALL instruction calls a subroutine located at the specified		

	address. This instruction first adds 3 to the PC to generate the address of the next instruction. This result is pushed onto the stack low-byte first and the stack pointer is incremented by 2. The high-order and low-order bytes of the PC are loaded from the second and third bytes of the instruction respectively. Program execution is transferred to the subroutine at this address. No flags are affected by this instruction.
18	**What is the operation of the given 8051 microcontroller instruction XRL A? BTL 1** The XRL instruction performs a logical exclusive OR operation between the specified operands. The result is stored in the destination operand.

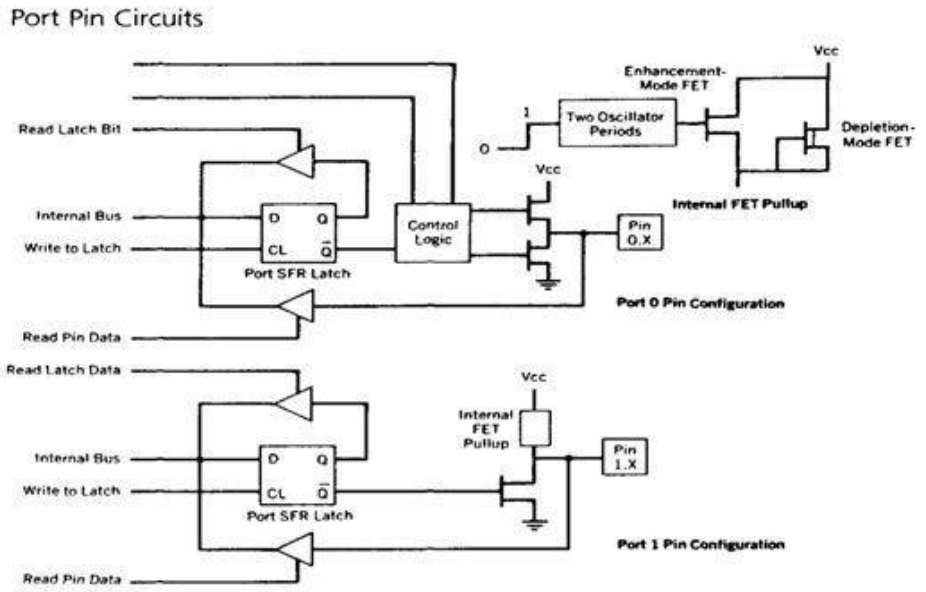
19	**Write a program to perform multiplication of 2 numbers using 8051? BTL 1**
	MOV A, #data1
	MOV B, #data2
	MUL AB
	MOV DPTR, # 4500H
	MOVX @ DPTR, A
	INC DPTR
	MOV A,B
	MOVX @ DPTR, A
	STOP : SJMP STOP

20	**Write a program to perform 2's complement of a given number using 8051? BTL 1** MOV DPTR, # 4500H MOVX A, @ DPTR CPL A ADD A,#01H INC DPTR STOP : SJMP STOP
21	**Which port used as multifunction port? List the signals. (Apr/May 2017) BTL 1** Port 3 has multifunction port. Each pin of port 3 has i/o or as of one of the alternate function. Signals are: P3.0– RXD P3.1– TXD P3.4– T0 P3.5- T1
22	**Illustrate the CJNE instruction (Apr/May 2017) BTL 1** **CJNE-** Compare and jump if not equal. This instruction compares the magnitudes of the source byte and the destination byte.
23	**If a 12 Mhz crystal is connected with 8051, how much is the time taken for the count in timer 0 to get incremented by one? BTL 1** Baud rate = oscillator frequency/12 = (12 X 106) / 12=1 X106Hz T = 1/f = 1 /(1 X 106) = 1 μ sec.
24.	**Which bits of the PSW are responsible for selection of the register banks? <u>APRIL/MAY 2019</u> BTL 1** 

25	**For an 8051 system of 11.0592 Mhz find the time delay for the following subroutine: APRIL/MAY 2019 BTL 1** **MACHINE CYCLE** **DELAY MOV R3 # 250 1** **NOP 1** **NOP 1** **NOP 1** **NOP 1** **DJNZ R3 ;HERE 2** **RET 1**
	Part B/Unit IV
1	**Draw & explain the pin configuration of 8051 in detail(May 2014) BTL 5 (13M)** **Ans: Refer:**Mohamed Ali Mazidi, Janice Gillispie Mazidi, Rolin McKinlay, "The 8051 Microcontroller and Embedded Systems: Using Assembly and C", Second Edition, Pearson Education, 2011.**PG.NO:75-79** 8051 is available in a 40 pin plastic and ceramic DIP packages. The pin diagram of 8051 is shown in the following figure. **Vcc:** This is a +5V supply voltage pin. **Vss:** This is a return pin for the supply. **RESET:** The reset input resets the 8051, only when it goes high for two or more machine cycles. For a proper initialization after reset, the clock must be running. **ALE/PROG:** The latch enable output pulse indicates that the valid address bits are available on their respective pins. This ALE signal is valid only for external memory accesses. Normally, the ALE pulses are emitted at a rate of one-sixth of the oscillator frequency. This pin acts as program pulse input during on-chip EPROM programming. ALE may be used for external timing or clocking purpose. One ALE pulse is skipped during each access to external data memory. **EA/VPP:** External access enable pin, if tied low, indicates that the 8051 can address external program memory. In other words, the 8051 can execute a program in external memory, only if EA is tied low. For execution of programs in internal memory, the EA must be tied high. This pin also receives 21 volts for programming of the on-chip EPROM.  (13M)
2	**Explain in detail the different addressing modes supported by 8051.APRIL/MAY 2019. BTL 5 (13M)** **Ans: Refer:**Mohamed Ali Mazidi, Janice Gillispie Mazidi, Rolin McKinlay, "The 8051 Microcontroller and Embedded Systems: Using Assembly and C", Second Edition, Pearson Education, 2011.**PG.NO:90-96** 8051 supports six addressing modes as listed below. 1. Direct Addressing

	2. Indirect Addressing 3. Register Indirect 4. Register specific (Register Implicit) 5. Immediate mode 6. Indexed Addressing (13M)
3	**Draw the architecture of 8051 and explain.(16) (May 2015)** **(Apr/May 2016) BTL 5 (13M)** **Ans: Refer:**Mohamed Ali Mazidi, Janice Gillispie Mazidi, Rolin McKinlay, "The 8051 Microcontroller and Embedded Systems: Using Assembly and C", Second Edition, Pearson Education, 2011.**PG.NO:22-23** **Accumulator (ACC):** The accumulator register (ACC or A) acts as an operand register. This may either be implicit or specified in the instruction. The ACC register is allotted an address in the on-chip special function register bank. **B Register:** This register is used to store one of the operands for multiply and divide instructions. In other instructions, it may just be used as a scratch pad. This register is considered as a special function register. **Program Status Word (PSW):** This set of flags contains the status information and is considered as one of the special function registers. This bit-addressable register has the following format:  (13M)
4	**Write an 8051ALP to create a square wave of 66% duty cycle** **on bit 3 of port1.(Apr/May 2016) BTL 1(13M)** **Ans: Refer Notes** (13M)
5	**Explain the instruction set of 8051? (May 2015) BTL 5 (13M)**

```
        MOV   TMOD,#01      ;Timer 0, mode 1(16-bit mode)
HERE:   MOV   TL0,#0F2H     ;TL0 = F2H, the Low byte
        MOV   TH0,#0FFH     ;TH0 = FFH, the High byte
        CPL   P1.5          ;toggle P1.5
        ACALL DELAY
        SJMP  HERE          ;load TH, TL again
      -delay using Timer 0
DELAY:
        SETB  TR0           ;start Timer 0
AGAIN:  JNB   TF0,AGAIN     ;monitor Timer 0 flag until
                            ;it rolls over
        CLR   TR0           ;stop Timer 0
        CLR   TF0           ;clear Timer 0 flag
        RET
```

	Ans: Refer: Mohamed Ali Mazidi, Janice Gillispie Mazidi, Rolin McKinlay, "The 8051 Microcontroller and Embedded Systems: Using Assembly and C", Second Edition, Pearson Education, 2011.**PG.NO:533-536** These instructions perform arithmetic operations such as addition, subtraction, increment and decrement. • **Addition** — Any 8-bit number, or the contents of a register, or the contents of a memory location can be added to the contents of the accumulator and the result is stored in the accumulator • **Subtraction** — Any 8-bit number, or the contents of a register, or the contents of a memory location can be subtracted from the contents of the accumulator and the result is stored in the accumulator. • **Increment / Decrement** — The 8-bit contents of a register or a memory location can be incremented or decremented by one. Similarly, the 16- bit contents of a register pair can be incremented or decremented by 1. These increment and decrement operation differ from the addition and subtraction in an important way; i.e., they can be performed in one of the registers pr in a memory location. (13M)
6	**Explain the I/O structure of 8051 (8) (Nov 2013) (May 2014) BTL 5 (13M)** **Ans: Refer:**Mohamed Ali Mazidi, Janice Gillispie Mazidi, Rolin McKinlay, "The 8051 Microcontroller and Embedded Systems: Using Assembly and C", Second Edition, Pearson Education, 2011.**PG.NO:76-85** **Port 0 to 3 Latches and Drivers:** These four latches and driver pairs are allotted to each of the no-chip I/O ports. These latches have been allotted addresses in the special function register bank. Using the allotted addresses, the user can communicate with these ports. These are identified as P0, P1, P2 and P3.  **(13M)**
7	**List the special function registers of 8051 TMOD, SMOD and explain their functi (May 2015) BTL 5 (13M)** **Ans: Refer:**Mohamed Ali Mazidi, Janice Gillispie Mazidi, Rolin McKinlay, "The 8051 Microcontroller and Embedded Systems: Using Assembly and C", Second Edition, Pearson Education, 2011.**PG.NO:92-93.**

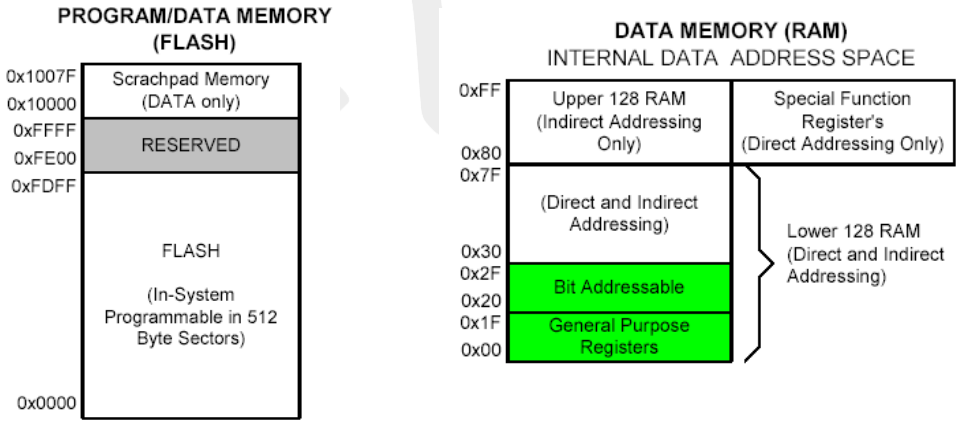
NAME	FUNCTION	INTERNAL RAM ADDRESS (HEX)
A	Accumulator	OEO
B	Arithmetic	0F0
DPH	Addressing external memory	83
DPL	Addressing external memory	82
IE	Interrupt enable control	0A8
IP	Interrupt priority	0B8
PO	Input/output port latch	80
Pl	Input/output port latch	90
P2	Input/output port latch	A0
P3	Input/output port latch	0B0
PC ON	Power control	87
PSW	Program status word	0D0
SCON	Serial port control	98
SBUF	Serial port data buffer	99
SP	Stack pointer	81
TMOD	Timer / counter mode control	89
TCON	Timer / counter control	88
TLO	Timer 0 low byte	8A
THO	Timer 0 low byte	8C
TL1	Timer 0 low byte	8B
TH1	Timer 1 high byte	8D

Special Function Registers

(13M)

8 **Explain the internal and external data memory organization of 8051. (10) (Nov2013) Explain in detail about the 8051 register bank and stack. APRIL/M 2019 BTL 5 (13M)**

Ans: Refer: Mohamed Ali Mazidi, Janice Gillispie Mazidi, Rolin McKinlay, "The 8051 Microcontroller and Embedded Systems: Using Assembly and C", Second Edition, Pearson Education, 2011.**PG.NO:367-374**



(13M)

9 **Describe how to program and interface an LCD to an 8051 using Assembly language programming. APRIL/MAY2019 BTL 5 (13M)**

```
MOV A,#38H // Use 2 lines and 5x7 matrix
ACALL CMND
MOV A,#0FH // LCD ON, cursor ON, cursor blinking ON
ACALL CMND
MOV A,#01H //Clear screen
ACALL CMND
MOV A,#06H //Increment cursor
ACALL CMND
MOV A,#82H //Cursor line one , position 2
ACALL CMND
MOV A,#3CH //Activate second line
```

```
ACALL CMND
MOV A,#49D
ACALL DISP
MOV A,#54D
ACALL DISP
MOV A,#88D
ACALL DISP
MOV A,#50D
ACALL DISP
MOV A,#32D
ACALL DISP
MOV A,#76D
ACALL DISP
MOV A,#67D
ACALL DISP
MOV A,#68D
ACALL DISP

MOV A,#0C1H //Jump to second line, position 1
ACALL CMND

MOV A,#67D
ACALL DISP
MOV A,#73D
ACALL DISP
MOV A,#82D
ACALL DISP
MOV A,#67D
ACALL DISP
MOV A,#85D
ACALL DISP
MOV A,#73D
ACALL DISP
MOV A,#84D
ACALL DISP
MOV A,#83D
ACALL DISP
MOV A,#84D
ACALL DISP
MOV A,#79D
ACALL DISP
MOV A,#68D
ACALL DISP
MOV A,#65D
ACALL DISP
MOV A,#89D
ACALL DISP

HERE: SJMP HERE

CMND: MOV P1,A
CLR P3.5
CLR P3.4
```

```
SETB P3.3
CLR P3.3
ACALL DELY
RET

DISP:MOV P1,A
SETB P3.5
CLR P3.4
SETB P3.3
CLR P3.3
ACALL DELY
RET

DELY: CLR P3.3
CLR P3.5
SETB P3.4
MOV P1,#0FFh
SETB P3.3
MOV A,P1
JB ACC.7,DELY

CLR P3.3
CLR P3.4
RET

END
```

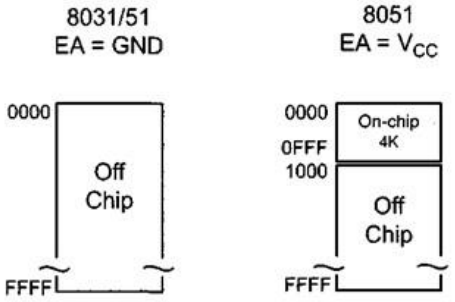
(13M)

10 **Briefly explain about the interfacing of 8051 with external data ROM. APRIL/MAY2019 BTL 5 (13M)**

When EA = 0, the EA pin is strapped to GND, and all program fetches are directed to external memory regardless of whether or not the 8751 has some on-chip ROM for program code. This external ROM can be as high as 64K bytes with address space of 0000 – FFFFH. In this case an 8751 (89C51) is the same as the 8031 system.

With the 8751 (89C5.1) system where EA = V_{cc}, the microcontroller fetches the program code of addresses 0000 – OFFFH from on-chip ROM since it has 4K bytes of on-chip program ROM and any fetches from addresses 1000H – FFFFH are direct ed to external ROM.

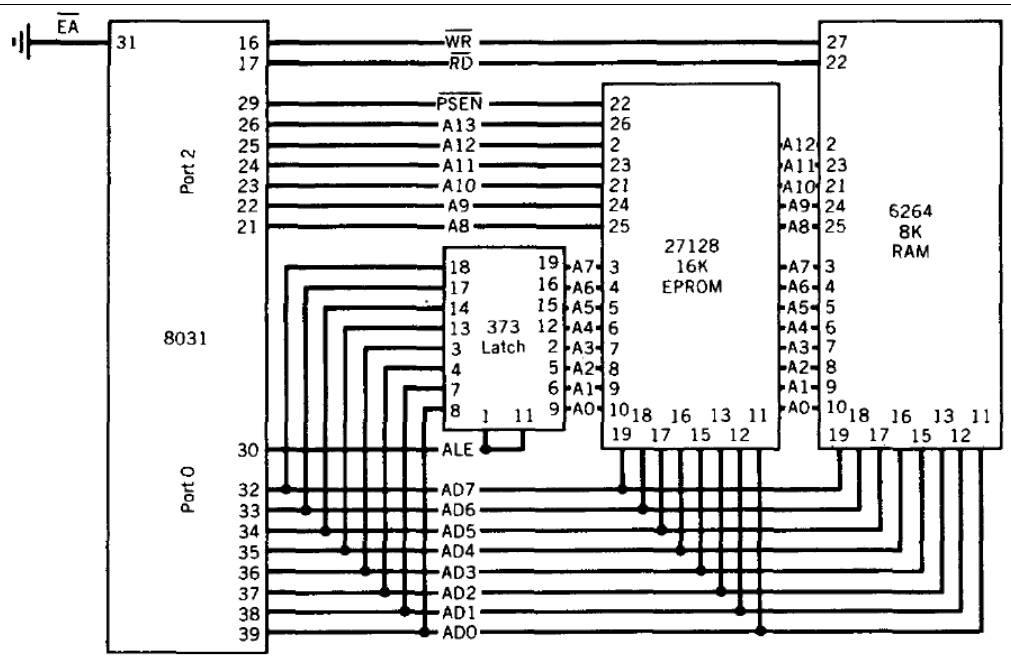
With the 8752 (89C52) system where EA = V_{cc}, the microcontroller fetches the program code of addresses 0000 – 1FFFH from on-chip ROM since it has 8K bytes of on-chip program ROM and any fetches from addresses 2000H – FFFFH are direct ed to external ROM.



(13M)

PART C

1 **Discuss the number of pin sets aside for addresses in each of the following memory chips(1) 16 K * 4 DRAM and (2)16K * 4 SRAM .APRIL/MAY2019 BTL 5 (15M)**



2 **With necessary diagrams explain how to interface LM 35 temperature sensor and then discuss the issues of signal condoning. APRIL/MAY2019 BTL 5 (15M)**

Important components in digital temperature measurement system are:

1. A sensor, sensor is nothing but a component or device whose physical parameters will change according to changes in atmospheric parameters or factors. For eg: Temperature Sensor, it might change its resistance, output voltage or dimension as there is some change in surrounding temperature. In this project we are using LM35, its output voltage increases by +10mV as there is 1° C rise in temperature.
2. A digital converter, as we all know the output of the sensor will be in form of analog voltage. This analog voltage can't be distinguished by the micro-controller or any other digital device. In order to understand changes in the output of sensor we need to convert it into digital form ie. Binary Data
3. A Interface which takes digital data as input processes it and produces signals or measured output which can be displayed or shown to operator on a screen like 16×2 LCD.

```
        MOV     P1,#0FFH
        SETB    EOC
        CLR     ALE
          CLR     START
        CLR     OE
         CLR     ADDR_C
          SETB    ADDR_B
          SETB    ADDR_A
           LCALL delay
            SETB    ALE
           LCALL delay
            SETB    START
    LCALL  delay
        CLR     ALE
        CLR     START
       JB      EOC,?C0001
        SETB    OE
       MOV     R7,P1
       MOV     A,#0DDH
          ADD     A,R7
          SETB    C
```

	SUBB A,#028H JC ?C0005 LCALL delay SETB RELAY
3	**Write an ALP for Multibyte addition BTL 2 (15M)**

UNIT V INTERFACING MICROCONTROLLER	
Programming 8051 Timers - Serial Port Programming - Interrupts Programming – LCD & Keyboard Interfacing - ADC, DAC & Sensor Interfacing - External Memory Interface- Stepper Motor and Waveform generation - Comparison of Microprocessor, Microcontroller, PIC and ARM processors	
PART A	
Q. No.	**Questions & Answers**
1	**What is the relation between RPM and steps per second in stepper motor interfacing? BTL 1** Steps per second= (rpm × steps per revolution)/60
2	**Write short notes on interrupts in 8051? BTL 1** Interrupts may be generated by internal chip operations or provided by external interrupts sources. Five interrupts are provided in 8051. Three of these interrupts are generated automatically by internal operations: **Timer flag 0, Timer flag 1, and the serial port interrupts (RI or TI)**. Two interrupts are triggered by external signals provided by the circuitry that is connected to the pins INT0 and INT1 (port pins P3.2 and P3.3).
3	**What is the purpose of Interrupt priority (IP) Control register in 8051? BTL 1** Register IP bits determine if any interrupt is to have a high or low priority. Bits set to 1 give the accompanying interrupt a high priority; a 0 assigns a low priority. If two interrupts with the same priority occur at the same time, then they have the following ranking: 1.IE0, 2.TF0, 3.IE1, 4.TF1,5.Serial = RI or TI.

4	**What is the purpose of counters in 8051 micro controller? BTL 1** The counters have been included on the chip to relieve the processor of timing and control chores. When the program wishes to count a certain number of internal pulses or external events, a number is placed in one of the counters. The number represents the following:**(Maximum count)-(Desired count) + 1.** The counter increments from the initial number to the maximum and then rolls over to zero on the final pulse.
5	**What is the basic difference between a timer and a counter? (May 2015) BTL 1** The only difference between a timer and a counter is the source of clock pulses to the counters. When used as a timer, the clock pulses are sourced from the oscillator through the divide-by-12d circuit. When used as a counter, pin T0 (P3.4) supplies pulses to counter 0, and pin T1(P3.5) to counter 1.
6	**Explain the operating mode 0 of 8051 serial port? BTL 2** • Mode 0 of 8051 serial port is shift register mode. • Serial data enters and exits through RXD pin. • Pin TXD is connected to the internal shift frequency pulse source. • 8-bits are transmitted and received. The baud rate is fixed at 1/12 of the crystal frequency.
7	**Define watch dog timer. BTL 1** • Watch dog timer is a dedicated timer to take care of system malfunction. It can be used to reset the controller during software malfunction, which is referred to as "Hanging". A watchdog timer contains a timer that expires after a certain interval unless it is restarted. It resets the microcontroller and starts the software over from the beginning if the software does not restart it periodically.
8	**What is the function of the TMOD register? BTL 1** TMOD (Timer mode) register is used to set the various timer operation modes. TMOD is dedicated solely to the two timers (T0 & T1) and can be considered to be two duplicate 4-bit registers, each of which controls the action of the timers.
9	**What is the difference between watch dog timer and ordinary timer? (Nov 2013) BTL 1** The watch dog timer is provided for the system to check itself and reset if it is not functioning properly. It is a16 bit-counter which is incremented every state time.
10	**List out the advantages of LCD over LED. BTL 1** • Declining prices of LED, • Ability to display numbers, characters and graphics • Incorporating a refreshing controller. Ease of programming for characters and graphics.
11	**What is the significance of BUSY flag in LCD interfacing? BTL 1** When D7 pin=1 and RS pin=0 the BUSY flag is set which means that LCD is busy taking care of internal operations and will not accept any new information. Therefore we have to check BUSY flag before writing data to LCD.
12	**How a pressed key is detected in keyboard interfacing? BTL 1** The keyboards are organized in a matrix of rows and columns. The microcontroller grounds all rows by providing zero to the output latch then reads the columns.
13	**What is the significance of WR and INTR pin in ADC chip? BTL 1** WR is an active low input and when it undergoes low to high transition the Start of

conversion signal is given. INTR is an active low output pin. It is normally high when the A to D conversion is finished. It goes low to signal EOC.

14 **Write an ALP to generate a saw tooth waveform. BTL 1**

```
    MOV A.#00H
    MOV P1,A
    BACK: INC A
SJMP BACK
```

15 **What is the significance of PSEN in memory interfacing? BTL 1**

PSEN (Program Store Enable) is an output signal for the 8051 microcontroller, which is connected to the OE pin of external ROM containing the program code. This is used when external ROM has to be accessed.

16 **What is SBUF? BTL 1**

SBUF stands for SERIAL BUFFER. SBUF is physically two registers. One is write only and is used to hold the data to be transmitted out of the 8051 via TXD. The other one is read only and holds the received data from external sources via RXD.

17 **What are the serial communication modes available in 8051? BTL 1**

Mode 0, Mode 1, Mode 2, Mode 3 is the serial communication modes available in 8051.

18 **What are the contents of SCON register? (May 2015) BTL 1**

SM0 - Serial port mode bit 0, **SM1** - Serial port mode bit 1, **SM2** - Serial port mode 2 bit multiprocessor communication enable bit; **REN** - Reception Enable bit. **TB8** - Transmitter bit 8. **RB8** - Receiver bit 8 or the 9th bit received in modes 2 and 3, **TI** - Transmit Interrupt flag & **RI** - Receive Interrupt flag.

7	6	5	4	3	2	1	0
SM0	SM1	SM2	REN	TB8	R	TI	RI

19 **What are the various baud rates possible in 8051 and how are they set? BTL 1**

Baud rate	TH1 (Dec)	TH1 (Hex)
9600	-3	FD
4800	-6	FA
2400	-12	F4
1200	-24	E8

20 **What are the various types of sensors that can be interfaced with 8051? (Apr/ May 2017) BTL 1**

1. Temperature Sensor, 2. IR Sensor, 3. Ultrasonic Sensor, 4. Touch Sensor, 5. Proximity Sensors, 6. Pressure Sensor, 7. Level Sensors, 8. Smoke and Gas Sensors.

21 **Define Baud rate of 8051. (Apr/May 2016) BTL 1**

In serial communication the data is rate known as the baud rate, which simply means the number of bits transmitted per second. In the serial port modes that allow variable baud rates, this baud rate is set by timer 1. The 8051 serial port is full duplex.

22 **What are the applications of stepper motor? BTL 1**

Industrial Machines – Stepper motors are used in automotive gauges and machine tooling automated production equipments. **Security** – new surveillance products for the security industry. **Medical** – Stepper motors are used inside medical scanners, samplers, and also found inside digital dental photography, fluid pumps, respirators and blood analysis machinery. **Consumer Electronics** Stepper motors in cameras for digital camera focus and zooming

23	**Compare polling and interrupt. (Apr/May 2016) BTL 1** Interrupt is a signal to the microprocessor from a device that requires attention. The microprocessor will respond by setting aside execution of its current task and deal with the interrupting device. When the interrupting device has been dealt with, the microprocessor continues with its original task as if it had never been interrupted. In Polling the processor continuously polls or tests every device in turn as to whether it requires attention (e.g. has data to be transferred). The polling is carried out by a polling program that shares processing time with the currently running task.
24	**What is the significance of TCON register? BTL 1** The Timer Control SFR is to configure, modify the way in which the 8051's two timers operate. This SFR controls whether each of the two timers is running or stopped and contains a flag to indicate that each timer has overflowed. Some non-timer related bits are located in the TCON SFR. These bits are used to configure the way in which the external interrupts are activated.
25	**List the 8051 interrupts with its priority (Apr/May 2017) BTL 1** Types of Interrupts in 8051 Microcontroller The 8051 microcontroller can recognize five different events that cause the main program to interrupt from the normal execution. These five sources of interrupts in 8051are: 1. Timer 0 overflow interrupt- TF0 2. Timer 1 overflow interrupt- TF1 3. External hardware interrupt-INT0 4. External hardware interrupt- INT1 Serial communication interrupt- RI/TI
26	**What are the different modes in which timer 2 can operate? BTL 1<u>APRIL/MAY 2019.</u>**
32	**When is an external memory access generated in 8051?<u>APRIL/MAY 2019.</u> BTL 1** **EA/VPP:** External access enable pin, if tied low, indicates that the 8051 can address external program memory. In other words, the 8051 can execute a program in external memory, only if EA is tied low. For execution of programs in internal memory, the EA must be tied high. This pin also receives 21 volts for programming of the on-chip EPROM.
	PART-B/Unit V
1	**Draw the block diagram of Intel 8051 timer/counter and explain its different modes of operations. (May 2015) (13M) BTL 5** **Ans: Refer:**Mohamed Ali Mazidi, Janice Gillispie Mazidi,Rolin McKinlay, "The 8051 Microcontroller and Embedded Systems: Using Assembly and C", Second Edition, Pearson Education, 2011.**PG.NO:202-221**

Timer Modes of Operation

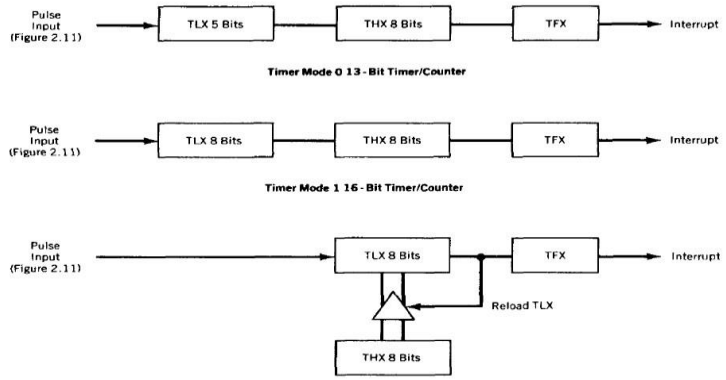
The timers may operate in any one of four modes that are determined by the mode bits, M1 and M0, in the TMOD register. Figure 2.12 shows the four timer modes.

Timer Mode 0

Setting timer X mode bits to 00b in the TMOD register results in using the THX register as an 8-bit counter and TLX as a 5-bit counter; the pulse input is divided by 32d in TL so that TH counts the original oscillator frequency reduced by a total 384d. As an example, the 6 megahertz oscillator frequency would result in a final frequency to TH of 15625 hertz. The timer flag is set whenever THX goes from FFh to 00h, or in .0164 seconds for a 6 megahertz crystal if THX starts at 00h.

Timer Mode 1

Mode 1 is similar to mode 0 except TLX is configured as a full 8-bit counter when the mode bits are set to 01b in TMOD. The timer flag would be set in .1311 seconds using a 6 megahertz crystal.



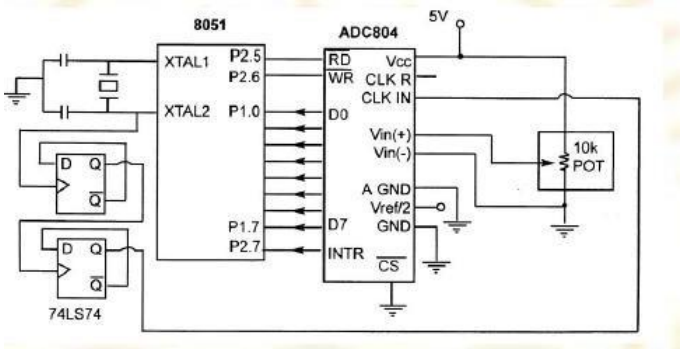
(13M)

2 **Explain how to interface ADC in detail.(16) (Dec 2013) (13M) BTL 5 (13M)**

Ans: Refer: Mohamed Ali Mazidi, Janice Gillispie Mazidi, Rolin McKinlay, "The 8051 Microcontroller and Embedded Systems: Using Assembly and C", Second Edition, Pearson Education, 2011.**PG.NO:322-327**

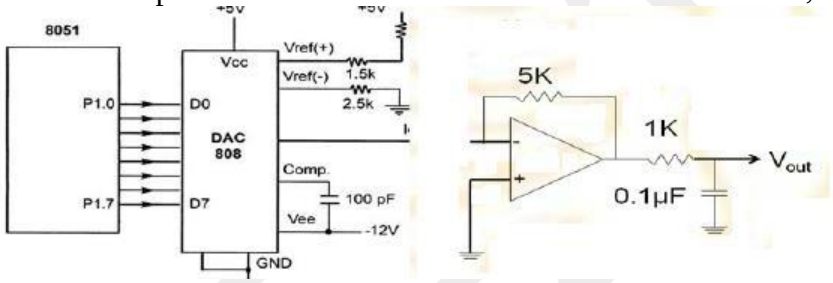
Analog-to-digital converter (ADC) interfacing: ADCs (analog-to-digital converters) are among the most widely used devices for data acquisition. A physical quantity, like temperature, pressure, humidity, and velocity, etc., is converted to electrical (voltage, current) signals using a device called a transducer, or sensor. We need an analog-to-digital converter to translate the analog signals to digital numbers, so microcontroller can read them.

ADC804 chip:ADC804 IC is an analog-to-digital converter. It works with +5 volts and has a resolution of 8 bits. Conversion time is another major factor in judging an ADC. Conversion time is defined as the time it takes the ADC to convert the analog input to a digital (binary) number. In ADC804 conversion time varies depending on the clocking signals applied to CLK R and CLK IN pins, but it cannot be faster than 110µs.



(13M)

4 **Explain how to interface DAC in detail.(13)<u>APRIL/MAY 2019</u> (13M) BTL 5**

	Ans: Refer: Mohamed Ali Mazidi, Janice Gillispie Mazidi, Rolin McKinlay, "The 8051 Microcontroller and Embedded Systems: Using Assembly and C", Second Edition, Pearson Education, 2011.**PG.NO:344-348** **Digital-to-Analog (DAC) converter:** The DAC is a device widely used to convert digital pulses to analog signals. In this section we will discuss the basics of interfacing a DAC to 8051.The two method of creating a DAC is binary weighted and R/2R ladder. The Binary Weighted DAC, which contains one resistor or current source for each bit of the DAC connected to a summing point. These precise voltages or currents sum to the correct output value. This is one of the fastest conversion methods but suffers from poor accuracy because of the high precision required for each individual voltage or current. Such high-precision resistors and current sources are expensive, so this type of converter is usually limited to 8-bit resolution or less. The R-2R ladder DAC, which is a binary weighted DAC that uses a repeating cascaded structure of resistor values R and 2R. This improves the precision due to the relative ease of producing equal valued matched resistors (or current sources). However, wide converters perform slowly due to increasingly large RC-constants for each added R-2R link. The first criterion for judging a DAC is its resolution, which is a function of the number of binary inputs. The common ones are 8, 10, and 12 bits. The number of data bit inputs decides the resolution of the DAC since the number of analog output levels is equal to 2^n, where n is the number of data bit inputs. **DAC0808:** The digital inputs are converter to current $I_{out,}$ and by connecting a resistor to the I_{out} pin, we can convert the result to voltage. The total current I_{out} is a function of the binary numbers at the D0-D7 inputs of the DAC0808 and the reference current I_{ref} , and is as follows:  **(13M)**
6	**With necessary hardware & software details explain how to interface LCD'S with 8051(16) (May 2015) (13M) BTL 5** **Ans: Refer:**Mohamed Ali Mazidi, Janice Gillispie Mazidi, Rolin McKinlay, "The 8051 Microcontroller and Embedded Systems: Using Assembly and C", Second Edition, Pearson Education, 2011.**PG.NO:300-306** LCD is finding widespread use replacing LEDs for the following reasons: 1. The declining prices of LCD 2. The ability to display numbers, characters, and graphics 3. Incorporation of a refreshing controller into the LCD, thereby relieving the CPU of the task of refreshing the LCD 4. Ease of programming for characters and graphics **Sending Data/ Commands to LCDs with Time Delay:** To send any of the commands to the LCD, make pin RS=0. For data, make RS=1. Then send a high-to-low pulse to the E pin to enable the internal latch of the LCD. This is shown in the code below. The interfacing diagram of LCD to 8051 is as shown in the figure.

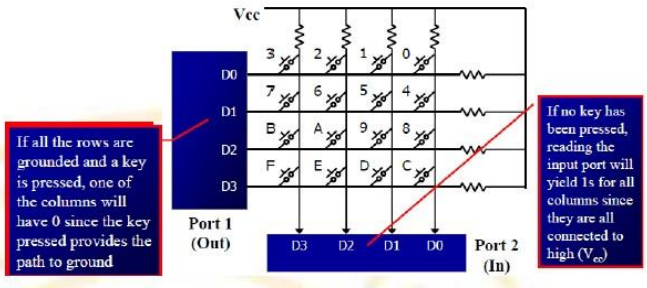
	<table><tr><th>Pin</th><th>Symbol</th><th>I/O</th><th>Description</th></tr><tr><td>1</td><td>V_{SS}</td><td>--</td><td>Ground</td></tr><tr><td>2</td><td>V_{CC}</td><td>--</td><td>+5V power supply</td></tr><tr><td>3</td><td>V_{EE}</td><td>--</td><td>Power supply to control contrast</td></tr><tr><td>4</td><td>RS</td><td>I</td><td>RS=0 to select command register, RS=1 to select data register</td></tr><tr><td>5</td><td>R/W</td><td>I</td><td>R/W=0 for write, R/W=1 for read</td></tr><tr><td>6</td><td>E</td><td>I/O</td><td>Enable</td></tr><tr><td>7</td><td>DB0</td><td>I/O</td><td>The 8-bit data bus</td></tr><tr><td>8</td><td>DB1</td><td>I/O</td><td>The 8-bit data bus</td></tr><tr><td>9</td><td>DB2</td><td>I/O</td><td>The 8-bit data bus</td></tr><tr><td>10</td><td>DB3</td><td>I/O</td><td>The 8-bit data bus</td></tr><tr><td>11</td><td>DB4</td><td>I/O</td><td>The 8-bit data bus</td></tr><tr><td>12</td><td>DB5</td><td>I/O</td><td>The 8-bit data bus</td></tr><tr><td>13</td><td>DB6</td><td>I/O</td><td>The 8-bit data bus</td></tr><tr><td>14</td><td>DB7</td><td>I/O</td><td>The 8-bit data bus</td></tr></table> **(13M)**
7	**Explain the different modes of operation of serial port in 8051, indicating various registers associated with it. (16) (Apr/May 2016) (13M) BTL 5** **Ans: Refer:**Mohamed Ali Mazidi, Janice Gillispie Mazidi, Rolin McKinlay, "The 8051 Microcontroller and Embedded Systems: Using Assembly and C", Second Edition, Pearson Education, 2011.**PG.NO:244-231** **Serial Port** • The serial buffer consists of two separate registers: **1.** Transmit buffer **2.** Receive buffer. • Writing data to the SFR sbuf sets this data in the serial output buffer and starts the transmission. Reading from the sbuf register reads data from the serial receive buffer. • The serial port can simultaneously transmit and receive data. • It can also buffer one byte at receive, which prevents the receive data from being lost • The serial port can operate in one of four modes. **a) Mode 0** • In this mode, the rxd0i pin receives serial data and the rxd0o pin transmits serial data. The txd0 pin outputs the shift clock. • Eight bits are transmitted with LSB first. • The baud rate is fixed at 1/12 of the crystal (clk input) frequency. **b) Mode 1** • In this mode, the rxd0i pin receives serial data and the txd0 pin transmits serial data. • No external shift clock is used, and the following 10 bits are transmitted: 1. One Start Bit (always 0) 2. Eight Data Bits (LSB first) 3. One Stop Bit (always 1) 4. On receive, **c) Mode 2** • The baud rate is fixed at 1/32 or 1/64 of the oscillator (clk input) frequency, and the following 11 bits are transmitted or received: 1. One Start Bit (0) 2. Eight Data Bits (LSB first) 3. One Programmable Ninth Bit 4. One Stop Bit (1) • The ninth bit can be used to control the parity of the serial interface.

d) Mode 3
The only difference between Mode 2 and Mode 3 is that the baud rate is variable in Mode 3.
(13M)

8 **How do you interface 8051 microcontroller with keyboard? Explain in detail. (13M) BTL 6**

Ans: Refer:Mohamed Ali Mazidi, Janice Gillispie Mazidi,Rolin McKinlay, "The 8051 Microcontroller and Embedded Systems: Using Assembly and C", Second Edition, Pearson Education, 2011.PG.NO:311-314

Keyboards are organized in a matrix of rows and columns. The CPU accesses both rows and columns through ports. Therefore, with two 8-bit ports, an 8 x 8 matrix of keys can be connected to a microprocessor. When a key is pressed, a row and a column make a contact. Otherwise, there is no connection between rows and columns. A 4x4 matrix connected to two ports. The rows are connected to an output port and the columns are connected to an input port.



(13M)

PART C

1 **Write an ALP to generate a triangular waveform and sine waveform**
Ans: Refer: Mohamed Ali Mazidi, Janice Gillispie Mazidi, Rolin McKinlay, "The 8051 Microcontroller and Embedded Systems: Using Assembly and C", Second Edition, Pearson Education, 2011.**PG.NO:331,344-346**

```
MOV A, #00H
INCR: MOV P1, A
INC A
CJNE A, #255, INCR
DECR: MOV P1, A
DEC A
CJNE A, #00, DECR
SJMP INCR
END
```

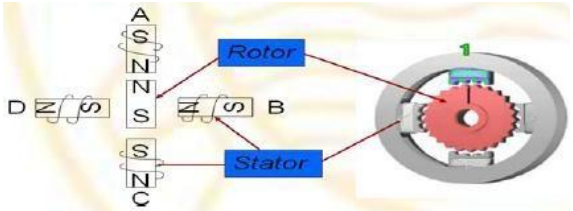
```
ORG 0000H
AGAIN: MOV DPTR, #SINETABLE
MOV R3, #COUNT
UP: CLR A
MOVC A, @A+DPTR
MOV P1, A
INC DPTR
DJNZ R3, UP
SJMP AGAIN
ORG 0300H
SINETABLE DB 128, 192, 238, 255, 238, 192, 128, 64, 17, 0, 17, 64, 128
END
```

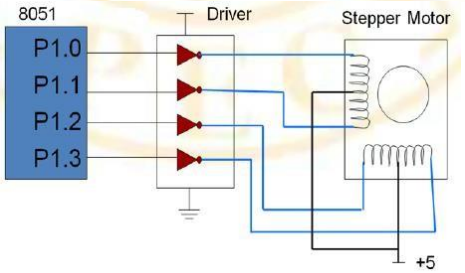
2 **Explain in detail the procedure to interface stepper motor with 8051. (May 2015)**

BTL 5

Ans: Refer: Mohamed Ali Mazidi, Janice Gillispie Mazidi,Rolin McKinlay, "The 8051 Microcontroller and Embedded Systems: Using Assembly and C", Second Edition, Pearson Education, 2011.**PG.NO:432-438**

Stepper motor is a widely used device that translates electrical pulses into mechanical movement. Stepper motor is used in applications such as; disk drives, dot matrix printer, robotics etc,. The construction of the motor is as shown in figure 1 below.





Program:

```
MOV A,#66H
BACK: MOV P1,A
RR A
ACALL DELAY
SJMP BACK
DELAY: MOV R1,#100
UP1: MOV R2,#50
UP: DJNZ R2,UP
DJNZ R1,UP1
RET
```

Program:

```
ORG 0000H
MOV A, #66H
MOV R0, #45
BACK: RR A
MOV P1, A
ACALL  DELAY
DJNZ R0, BACK
END
```

3 **Write a program for generation of unipolar square waveform of 1KHZ frequency using Timer 0 of 8051 in mode 0. Consider the system frequency as 12 MHZ. (Apr/May 2017) BTL 5**

Ans: Refer: Mohamed Ali Mazidi, Janice Gillispie Mazidi, Rolin McKinlay, "The 8051 Microcontroller and Embedded Systems: Using Assembly and C", Second Edition, Pearson Education, 2011.**PG.NO:203**

Mode-1 baud rate generation:

- Timer-1 is used to generate baud rate for mode-1 serial communication.
- Timer-1 is used in timer mode-2 as an auto-reload 8-bit timer.
- The data rate is generated by timer-1 using the following formula
- Where, SMOD is the 7th bit of PCON register f_{osc} is the crystal oscillator frequency
- f_{osc}/ (12 X [256- (TH1)]) is the timer overflow frequency in timer mode-2, which is the

	auto-reload mode. • If timer-1 is not run in mode-2, then the baud rate is, $f_{baud} = \frac{2^{SMOD}}{32} X \frac{fosc}{12 X [256-(TH1)]}$