EC8095 VLSI DESIGN L T P C

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OBJECTIVES:

- Study the fundamentals of CMOS circuits and its characteristics
- Learn the design and realization of combinational & sequential digital circuits.
- Architectural choices and performance tradeoffs involved in designing and realizing the circuits in CMOS technology are discussed
- Learn the different FPGA architectures and testability of VLSI circuits.

UNIT I INTRODUCTION TO MOS TRANSISTOR 9

MOS Transistor, CMOS logic, Inverter, Pass Transistor, Transmission gate, Layout Design Rules, Gate Layouts, Stick Diagrams, Long-Channel I-V Charters tics, C-V Charters tics, Non ideal I-V Effects, DC Transfer characteristics, RC Delay Model, Elmore Delay, Linear Delay Model, Logical effort, Parasitic Delay, Delay in Logic Gate, Scaling

UNIT II COMBINATIONAL MOS LOGIC CIRCUITS 9

Circuit Families: Static CMOS, Ratioed Circuits, Cascode Voltage Switch Logic, Dynamic Circuits, Pass Transistor Logic, Transmission Gates, Domino, Dual Rail Domino, CPL, DCVSPG, DPL, Circuit Pitfalls. Power: Dynamic Power, Static Power, Low Power Architecture.

UNIT III SEQUENTIAL CIRCUIT DESIGN 9

Static latches and Registers, Dynamic latches and Registers, Pulse Registers, Sense Amplifier Based Register, Pipelining, Schmitt Trigger, Monostable Sequential Circuits, Astable Sequential Circuits. Timing Issues : Timing Classification Of Digital System, Synchronous Design.

UNIT IV DESIGN OF ARITHMETIC BUILDING BLOCKS AND SUBSYSTEM 9

Arithmetic Building Blocks: Data Paths, Adders, Multipliers, Shifters, ALUs, power and speed tradeoffs, Case Study: Design as a tradeoff. Designing Memory and Array structures: Memory Architectures and Building Blocks, Memory Core, Memory Peripheral Circuitry.

UNIT V IMPLEMENTATION STRATEGIES AND TESTING 9

FPGA Building Block Architectures, FPGA Interconnect Routing Procedures. Design for Testability: Ad Hoc Testing, Scan Design, BIST, IDDQ Testing, Design for Manufacturability, Boundary Scan.

OUTCOMES:

- Realize the concepts of digital building blocks using MOS transistor.
- Design combinational MOS circuits and power strategies.
- Design and construct Sequential Circuits and Timing systems.
- Design arithmetic building blocks and memory subsystems.
- Apply and implement FPGA design flow and testing.

TEXT BOOKS:

1. Neil H.E. Weste, David Money Harris ―CMOS VLSI Design: A Circuits and Systems Perspective‖, 4th Edition, Pearson , 2017 (UNIT I,II,V)
2. Jan M. Rabaey ,Anantha Chandrakasan, Borivoje. Nikolic, ‖Digital Integrated Circuits:A Design perspective‖, Second Edition , Pearson , 2016.(UNIT III,IV)

REFERENCES:

1. M.J. Smith, ―Application Specific Integrated Circuits‖, Addisson Wesley, 1997
2. Sung-Mo kang, Yusuf leblebici, Chulwoo Kim ―CMOS Digital Integrated Circuits:Analysis & Design‖,4th edition McGraw Hill Education,2013
3. Wayne Wolf, ―Modern VLSI Design: System On Chip‖, Pearson Education, 2007
   R.Jacob Baker, Harry W.LI., David E.Boyee, ―CMOS Circuit Design, Layout and Simulation‖, Prentice Hall of India 2005.

UNIT I – MOS TRANSISTOR PRINCIPLE

MOS Transistor, CMOS logic, Inverter, Pass Transistor, Transmission gate, Layout Design Rules, Gate Layouts, Stick Diagrams, Long-Channel I-V Charters tics, C-V Charters tics, Non ideal I-V Effects, DC Transfer characteristics, RC Delay Model, Elmore Delay, Linear Delay Model, Logical effort, Parasitic Delay, Delay in Logic Gate, Scaling.

PART * A

Q.No.	Questions
1.	**What are the advantages CMOS technology? (April/May2019)** BTL2 • Low power consumption • High performance • Scalable threshold voltage • High noise margin • Low output drive current
2.	**Distinguish between nMOS and pMOS devices. (April/May2019)** BTL2

nMOS	pMOS
In nMOS, electrons are the majority carriers. When positive voltage is applied on gate, no. of electrons will increase. So conductivity of channel is increased	In pMOS, majority carriers are holes.
Switching speed is high, since the mobility of electron is high.	Switching speed is low, since the mobility of hole is low.
nMOS conducts at logic 1.	pMOS conducts at logic 0.

3.	**What is meant by body effect? (November/December 2019)** BTL1 V_t is not constant with respect to voltage difference between substrate and source of transistor. This is known as body effect. It is otherwise known as substrate-bias effect.
4.	**What is velocity saturation? (November/December 2019)** BTL1 The saturation current increases less than quadratically with increasing V_{gs} .Tis is caused by two effects velocity saturation and mobility degradation. At high electric fields strengths V_{ds}/L carrier velocity ceases to increase linearly with field strength. This is called velocity saturation and results in lower I_{ds} ,than expected at high V_{ds}.
5.	**Define inversion layer. (November/December 2018)** BTL1 When a higher positive potential greater than critical threshold is applied, it attracts more positive charge to the gate. These holes are repelled further and a small number of free electrons in the body are attracted to the region beneath the gate. This conductive layer of electrons in the p-type body is called inversion layer.
6.	**Define Noise Margin. (November/December 2018)** BTL1 Noise margin represents the amount of noise voltage on the input of a gate so that the output

	will not be corrupted. It is closely relating to the dc characteristics and it is also known as noise immunity. There are two parameters ▪ Low noise margin-NM_L ▪ High noise margin-NM_H
7.	**Give the expression for rise time and fall time in CMOS inverter circuit. (April/May2019)** BTL2 **Rise time:** The time needed for v_{out} to rise fron 0.1 v_{dd} to 0.9 v_{dd} is called rise time. $t_r=\ln(9)\ \tau_p$ $t_r=2.2\ \tau_p$ **Fall time:** The time needed for v_{out} to fall from 0.9 v_{dd} to 0.1 v_{dd} is called fall time. $t_f=\ln(9)\tau_n$ $t_f=2.2\ \tau_n$
8.	**What are the steps involved in manufacturing of IC? (April/May2019)** BTL2 The steps are ▪ Wafer preparation ▪ Epitaxial growth ▪ Oxidation ▪ Photo lithography ▪ Diffusion and Ion implantation ▪ Isolation ▪ Metallization
9.	**What is photo lithography?** BTL1 The patterning is achieved by a process called photolithography. In areas where the mask is absent, the implantation can occur, or dielectric or metal could be etched away.
10.	**What is CMOS technology?** BTL1 Complementary Metal Oxide Semiconductor (CMOS) in which both n-channel MOS and p-channel MOS are fabricated in the same IC.
11.	**What are the advantages of CMOS over NMOS technology?** BTL2 • In CMOS technology the aluminum gates of the transistors are replaced by poly silicon gate. • The main advantage of CMOS over NMOS is low power consumption. • In CMOS technology the device sizes can be easily scalable than NMOS.
12.	**What are the advantages of CMOS technology?**BTL2 • Low power consumption • High performance • Scalable threshold voltage • High noise margin • Low output drive current
13.	**What are the disadvantages of CMOS technology?** BTL2 • Low resistance to process deviations and temperature changes • Low switching speed at large values of capacitive loads
14.	**What is latch-up condition in CMOS circuits?** BTL4 Latch-up is a condition which creates a short circuit from positive supply voltage to ground. Latch-up is a condition occurs when:

	• The parasitic components give rise to the establishment of low resistance conducting path between VDD and GND • The product of the gains of the two transistors (n and p) in the feedback loop, b1x b2 is greater than one.
15.	**How to prevent latch up? (May/June 2016)**BTL4 Reduce the gain product b1x b2 Reduce the well and substrate resistances
16.	**What are the system approaches to prevent latch-up?** BTL2 By using proper grounding technique By using decoupling capacitors at the supply pins of the IC By placing a reversed-biased diode between each supply rail and the I/O pins By placing series resistance to limit the fault current to a safe value Carefully protect electrostatic protection devices associated with I/O pads with guard rings
17.	**What is design rule?** BTL1 Design rules are the communication link between the designer specifying requirements and the fabricator who materializes them. The design rule conform to a set of geometric constraints or rules specify the minimum allowable line widths for physical objects on-chip such as metal and poly silicon interconnects or diffusion area, minimum feature dimensions and minimum allowable separations between two layers.
18.	**What is stick diagram? (Nov/Dec 2014)** BTL1 Stick diagram are the key element of designing a circuit used to convey layer information through the use of a color code.
19.	**What is micron design rule?** BTL1 Micron rules specify the layout constraints such as minimum feature sizes and minimum allowable feature separations are stated in terms of absolute dimensions in micrometers.
20.	**What is lambda design rule? (April/May 2015)** BTL1 Lambda rules specify the layout constraints such as minimum feature sizes and minimum allowable feature separations are stated in terms of a single parameter λ and thus linear, proportional scaling of all geometrical constraints.
21.	**What is DRC?** BTL1 Design rule check program looks for design rule violations in the layout. It checks for minimum spacing and minimum size and ensures that combinations of layers form legal components.
22.	**What is LVS?** BTL1 The process of comparing two networks is called Layout Versus Schematic or netlist comparison or network isomorphism. This is used to prove that a layout is equivalent to a network extracted from schematic or HDL structural netlist.
23.	**Mention MOS transistor characteristics.** BTL4 Metal Oxide Semiconductor is a three terminal device having source, drain and gate. The resistance path between the drain and source is controlled by applying a voltage to the gate. The normal conduction characteristics of an MOS transistor can be categorized as Cut off region, Non-saturated region and saturated region.
24.	**What is threshold voltage?** BTL1 It is defined as the minimum voltage at which the device starts conduction (ie.,) turns on.
25.	**What are the different operating modes of MOS transistor?** BTL2 • Accumulation mode

	• Depletion mode • Inversion mode
26.	**What is accumulation mode?** BTL2 When the gate to source voltage (Vgs) is much less than the threshold voltage (Vt) then it is termed as the accumulation mode. There is no conduction between source and drain. The device is turned off.
27.	**What is depletion mode?** BTL2 When the gate to source voltage (Vgs) is increased greater than the threshold voltage (Vt) the electrons are attracted towards the gate while the holes are repelled causing a depletion region under the gate. This is called depletion mode.
28.	**What is inversion mode?** BTL2 When Vgs is raised above the Vt the electrons are attracted to the gate region. Under such a condition the surface of the underlying p-type silicon is said to be inverted to n-type and provides a condition paths between source and drain. The device is turned on. This is called inversion mode.
29.	**What are the three operating regions of MOS transistor?** BTL2 Cut-off region Non Saturated Region Saturated Region
30.	**What is cut-off region?** BTL1 The region where the current flow is essentially zero is called cut-off region. Ids=0, Vgs≤ Vt
31.	**What is saturated region?**BTL1 Channel is strongly inverted and the drain current flow is ideally independent of drain-source voltage is called saturated region. 0<Vgs-Vt<Vds
32.	**What is Non-saturated region?** BTL1 Weak inversion region where the drain current is dependent on the gate and the drain voltage is called non saturated region. 0<Vds<Vgs-Vt
33.	**What are the parameters that effect the magnitude of drain –source current Ids?** BTL2 • The distance between source and drain • The channel length • The threshold voltage • The thickness of the gate oxide layer • The dielectric constant of the gate insulator • The carrier mobility
34.	**What are the functional parameters of threshold equation?** BTL2 • Gate conductor material • Gate insulator material • Gate insulator thickness- channel doping • Impurities at the silicon- insulator interface • Voltage between the source and the substrate, Vsb
35.	**How the threshold voltage can be varied?** BTL3 • Threshold voltage may be varied by changing • The doping concentration (N_A)

	• The oxide capacitance (C_{ox}) • Surface state charge (Q_{fc})
36.	**What are the common methods used to adjust threshold voltage?**BTL2 • Change Q_{fc} by introducing a small doped region at the oxide/ substrate interface via ion implantation • Change C_{ox} by using a different insulating material for the gate
37.	**What is body effect? (Nov/Dec 2016)** BTL2 The threshold voltage V_t is not constant with respect to voltage difference between source and substrate is called body effect.
38.	**What are the second order effects of MOS transistor?** BTL1 • Threshold voltage- body effect • Sub threshold current • Channel length modulation • Mobility variation • Impact Ionization • Velocity Saturation
39.	**What is sub threshold current?** BTL2 The cut-off region described by Ids=0, Vgs≤Vt is also referred to as the sub threshold region, where Ids=0 increases exponentially with Vds and Vgs.
40.	**What is channel length modulation? (May/June 2016), (April / May 2017)**BTL2 The increase of the depletion layer width at the drain as the drain voltage is increased. This leads to a shorter channel length and an increased current is called Channel length modulation in a MOS.
41.	**What is mobility variation?** BTL2 The mobility is defined as the ratio of average carrier drift velocity to the electric field intensity.
42.	**What is drain punch through?** BTL2 When the drain is at a high enough voltage with respect to the source, the depletion layer around the drain and source regions merge into a single depletion region thus causing current to flow irrespective of the gate voltages. This is known as punch through effect.
43.	**What is impact ionization?** BTL2 When the length of the gate is reduced, the electric field at the drain of a transistor in saturation increases. For submicron gate lengths, the field can become so high that electron is imparted with enough energy to become "hot". The hot electrons impact the drain, dislodging holes that are swept towards the negatively charged substrate and appear as a substrate current. This effect is known as impact ionization.
44.	**What is SPICE?** BTL1 The acronym SPICE stands for Simulation Program with Integrated Circuit Emphasis is a general purpose circuit program that simulates electronic circuits.
45.	**Compare CMOS and Bipolar technologies. (Nov/Dec 2013)** BTL4

S.No.	CMOS Technology	Bipolar Technology
1.	Low static power dissipation	High power dissipation
2.	High input impedance	Low input impedance
3.	High packing density	Low packing density
4.	Low output drive current	High output drive current
5.	Drain and source are interchangeable	It is unidirectional
6.	High noise margin	Low voltage swing logic

46. **Define noise margin (May/June 2014). Illustrate how it can be obtained from the transfer characteristics of a CMOS Inverter. (Nov/Dec 2016)** BTL4

Noise margin is a parameter that allows us to determine the allowable noise voltage on the input of a gateso that the output will not be affected. The 2 common parameters are NMH & NML Where

NML = | VILmax – VOLmax| and NMH = | VOHmin – VIHmin|

VIHmin=minimum HIGH input voltage

VILmax = maximum LOW i/p voltage

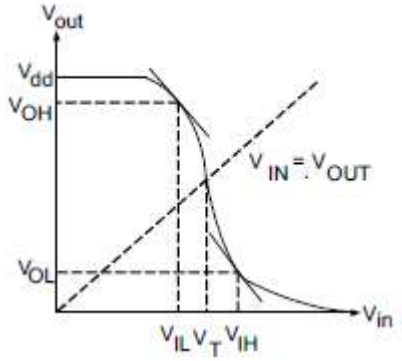
VOHmin = minimum HIGH o/p voltage

VOLmax = maximum LOW o/p voltage

47. **Discuss any two layout design rules? (May/June 2014)** BTL1

The two main approaches for describing layout rules are (i) micron rule (ii) μ- based rules. Micron design rules give a list of minimum feature sizes and spacing for all the masks required in a given process. λ- based design rules are based on a single parameter, 'λ' which characterizes the linear feature- the resolution of the complete wafer implementation process

48. **Draw the DC transfer characteristics of CMOS inverter? (Nov/Dec 2013), (April/May 2015)** BTL2



DC Transfer Characteristics

VIH: minimum HIGH input voltage, VIL: maximum LOW input voltage, VOH: minimum HIGH output voltage, VOL: maximum LOW output voltage. VT – Threshold voltage

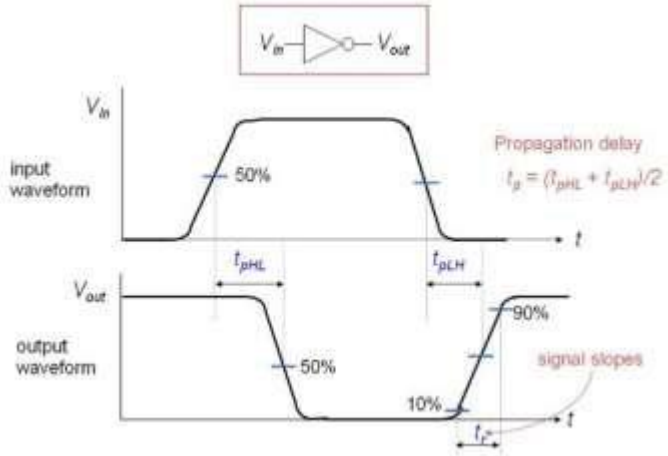
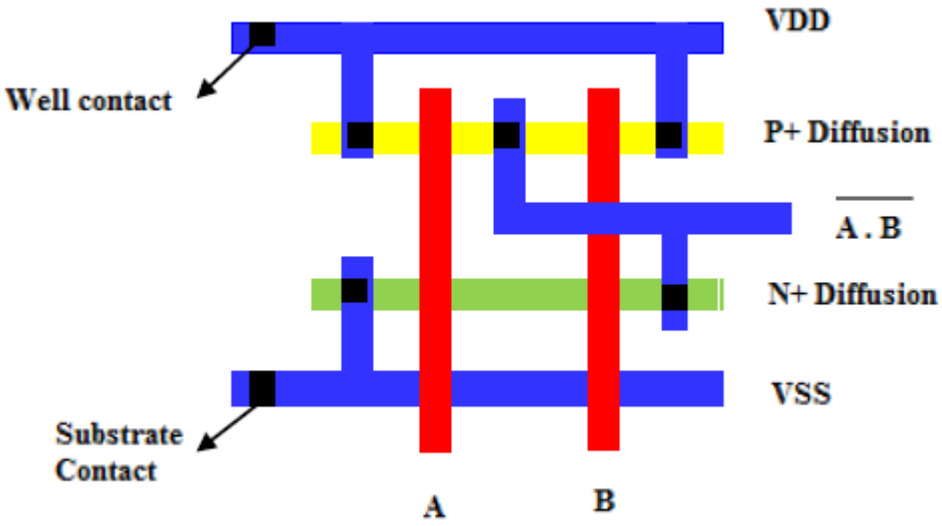
49. **Define scaling? (Nov/Dec 2013), (April/May 2015)** BTL2

Scaling of MOS transistor is concerned with systematic reduction of overall dimensions of the devices as allowed by the available technology, while preserving the geometric ratios found in the larger devices.

50. **What is propagation delay time tpd? / Define propagation delay of a CMOS inverter. (May/June 2014), (May/June 2016), (April / May 2017)** BTL2

It is the maximum time from the input crossing 50% to the output crossing 50%. It is also called as Maxtime.

High-to-Low propagation delay (tpHL): Time taken to fall from VOH to 50%.

	Low-to-High propagation delay (tpLH): Time taken to rise from 50% to VOL. Propagation Delay (tp): (tpHL + tpLH)/2.  **Input and Output waveform**
51.	**Give the types of scaling in CMOS technology. (Nov/Dec 2013)** BTL1 Transistor scaling, Interconnect scaling
52.	**Sketch the layout of a 2-input NAND gate. (NOV/DEC 2016)** BTL4  **Layout for 2 input NAND gate**
	PART * B
1.	**Explain the operation of a CMOS inverter clearly indicating the various regions of operation. (13M)** BTL4 **Answer: Page 1.81-1.86 –Dr.R.Uma** **CMOS Inverter**- Diagram-Circuit-Operation- input "0"- Output "1" (2M) **CMOS Inverter DC Characteristics**- Cut off- Ids=0, Vgs≤ Vt –Saturated-0<Vgs-Vt<Vds -Non-Saturated-0<Vds<Vgs-Vt (3M) **CMOS Inverter DC transfer and operating regions**- Diagram-Region A-Region B-Region C-Region D-Region E (8M)
2.	**Explain in detail about the ideal I-V characteristics and non-ideal I-V characteristics of NMOS and PMOS devices and derive its equation.(13M) (May/June 2013) (May/June 2016) (Nov/Dec 2016)** BTL4

	Answer: Page 1.14-1.18 and 1.56- 1.68- Dr.R.Uma **MOS DC Equations-** Cut-off mode- Non-saturated or Linear mode- Saturated mode (4M) **Non ideal IV characteristics**- **Threshold voltage**- minimum voltage at which the device starts conduction **Body effect**- The threshold voltage V_t is not constant with respect to voltage difference between source and substrate **Sub threshold conduction**- The cut-off region described by Ids=0, Vgs≤Vt - sub threshold region, where Ids=0 increases exponentially with Vds and Vgs. **Channel length modulation**- The increase of the depletion layer width at the drain as the drain voltage is increased. This leads to a shorter channel length and an increased current is called Channel length modulation in a MOS. **Mobility variation**- ratio of average carrier drifts velocity to the electric field intensity. **Drain punch through**- When the drain is at a high enough voltage with respect to the source, the depletion layer around the drain and source regions merge into a single depletion region thus causing current to flow irrespective of the gate voltages. **Impact ionization**- When the length of the gate is reduced, the electric field at the drain of a transistor in saturation increases. For submicron gate lengths, the field can become so high that electron is imparted with enough energy to become "hot". The hot electrons impact the drain, dislodging holes that are swept towards the negatively charged substrate and appear as a substrate current. Drain induced barrier lowering- Tunneling-Velocity saturation and mobility degradation-Junction leakage- Temperature dependence- Geometry Dependence (9M)
3.	**Explain the electrical properties of MOS transistor in detail (13M) (Nov/Dec 2013)** BTL3 **Answer: Page 1.11-1.68-Dr.R.uma** **Electrical Properties-** Threshold Voltage- Threshold voltage equations-Body effect (2M) **MOS DC Equations-** Cut off- Ids=0, Vgs≤ Vt –Saturated-0<Vgs-Vt<Vds -Non-Saturated-0<Vds<Vgs-Vt (2M) **Small Signal AC Characteristics**-Voltage gain-Figure of merit (2M) **MOS Capacitances**-Simple MOS capacitance model-Detailed MOS Capacitance model-MOS Device Capacitance (2M) **MOS Resistance**-Resistance of Non-rectangular Regions-Contact and via Resistance-Distributed RC effect-Wire length Design Guide- (1M) **Inductance- Non-Ideal I-V Characteristics of MOS**-Threshold voltage- Body effect- Sub threshold conduction- Channel length modulation- Mobility variation- Drain punch through-Impact ionization- Drain induced barrier lowering- Tunneling-Velocity saturation and mobility degradation- Junction leakage- Temperature dependence- Geometry Dependence (4M)
4.	**Briefly discuss about the CMOS process enhancements and layout design rules.(13M) (May/June 2014)** BTL2 **Answer: Page 1.99-1.105-Dr.R.Uma** **Micron Rules**-Features-CMOS layout Rules (6M) **Lambda Based Design Rules**-Features-Transistor design rules for nMOS, pMOS and CMOS (7M)
5.	**Discuss the CV characteristics and DC transfer characteristics of the CMOS. (13M) (May/June2014)** BTL4 **Answer: Page 1.31-1.38 &1.82-1.86-Dr.R.Uma** **MOS Capacitances**-Simple MOS capacitance model-Detailed MOS Capacitance model-MOS Device Capacitance (4M) **CMOS Inverter**- Diagram-Circuit-Operation (2M)

	CMOS Inverter DC Characteristics- Cut off- Ids=0, Vgs≤ Vt –Saturated-0<Vgs-Vt<Vds - Non-Saturated-0<Vds<Vgs-Vt (3M) **CMOS Inverter DC transfer and operating regions-** Diagram-Region A-Region B-Region C-Region D-Region E (4M)
6.	**Explain in detail about the scaling concept of CMOS chips.(13M) (May/June2013)** BTL4 **Answer: Page 1.80-1.81 -Dr.R.Uma** **Constant field Scaling-**Largest reduction in power delay product of single transistor (3M) **Constant voltage scaling-**Voltage compatibility with older circuits (3M) **Comparison of the effect of scaling on MOSFET devices-** Gate length- Gate width- Field-Oxide Thickness- Substrate doping- Gate capacitance-Oxide capacitance- Transit time- Transit frequency- Voltage- Current- Power- Power-delay (7M)
7.	**Describe the equation for source to drain current in the three regions of operation of a MOS transistor and draw the VI characteristics.(13M) (May/June 2016)** BTL4 **Answer: Page 1.80-1.81 -Dr.R.Uma** **MOS DC Equations-** Cut off mode-Non Saturated mode-Saturated mode (2M) **Cut off Mode:** Sub threshold Mode-Weak inversion current- Sub threshold leakage (3M) **Non-Saturated Mode**- Transit time- Electric Field- Trans-conductance- Device Trans-conductance (5M) **Saturated Mode**- Channel created (3M)
8.	**Explain in detail about the body effect and its effect in NMOS and PMOS devices. (13M) (May/June 2013) (May/June 2016)** BTL3 **Answer: Page 1.13-1.32 -Dr.R.Uma** Normal condition depletion layer width remains constant and charge carriers are pulled into the channel from the source (3M) Substrate bias increased- width of the channel substrate depletion layer increases results in increase in the density of the trapped carriers in the depletion layer (4M) nMOS enhancement mode Transistor (3M) nMOS depletion mode Transistor (3M)
9.	**Explain in detail about Device models.(13M) (May/June 2014)** BTL2 **Answer: Page 1.75-1.80 -Dr.R.Uma** **Device Models- Types of Models** **Level 1 model-** VTO, KP, LAMBDA, PHI and GAMMA (2M) **Level 2 Model-** Bulk Depletion charge must be calculated by taking into account its dependence on the channel voltage. (2M) **Level 3 Model-** Empirical equations instead of analytical models are both to improve the accuracy of the model (2M) **BSIM Model-** Berkeley short-channel IGFET model – based on small parameters- accuracy and efficiency (3M) **Diffusion Capacitance Model-**parasitic capacitance of the source and drain diffusion regions are simulated in SPICE with the simple pn-junction model. (4M)
	PART * C
1.	**Draw the layout diagram for NAND and NOR gate. (15M) (May/June 2017)**BTL5 **Answer: Page 1.108-1.109- Dr.R.Uma** Static CMOS Diagram for both NAND and NOR Gate (2+2)M Stick Diagram for both NAND and NOR Gate (2+2)M Layout Diagram based on Design Rules for both NAND and NOR Gate (2+2)M Coloring based on Design Rules for both NAND and NOR Gate (3M)

2.	**Explain the various steps involved in the P-well CMOS process with necessary diagrams. (15M) (Nov'2012)**BTL2 **Answer: Page 11-13 - N.Weste, K.Eshraghian** **Step 1 :** A thin layer of SiO_2 is deposited which will serve as the pad oxide. (1M) **Step 2 :** A thicker sacrificial silicon nitride layer is deposited by chemical vapour deposition (CVD). (1M) **Step 3 :** A plasma etching process is used to create trenches used for insulating the devices. (1M) **Step 4 :** The trenches are filled with SiO_2 which is called as the field oxide. (1M) **Step 5 :** To provide flat surface chemical mechanical planarization is performed and also sacrificial nitride and pad oxide is removed. (1M) **Step 6 :** The p-well mask is used to expose only the p-well areas, after this implant and annealing sequence is applied to adjust the well doping. This is followed by a second implant step to adjust the threshold voltage of the NMOS transistor. (1M) **Step 7 :** Implant step is performed to adjust the threshold voltage of PMOS transistor. (1M) **Step 8 :** A thin layer of gate oxide and polysilicon is chemically deposited and patterned with the help of polysilicon mask. (1M) **Step 9 :** Ion implantation to dope the source and drain regions of the PMOS (p^+) and NMOS (n^+) transistors, this will also form n^+ polysilicon gate and p^+ polysilicon gate for NMOS and PMOS transistors respectively. Hence this process is called as self aligned process. (1M) **Step 10 :** Then the oxide and nitride spacers are formed by chemical vapour deposition. (1M) **Step 11 :** In this step contact or via holes are etched, metal is deposited and patterned. After the deposition of last metal layer final passivation or overglass is deposited for protection.(1M) Diagram (2M)
3	**Explain the various steps involved in the n-well CMOS process with necessary diagrams. (15M) (Nov'2012)**BTL2 **Answer: Page 9-11- N.Weste, K.Eshraghian** **Step 1 :** A thin layer of SiO_2 is deposited which will serve as a the pad oxide. (1M) **Step 2 :** Deposition of a thicker sacrificial silicon nitride layer by chemical vapour deposition (CVD). (1M) **Step 3 :** A plasma etching process using the complementary of the active area mask to create trenches used for insulating the devices. (1M) **Step 4 :** The trenches are filled with SiO_2 which is called as the field oxide. (1M) **Step 5 :** To provide flat surface chemical mechanical planarization is performed and also sacrificial nitride is removed. (1M) **Step 6 :** The n-well mask is used to expose only the n-well areas, after this implant and annealing sequence is applied to adjust the well doping. This is followed by second implant step to adjust the threshold voltage of the PMOS transistor. (1M) **Step 7 :** Implant step is performed to adjust the threshold voltage of NMOS transistor. (1M) **Step 8 :** A thin layer of gate oxide and polysilicon is chemically deposited and patterned with the help of polysilicon mask. (1M) **Step 9 :** Ion implantation to dope the source and drain regions of the PMOS (p^+) and NMOS (n^+) transistors, this will also form n^+ polysilicon gate and p^+ polysilicon gate for NMOS and PMOS transistors respectively. Hence this process is called as self aligned process. (1M) **Step 10 :** Then the oxide or nitride spacers are formed by chemical vapour deposition. (1M) **Step 11 :** In this step contact or via holes are etched, metal is deposited and patterned. After the deposition of last metal layer final passivation or overglass is deposited for protection. (1M) Diagram (2M)

UNIT II – COMBINATIONAL LOGIC CIRCUITS

Circuit Families: Static CMOS, Ratioed Circuits, Cascode Voltage Switch Logic, Dynamic Circuits, Pass Transistor Logic, Transmission Gates, Domino, Dual Rail Domino, CPL, DCVSPG, DPL, Circuit Pitfalls. Power: Dynamic Power, Static Power, Low Power Architecture.

PART * A

Q.No.	Questions
1.	**What are the short falls of pass transistor logic? (Nov/Dec 2019)** BTL1 The short fall associated with PTL is threshold variation (or) threshold drop. An NMOS device is effective at passing a 0, but it is poor at pulling a node to VDD. When the pass-transistor pulls a node high, the output only charges to VDD − Vtn. The output voltage will also gets affected when the source-to-body voltage is present (body effect).
2.	**What is complementary pass transistor logic? (Nov/Dec 2019)** BTL 1 CPL is an alternative structure to eliminate threshold variation. The main concept behind CPL is the use of only an nMOS network for the implementation of logic functions. This results in low input capacitance and high speed operation. It consists of nMOS pass transistor logic network driven by two sets of complementary inputs and CMOS inverter used as buffers.
3.	**What are the two methods of restoration in PTL? (April/May 2019)** BTL1 1. The first method consist of single pMOS transistor connected in feedback path. (ie) cross coupled feedback. 2. The second restoration method utilizes pMOS gate connected to the output of inverter.
4.	**What is swing-restored pass transistor logic? (April/May 2019)** BTL1 It is an alternate configuration for PTL to eliminate threshold drop. In SRPL the output inverters are cross-coupled like a latch structure, which performs both swing restoration and output buffering.
5.	**What is the advantages of multiple threshold transistors. (Nov/Dec 2018)** BTL1 The threshold problem in pass transistors can be reduced using multiple threshold transistors. The primary goal of multiple threshold voltage circuits is to selectively scale the threshold voltages together with the supply voltage in order to enhance speed without increasing the subthreshold leakage current.
6.	**What are the limitations of multiple threshold transistor? (Nov/Dec 2018)** BTL1 The primary disadvantage of using multiple threshold transistors, has impact on the power consumption due to subthreshold current flowing through the pass transistors, even if *Vgs* is below *Vt*. The subthreshold leakage is not significant in the critical paths when the device is constantly switching but produces negative impact when the device is idle.
7.	**What is pass transistor logic? (April/May 2018)** BTL1 It is a MOS transistor, in which gate is driven by a control signal, the source (out), the drain of the transistor is called constant or variable voltage potential (in). When the control signal is high, input is passed to the output and when the control signal is low, the output is in high impedance (floating).
8.	**List the advantages of pass transistor logic. (April/May 2018)** BTL2 1. PTL circuits are often superior to standard CMOS circuits in terms of layout density, circuit delay and power consumption. 2. They do not have a path to GND and do not dissipate standby power (static power dissipation).
9.	**What is transmission gate?** BTL1 The circuit constructed with the parallel connection of PMOS and NMOS with shorted drain and

	source terminals. The gate terminal uses two select signals *s* and *s(bar)* then the transmission gate passes the signal from input to output. When *s* is low then the circuit enters into high impedance state.
10.	**Write the application of TG.** BTL2 • Multiplexing element or path selector • A latch element • An Analog switch • Act as a voltage controlled resistor connecting the input and output.
11.	**List the Important properties of static CMOS design.** BTL2 • At any instant of time, the output of the gate is directly connected to *VSS* or *VDD*. • All functions are composed of either AND'ed or OR'ed sub functions. The AND function is composed of NMOS transistors in series. The OR function is composed of NMOS transistors in parallel. • Contains a pull-up network (PUP) and pull down network (PDN). • PUP networks consist of PMOS transistors. • PDN networks consist of NMOS transistors. • Each network is the dual of the other network. • The output of the complementary gate is inverted.
12.	**What is Elmore delay model? (April / May 2017)** BTL2 This is an approximate method to find the delay of net or interconnects in terms of resistance and capacitance. General property of Elmore delay model network has • Single input node • All the capacitors are between a node and ground. • Network does not contain any resistive loops.
13.	**What are the basic methods to implement inverter in PTL?** BTL1 NMOS using load resistance in parallel. NMOS depletion mode transistor where the gate is connected to the source so it is always on. NMOS enhancement mode transistor where the gate terminal is always connected to VDD.
14.	**What are the short falls of pass transistor logic?** BTL4 The short fall associated with PTL is threshold variation (or) threshold drop. An NMOS device is effective at passing a 0, but it is poor at pulling a node to VDD. When the pass- transistor pulls a node high, the output only charges to VDD-Vtn. The output voltage will also gets affected when the source to body voltage is present (body effect).
15.	**What are the methods to reduce threshold drop problems in PTL?** BTL3 Incorresponding level restoration circuit Multiple – threshold transistors Transmission gate
16.	**What is complementary pass transistor logic?** BTL2 CPL is an alternative structure to eliminate threshold variation. The main concept behind CPL is the use of only an nMOS network for the implementation of logic functions. This results in low input capacitance and high speed operation. It consists of nMOS pass transistor logic network driven by two sets of complementary inputs and CMOS inverter used as buffers.
17.	**What are the two methods of restoration in PTL?** BTL1 The first method consists of single pMOS transistor connected in feedback path. (ie.,) cross coupled feedback.

	The second restoration method utilizes pMOS gate connected to the output of inverter.
18.	**What is swing-restored pass transistor logic?** BTL2 Swing restored pass transistor is an alternate configuration for PTL to eliminate threshold drop. In SRPTL the output inverters are cross coupled like a latch structure, which performs both swing restoration and output buffering.
19.	**What are the advantages of multiple threshold transistors?** BTL2 The threshold problem in pass transistors can be reduced using multiple threshold transistors. The primary goal of multiple threshold voltage circuits is to selectively scale the threshold voltages together with the supply voltage in order to enhance speed without increasing the subthreshold leakage current.
20.	**What are the limitations of multiple threshold transistors?** BTL2 The primary disadvantage of using multiple threshold transistors, has impact on the power consumption due to sub-threshold current flowing through the pass transistors, even if V_{gs} is below V_t. the sub-threshold leakage is not significant in the critical paths when the device is constantly switching but produces negative impact when the device is idle.
21.	**What is pass transistor logic?** BTL2 Pass transistor is a MOS transistor, in which gate is driven by a control signal, the source(out), the drain of the transistor is called constant or variable voltage potential (in). When the control signal is high, input is passed to the output and when the control signal is low, the output is in high impedance.
22.	**List the advantages of pass transistor logic.** BTL2 • PTL circuits are often superior to standard CMOS circuits in terms of layout density, circuit delay and power consumption. • They do not have a path to GND and do not dissipate standby power (state power dissipation)
23.	**What is transmission gate?** BTL2 The circuit constructed with the parallel connection of PMOS and NMOS with shorted drain and source terminals. The gate terminal uses two select signals s and sbar, when s is high then the transmission gate passes the signal from input to output. When s is low the the circuit enters into high impedance state.
24.	**List the application of transmission gate.** BTL1 • Multiplexing element or path selector circuit • A latch element • An analog switch • Act as a voltage controlled resistor connecting the input and output.
25.	**List the important properties of static CMOS design.** BTL1 • At any instant of time, the output of the gate is directly connected to VSS or VDD. • All functions are composed of either ANDed or ORed sub functions. The AND function is composed of NMOS transistors in series. The OR function is composed of NMOS transistors in parallel. • Contains a pull-up network (PUP) and Pull down network (PDN) • PUP network consists of PMOs transistors • PDN network consists of NMOS transistors • Each network is the dual of the other network. • The output of the complementary gate is inverted.
26.	**What are the advantages of static CMOS design?** BTL2 • Robust in construction • Good noise immunity

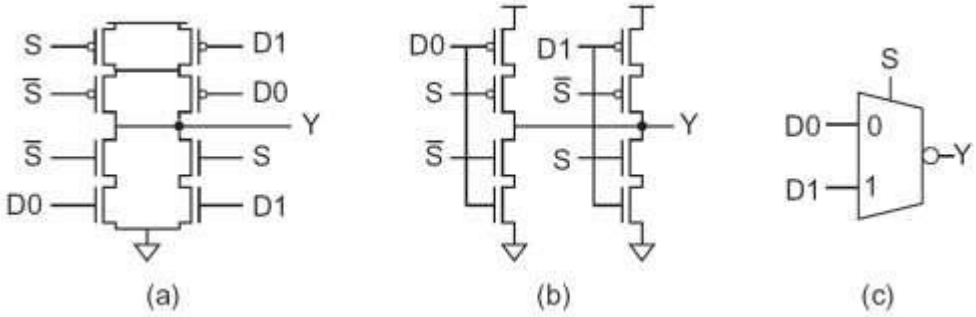
	• Static logic has no minimum clock rate, the clock can be pause indefinitely • Low power consumption • For low operating frequencies, CMOS static logic is used to obtain a relatively small die size.
27.	**List the limitations of static CMOS design.** BTL1 The main limitation of static circuits is slower speed as compared to dynamic circuits. The reasons are • Increased gate capacitance due to the presence of both PMOS and NMOS transistors • Output depends on the previous cycle inputs due to charges that may be present at internal inputs. • Multiple switching of the output within a cycle depending on the input switching pattern.
28.	**What are the classifications of CMOS circuit families?** BTL1 Static CMOS circuits Dynamic CMOS circuits Ratioed circuits Pass transistor circuits
29.	**What are the characteristics of static CMOS design?** BTL2 A static CMOS circuit is a combination of two networks- the pull up network (PUN) and the pull down network (PDN) in which at every point in time, each gate output is connected to either VDD or Vss via a low resistance path.
30.	**What is bubble pushing?** BTL2 Bubble pushing is a principle which is applied for static CMOS structure that is dual in nature that can be obtained using the duality principle of Demorgan's theorem. For example an OR gate is equivalent to a NAND gate with bubbles at its inputs and an AND gate is equivalent to a NOR gate with bubbles at its inputs.
31.	**What is AOI and OAI logic?** BTL2 AND-OR-INVERT (AOI) logic are two level compound (or complex) logic functions constructed from the combination of one or more AND gates followed by a NOR gate. Construction of AOI cells is particularly efficient using CMOS technology where the total number of transistor gates can be reduced compared to the same construction using NAND logic. In OR-AND-INVERT (OAI) logic where the OR gates precede an AND gate.
32.	**Define critical paths.** BTL2 Critical path is the longest path in the circuit which decides the most critical function and requires the attention to timing details.
33.	**What are the main levels that critical paths affect a system?** BTL1 • The architectural/ micro-architectural level • The logic level • The circuit level • The layout level
34.	**Define RC delay model.** BTL2 RC delay model is an analytical method used to estimate the delay of logic gates. The RC delay model treats transistors switches in series with resistors. Once the delay in the circuit is estimated, the circuit can be modified to operate faster.
35.	**What is intrinsic delay?** BTL2 The RC product of an MOS transistor is called intrinsic delay denoted as τ.
36.	**Define Elmore delay model.** BTL2 Elmore delay model is an analytical method used to estimate the RC delay in a network. Elmore delay model estimates the delay of a RC ladder as the sum over each node in the ladder of the

	resistance Rn-1 between that node and a supply multiplied by the capacitor on the nodes.
37.	**What are the general properties of Elmore delay model?** BTL2 General property of Elmore delay model network has • Single input node • All the capacitors are between a node and ground • Network does not contain any resistive loop
38.	**Define absolute delay.** BTL2 The absolute delay of a gate is the product of a unit-less delay of the gate (gate with as parasitics) and the delay unit that characterizes a given process.
39.	**Define linear delay.** BTL2 Linear delay is the sum of effort delay and parasitic delay.
40.	**Define effort delay.** BTL2 The delay that depends on the load and on properties of the logic gate driving the load. It is related in two terms: the logic effort of the logic gate and the electrical effort h characteristics the load.
41.	**Define electrical effort.** BTL2 Electrical effort is the ratio of output capacitances to the input capacitance of the gate. The electrical effort describes how the electrical environment of the logic gate affects the performance and how the size of the transistors in the gate determines its load-driving capability.
42.	**Define logical effort.** BTL2 Logical effort of a gate is defined as the ratio of the input capacitance of the gate to the input capacitance of an inverter that can deliver the same output current.
43.	**Define parasitic delay.** BTL2 The parasitic delay is the ratio of the parasitic capacitance to the input capacitance of the inverter, which is just $P_{inv.}$
44.	**Define path logical effort.** BTL2 The logical effort along a path compounds by multiplying the logical efforts of all the logic gates along the path.
45.	**Define path electrical effort.** BTL2 The electrical effort along a path through a network is simply the ratio of the capacitance with loads the last logic gate in the path to the input capacitance of the first gate in the path.
46.	**Define branching effort.** BTL2 When fan out occurs within a logic network, some of the variable drive current is directed along the path.
47.	**Define path effort.** BTL2 The path effort is the product of the stage efforts to the electrical effort of each stage.
48.	**Define path delay.** BTL2 The path delay is the sum of the delays of each of the stage of logic in the path. It can also be written as the sum of the path effort delay and path parasitic delay.
49.	**What are the ways to minimize delay in a chain of inverter?** BTL4 • Minimize the delay between input and output. • Increase the size of successive inverter. • Use minimum number of stages. • Minimize gate delay.
50.	**What are the sources of power dissipation? (April/May 2015)**BTL2 • Static power dissipation (due to leakage current when the circuit is idle) • Dynamic power dissipation (when the circuit is switching) and • Short-circuit power dissipation during switching of transistors.

51.	**What is static power dissipation?** BTL2 Power dissipation due to leakage current when the circuit is idle is called the static power dissipation. Static power due to • Sub-threshold conduction through OFF transistors. • Tunneling current through gate oxide. • Leakage through reverse biased diodes. • Contention current in ratioed circuits.
52.	**What is Dynamic power dissipation?** BTL2 Power dissipation due to circuit switching to charge and discharge the output load capacitance at a particular node at operating frequency is called dynamic power dissipation.
53.	**Define activity factor.** BTL2 The node transition activity factor, is a statistical parameter and is data rate dependent and defines the probability of the gate's output to make logic transition during one clock cycle.
54.	**What is short circuit power dissipation?** BTL2 During switching, both nMOS and pMOS transistors will conduct simultaneously and provide a direct path between VDD and the ground rail resulting in short circuit power dissipation.
55.	**What are the methods to reduce dynamic power dissipation? (Nov/Dec 2013)**BTL4 • Reducing the product of capacitance and its switching frequency. • Eliminate logic switching that is not necessary for computation. • Reduce activity factor. • Reduce supply voltage.
56.	**What are the methods to reduce static power dissipation?(Nov/Dec 2013)** BTL4 • By selecting multi threshold voltages on critical paths with low Vt transistors while leakage on other paths with high Vt transistors. • By using two operating modes, active and standby for each function blocks. • By adjusting the body bias that is adjusting fbb(forward body bias)in active mode to increase performance and RBB(reverse body bias)in standby mode to reduce leakage. • By using sleep transistor to isolate the supply from block to achieve significance leakage power savings.
57.	**What is SFPL?** BTL2 Source Follower Pull up logic is a variation on Pseudo nMOS whereby the load device is an N pull-down transistor and N source follower pull ups are used on the inputs.
58.	**What is CVSL?** BTL2 Cascade Voltage switch logic belongs to class of differential logic types. The network consists of a dual n block instead of a dual p-block and a pair of cross coupled pMOS transistors computes the logic function and its complement. CVSL can be roughly as fast as dynamic logic, it dissipates almost as little static power as static CMOS and is relatively robust against large structure.
59.	**What are the characteristics of CVSL?** BTL3 • CVSL is a differential type of logic circuit whereby both true and complement inputs are required. • N pull down trees are the dual of each other. • P pull up devices are cross coupled to latch output. • Both true and complement outputs are obtained.
60.	**What is dynamic CMOS logic?** BTL2 • Dynamic circuits rely on the temporary storage of signal values on the capacitance of high impedance nodes. • Requires only N+2 transistors.

	• Takes a sequence of precharge and conditional evaluation phases to realize logic functions.
61.	**What are the properties of Dynamic Logic?** BTL4 • Logic function is implemented by the pull down network only. • Full swing outputs(V_{OL}=GND and V_{OH}=VDD) • Non-ratioed • Faster switching speeds • Needs a precharge clock
62.	**What is ratioed circuits?** BTL2 Ratioed logic is an attempt to reduce the number of transistors required to implement a given logic function, often at the cost of reduced robustness and extra power dissipation.
63.	**What is pseudo-nMOS circuits?** BTL2 Circuit implemented with nMOS having grounded pMOS gate is called pseudo-nMOS circuits.
64.	**What are the advantages of pseudo-nMOS circuits?** BTL4 • Reduce number of transistors (N+1, versus 2N for CMOS) • The normal high output voltage (V_{OH}) for this gate is VDD since the pull-down stack are turned off when the output is pulled high. • Pseudo-nMOS gates offer improve speed factor.
65.	**What are the disadvantages of pseudo-nMOS circuits?** BTL2 • Reduced noise margin • Static power dissipation
66.	**What is precharge phase?** BTL2 The input to the next stage is charged up through the pMOS transistor when the clock is low, this phase of the clock is known as the precharge phase.
67.	**What is Evaluation phase?** BTL2 When the clock is high however, the pMOS is cutoff and the bottom nMOS is turned ON, thereby disconnecting the output node from VDD and providing a possible pull-down path to ground through the bottom nMOS transistor. This part of the clock cycle is known as the evaluation phase.
68.	**What is footed and unfooted dynamic circuits?** BTL2 • In unfooted dynamic circuits uses one pMOS through which a clk is connected which give rise to contention problem when both pMOS and nMOS ON precharge phase. • In footed dynamic circuits uses a single pMOS precharge transistor and one nMOS evaluation transistors to avoid contention problem.
69.	**What are the disadvantages of dynamic CMOS logic?** BTL2 • A fundamental difficulty with dynamic circuits is a loss of noise immunity and a serious timing restriction on the inputs of the gate. • Violate monotonicity during evaluation phase.
70.	**What is CMOS domino logic?** BTL2 A static CMOS inverter placed between dynamic gates which eliminate the monotonicity problem in dynamic circuits are called CMOS domino logic.
71.	**What are the properties of domino logic?** BTL2 • Only non-inverting logic can be implemented. • Very high speed having tp_{HL}=0 • Eliminates the monotonicity problem.
72.	**What is dual rail domino logic?** BTL2 Circuit is said to be dual-rail domino if each logical variable is represented by two wires, one that goes high if the signal is false, with this encoding, an input variable going true can cause an output

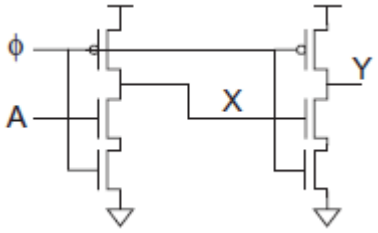
	variable to go true or false.
73.	**What are glitches?** BTL2 A node exhibiting multiple transitions in a single clock cycle before settling to the correct logic level is called glitches or dynamic hazards. The occurrence of glitching in a circuit is mainly due to mismatch in the path lengths in the network.
74.	**What are the non-ideal effects dynamic logic?** BTL2 Although a dynamic logic circuit has less propagation delay than its static counterpart, there are many non-ideal effects that severely affect the signal integrity of a dynamic logic circuit. Signal integrity means how well a signal can transfer from one place to another along a signal path, which may be a long chain, a wire, or both. There are many factors that can affect the signal integrity. These include leakage current, charge injection, clock (capacitive) feedthrough, backgate coupling, charge loss effect, charge-sharing effect, and power supply noise. These effects are often named as non ideal effects of dynamic logic.
75.	**What is charge sharing?** BTL2 Charge sharing is a serious problem in dynamic logic, which occurs when two or more capacitors at different potentials are tied together. A node of a network must never be driven simultaneously by signals of opposite polarity, as this can leave the node in an erroneous or undefined state. One must beware of sneak paths which allow charge to leak. Charge sharing can occur when dynamic gates drive pass transistors.
76.	**How to reduce charge sharing effects?** BTL4 The common approaches to reduce the charge sharing effect are as follows. • Increasing the capacitance of the critical node • Using the charge keeper • Precharging the internal nodes.
77.	**Define Transistor Sizing problem. (May/ June 2014)** BTL2 Transistor sizing, an important problem in designing high performance circuits, has traditionally been formally defined as Minimize *Area* or *Power,*Subject to *Delay* .
78.	**Why is the transmission of logic 1 degraded as it passes through a nMOS pass transistor.(Nov/Dec 2016)** BTL4 When S = 1 (Vdd) , and Vin = 1 the pass transistor begins to conduct and charges the CL towards Vdd. Initially Vin is at ahigher potential than Vout, the current flows through the device. As voltage ot the load approaches Vdd – Vtn, the n- device begins to turn – off. Vtn is the n- transistor body effected threshold .. Thus the transmission of logic 1 is degraded.
79.	**List the various power losses in CMOS circuits? (May/June 2013)** BTL1 Static power loss, Dynamic power loss
80.	**What is a pass transistor? What are its advantages? (Nov 2013)** BTL2 Pass transistor is similar to a buffer. Advantages of pass transistor are • Occupies less space, because any logical operation can be realized with lesser number of MOS transistors • No direct path between VDD and Gnd. So, amount of power dissipation is lesser understand by condition.
81.	**Draw the structure of 2:1 CMOS MUX.(Nov/Dec 2013)** BTL5



2:1 CMOS MUX

82. **Why single phase dynamic logic structure cannot be cascaded? Justify. (May/June 2016)** BTL4

Single phase dynamic logic structure cannot be cascaded. Because, a fundamental difficulty with dynamic circuits is the monotonicity requirement. While a dynamic gate is in evaluation, the inputs must be monotonically rising. Unfortunately, the output of a dynamic gate begins HIGH and monotonically falls LOW during evaluation. This monotonically falling output X is not a suitable input to a second dynamic gate expecting monotonically rising signals, as shown in Figure. Dynamic gates sharing the same clock cannot be directly connected. This problem is often overcome with domino logic.



Cascaded dynamic Logic

83. **State the advantages of transmission gates. (April / May 2017)** BTL2

The NMOS only pass transistor can only pass strong zero at the output where as it cannot pass strong one. Similarly, PMOS only pass transistor can only pass strong one at the output where as it cannot pass strong zero. The disadvantages of both PMOS and NMOS pass transistor are overcome by transmission gate where it is able to produce both strong one and strong zero at the output.

84. **List out the sources of static and dynamic power consumption.(Nov/Dec 2016)** BTL1

CMOS devices have very low static power consumption, which is the result of leakage current.
But, when switching at a high frequency, dynamic power consumption can contribute significantly to overall power consumption. Charging and discharging a capacitive output load further increases this dynamic power consumption.

PART * B

1. **What is meant by power dissipation? Derive an expression for static power dissipation and dynamic power dissipation with necessary diagram and expressions. (13M) (Nov/Dec 2013) / (May/June 2014) (Nov/Dec 2016)** BTL5

Answer: Page 2.140-2.145 –Dr.R.Uma

Static Power Dissipation-Sub-threshold conduction through OFF transistors- Tunneling current through gate oxide- Leakage through reverse biased diodes- Contention current in ratioed circuits (4M)

Dynamic Power Dissipation-Capacitances-Supply Voltage-Clock Frequency (4M)

Short Circuit power Dissipation-Total Power Dissipation (5)M

2.	**Explain the resistive and capacitive delay estimation of CMOS inverter circuit. (13M) (May/June2013)** BTL4 **Answer: Page 2.62-2.66- Dr.R.Uma** **RC Delay Models-**ON Resistance (3M) **Calculation of fall Delay** (4M) **Calculation of Rise Delay** (4M) **Propagation Delay** (2M)
3.	**Find the rising and falling propagation delays of an AND- OR- INVERT gate using the Elmore delay model. (13M) (Nov/Dec 2013)** BTL5 **Answer: Page 2.72-2.74- Dr.R.Uma** **Elmore Delay model Network-** Single input node- All the capacitors are between a node and ground- Network does not contain any resistive loops (4M) **Calculation of Rise Time** (3M) **Calculation of Fall Time** (3M) **Propagation Delay** (3M)
4.	**Design NAND gate using pseudo –nMOS Logic. (13M) (Nov/Dec 2013)** BTL6 **Answer: Page 2.107-2.111- Dr.R.Uma** **Static CMOS gates-** slower- input must drive both nMOS and pMOS transistors (2M) Ratioed Inverter Transfer Function (3M) NAND gate using Pseudo nMOS logic- Grounded PUN-PDN as static CMOS (5M) Diagram (3M)
5.	**Explain the domino and dual rail domino logic families with neat diagrams. (13M) (Nov/Dec 2012)** BTL2 **Answer: Page 2.125-2.127- Dr.R.Uma** **CMOS Domino Logic-** Dynamic CMOS logic configuration- drawback- Monotonicity Problem(5M) **Properties of Domino Logic** - Only non-inverting logic- Very high speed- Disadvantages (3M) **Dual Rail Domino Logic**- Diagram- AND/NAND structure- XOR/XNOR structure (5M)
6	**What is transmission gate? Explain the use of transmission gate.(13M). (April / May 2017)** BTL2 **Answer: Page 2.39-2.48- Dr.R.Uma** **Transmission Gate-** Basic Structure-DC Characteristics of Transmission Gate (6M) **Application of Transmission Gate**- Path Selector-Implementation of D-Latch using Transmission Gate (7M)
	PART * C
1	**Implement the following function using CMOS** **f(A,B,C) = A'BC + AB'C + ABC' (8M)** **y= (A+B)(C+D) (7M) (Nov/Dec 2013,2019)** BTL6 **Answer: Page 2.57-2.62- Dr.R.Uma** 1) The PUN will consist of multiple inputs, therefore requires a circuit with multiple PMOS transistors. (2M) 2) The PDN will consist of multiple inputs, therefore requires a circuit with multiple NMOS transistors. (2M) **PDN Design Synthesis** (4M) If the PDN is conducting, then the output will be low- Boolean expression for the complemented output Y. In turn, the PDN can only be conducting if one or more of the NMOS devices are conducting and

	NMOS devices will be conducting (i.e.,triode mode) when the inputs are high **PUN Design Synthesis** (4M) If the PUN is conducting, then the output will be high- Boolean expression for the un-complemented output Y. In turn, the PUN can only be conducting if one or more of the PMOS devices are conducting and PMOS devices will be conducting (i.e., triode mode) when the inputs are low **Diagram** (3M)
2	**(i) Draw the static CMOS logic circuit for the following expression** **(a) Y=(A.B.C.D)' (b) Y=(D(A+BC))'** **(ii) Discuss in detail about the characteristics of transmission gate.(15M) (May/June 2016,2018)** BTL6 **Answer: Page 2.57-2.62- Dr.R.Uma** 1)The PUN will consist of multiple inputs, therefore requires a circuit with multiple PMOS transistors. (2M) 2)The PDN will consist of multiple inputs, therefore requires a circuit with multiple NMOS transistors. (2M) **PDN Design Synthesis** (3M) 1.If the PDN is conducting, then the output will be low. Thus, we must find a Boolean expression for the complemented output Y. In turn, the PDN can only be conducting if one or more of the NMOS devices are conducting and NMOS devices will be conducting (i.e.,triode mode) when the inputs are high **PUN Design Synthesis** (3M) 1.If the PUN is conducting, then the output will be high. Thus, we must find a Boolean expression for the un-complemented output Y. In turn, the PUN can only be conducting if one or more of the PMOS devices are conducting and PMOS devices will be conducting (i.e., triode mode) when the inputs are low **Diagram** (1M) **Characteristics of Transmission Gate** (4M)
3	**Write short notes on i) Ratioed circuits ii) Dynamic CMOS circuits. (15M) (Nov/Dec 2016,2019)** BTL2 **Answer: Page 2.107-2.124- Dr.R.Uma** **Ratioed Circuits-** Pseudo nMOS circuits- Ratied Inverter transfer function- Logical effort of Pseudo nMOS gates-Advantages of Psudo nMOS gates- Disadvantages of Pseudo-nMOS logic- Source Follower Pull up Logic-Cascade Voltage Switch Logic (CVSL)- Characteristics (8M) **Dynamic CMOS Logic**- Properties of Dynamic Logic-Applications of Dynamic Logic (7M)
4.	**(i) Design D-flip-flop using transmission gate.** **(ii) Implement a 2- bit non-inverting dynamic shift register using pass transistor logic.(15M) (Nov/Dec 2013)** BTL6 **Answer: Page 2.39-2.48- Dr.R.Uma** **Transmission Gate-** Basic Structure-DC Characteristics of Transmission Gate (4M) **Application of Transmission Gate**- Path Selector-Implementation of D-Latch using Transmission Gate (3M) D-Flip flop Diagram (3M) 2 bit shift register using pass transistor logic Diagram (3M)

UNIT III – SEQUENTIAL LOGIC CIRCUITS

Static latches and Registers, Dynamic latches and Registers, Pulse Registers, Sense Amplifier Based Register, Pipelining, Schmitt Trigger, Monostable Sequential Circuits, Astable Sequential Circuits. Timing Issues : Timing Classification Of Digital System, Synchronous Design.

PART * A

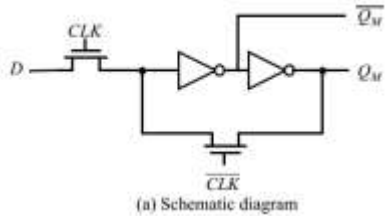
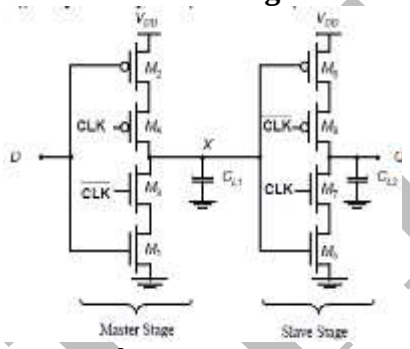
Q.No.	Questions
1.	**Define combinational and sequential circuit. (Nov/Dec 2019)** BTL2 A combinational circuit consists of logic gates whose outputs at any time are determined from the present combination of inputs. On the other hand a sequential circuit in which the output depends on previous as well as current inputs. They can be used to keep a record of what value a variable (input, output or intermediate) had in the past as well as store the current value of a variable for later use.
2.	**What is sequencing element? (Nov/Dec 2019)** BTL2 Sequential circuits are designed with flip flops or latches, which are sometimes called memory elements that hold data called tokens. They can be used to keep record of what value (previous token) a variable had in the past as well as store the current (current token) value of a variable. They are used to 'sequence' data, i.e. make a large amount of data appear in a pre-determined bit by bit sequence, they are called as sequencing elements.
3.	**What is sequencing overload? (April/May 2019)** BTL2 Sequencing elements delay tokens that arrive too early, preventing them from catching up with the previous tokens. Unfortunately, they inevitably add some delay to tokens that are already critical, decreasing the performance of the system. This extra delay is called sequencing overload.
4.	**Define static and dynamic sequencing element. (April/May 2019)** BTL2 Sequencing element can be static or dynamic. A sequencing element with static storage employs some sort of feedback to retain its output value indefinitely. A sequencing element with dynamic storage generally maintains its value as charge on a capacitor that will leak away if not refreshed for a long period of time.
5.	**Define metastability. (Nov/Dec 2018)** BTL2 Flip flop is a device that is susceptible to metastability. It has two well defined stable states, traditionally designated 0 and 1, but under certain conditions it can hover between them for longer than a clock cycle. This condition is known as metastability. Such a metastable "state" is considered a failure mode of the logic design and timing constraints. The most common cause of metastability is violating the flip-flop's setup and hold times. During the time from the setup to the hold time, the input of the flip-flop should remain in a stable logic state; a change in the input in that time will have a probability of setting the flip-flop to a metastable state.
6.	**Define metastable condition. (Nov/Dec 2018)** BTL2 In reality, when a flip flop samples as input that is changing during its aperture, the output Q may momentarily take on a voltage between 0 and VDD that is in the forbidden zone. This is called a metastable state. Eventually, the flip flop will resolve the output to a stable state of either 0 or 1.
7.	**Define resolution time. (April/May 2018)** BTL2 If the input to a bistable device such as a flip flop changes during the aperture time, the output may take on a metastable value for some time before resolving to a stable 0 or 1. The amount of time required to resolve is unbounded, because for any finite time, t the probability that the flip flop is still metastable is nonzero. However, this probability drops off exponentially as t increases. Therefore, if we wait long enough, much longer than t_{pcq}, we can expect with exceedingly high probability that the flip-flop will reach a valid logic level.

8.	**Define logic propagation delay (t_{pd}).** BTL2 Upper bound on interval between valid inputs and valid outputs.
9.	**Define logic contamination delay (t_{cd}).** BTL2 Lower bound on interval between invalid inputs and invalid outputs.
10.	**Define Latch/flip flop clock to Q propagation delay (t_{pcq}). (April/May 2018)** BTL2 t_{PLH}: 50% triggering edge point of the clock pulse to 50% transition of the output from low to high. t_{PHL}: 50% triggering edge point of the clock pulse to the high to low transition of the output.
11.	**Define Latch/flip flop clock to Q contamination delay (t_{ccq}).** BTL2 Output signal start to change after its input change and settles to the final value within a propagation delay.
12.	**Define Latch D to Q propagation delay (t_{pdq}).** BTL2 Assuming that the setup and hold times are met, the data at the D input is copied to the Q output after a worse case propagation delay.
13.	**Define Latch D to Q contamination delay (t_{cdq}).** BTL2 This delay ensures that the D input of the sequential elements is held enough after the clock edge and is not modified too soon by the new value of data coming in.
14.	**Define Latch/flip flop setup time (t_{setup}).** BTL2 The time before the clock edge that the D input has to be stable is called setup time.
15.	**Define Latch/flip flop hold time (t_{hold}).** BTL2 The time after the clock edge that the D input has remained stable is called hold time.
16.	**List the methods of sequencing static circuits.** BTL1 The three most widely used methods of sequencing static circuits • Flip flops • 2-Phase transparent latches • Pulsed latches
17.	**Define setup time failure or max-delay failure.** BTL2 If the combinational logic delay is too long, the receiving element will miss its setup time and sample the wrong value. This is called a setup time failure or max-delay failure.
18.	**What is called pulsed latch?** BTL2 The latch that has short clock to Q delay and a long hold time is called pulsed latch or single phase level triggered latch.
19.	**Define min-delay failure.** BTL2 In a sequential circuit if the hold time is large and the contamination delay is small, data can incorrectly propagate through two successive elements on one clock edge, corrupting the state of the system. This is called a race condition, hold time failure or min-delay failure.
20.	**Define time borrowing.** BTL2 The principle advantage of transparent latches over flip flops is the softer edges that allow data to propagate through the latch as soon as it arrives instead of waiting for a clock edge. Therefore, logic does not have to be divided exactly into half cycles. Some logic blocks can be longer while others are shorter, and the latch based system will tend to operate the average of the delays; a flip flop based system would operate at the longest delay. This ability of slow logic in one half-cycle to use time normally allocated to faster logic in another half-cycle is called time borrowing or cycle stealing.
21.	**What is clock skew?** BTL2 In reality clocks have some uncertainty in their arrival times that can cut into the time available for useful computation is called clock skew.

22.	**What are the different types of pipelines?** BTL2 Depending on the data forwarded fashion namely, when applied to new data, pipelining techniques can be classified into synchronous pipelining, asynchronous pipelining and wave pipelining. In the synchronous pipelining, new data are applied to a computational circuit in intervals determined by the maximum propagation delay of the computational circuit. In the asynchronous pipelining, new data are applied to a computational circuit in intervals determined by the average propagation delay of the computational circuit. In the wave pipelining, new data can be applied to a computational circuit in intervals determined by the difference between maximum and minimum propagation delays of the computational circuit.
23.	**What are the approaches used in the design of asynchronous pipeline systems?** BTL2 An asynchronous design is based on the concept of modular functional blocks intercommunicating using some communication protocols. The general approaches of asynchronous pipeline systems are one way control and two way control. The one way control is also called a strobe control and the two way control scheme is generally referred to as a handshaking control.
24.	**What are the important constraints for any synchronous or asynchronous pipeline systems to work properly?** BTL3 Regardless of which scheme is used and whether the underlying system is synchronous or asynchronous, any sequential logic must satisfy two constraints in order to work properly. These include physical timing constraint and event logical order. Physical timing constraint guarantees that each function unit and memory element has enough time to complete the specific operations. For example, in order to guarantee that the output data from a memory element is valid, the physical timing constraints, such as setup time and hold time of latches or flip flops, must always be satisfied. Event logical order means that events in the system must occur in the logical order set by the designer. In a synchronous system, this is commonly achieved by using a clock to provide a time base for determining what and when to happen. In an asynchronous system, some other schemes, such as handshaking signals or protocols are deployed.
25.	**What is resettable latch?** BTL2 Resettable latches and flip-flops employs a control input called reset signal to enter a known initial state on startup.
26.	**What are the two types of reset?** BTL1 The two types of reset are (i) Synchronous (ii) Asynchronous In synchronous reset, the flip-flop changes with synchronous control inputs and clock signal. In asynchronous reset, the output is independent of the synchronous input and the clock input.
27.	**What is klass semi-dynamic flip-flop?** BTL2 Klass semi-dynamic flip-flop is a single output positive edge-triggered flip flop. It is domino-style front end allows for efficient embedded combinational logic and reduces the load on the data network.
28.	**What is differential flip-flop?** BTL2 Differential flip-flops accept true and complementary inputs and produce true and complementary outputs. This can be built from a clocked sense amplifier so they can rapidly respond to small differential input voltages.
29.	**What is TSPC?** BTL2 The True Single Phase Clock latch is constructed by merging CMOS Domino and CMOS NORA logic. Conventional latches require both true and complementary clock signals. Normally the complementary signals are generated with an inverter in the latch cell.
30.	**What is regenerative circuit?** BTL2 The fundamental elements used in clock generation are called regenerative circuits which can be catalogued as astable and monostable. The astable circuit act as oscillators and can be used in on-chip

	clock generation. The monostable circuit act as one-shot circuit and can be used in pulse generation. Another important regenerative circuit is the Schmitt trigger having the property of showing hysteresis in its dc characteristics.
31.	**What are the important properties of Schmitt trigger circuit?** BTL3 A Schmitt trigger circuit has two important properties: • It responds to a slowly changing input waveform with a fast transition time at the output. • Its switching threshold is variable and depends upon the direction of the transition (low to high or high to low). The main advantage of this property is the Schmitt trigger is turn a noisy or slowly varying input signal into a clean digital output signal.
32.	**Define monostable circuit.** BTL2 A monostable circuit is a circuit that generates a pulse of predetermined width every time the quiescent circuit is triggered by a pulse or transition event. It is called monostable because it has only one stable state. A trigger event, which is either a signal transition or a pulse, causes the circuit to go temporarily into another quasi-stable state. This means that it eventually returns to its original state after a time period determined by the circuit parameters. This circuit, also called a one shot, is useful in generating pulses of a known length.
33.	**Define astable circuit.** BTL2 An astable circuit has no stable states. The output oscillates back and forth between two quasi-stable states, with a period determined by the circuit topology and parameters. One of the main applications of oscillators is the on-chip generation of clock signals. The ring oscillator is a simple example of an astable circuit.
34.	**How memory classified based on the type of data access?** BTL4 The semiconductor memory can be classified in terms of the type of data access and the capability of information retention. According to the type of data access, semiconductor memory can be subdivided into serial access, content addressable, and random access. The data in serial-access memory can only be accessed in a predetermined order and mainly contains shift registers and queues. Content addressable memory (CAM) is a device capable of parallel search; namely, it behaves likes a lookup table in which all entries can be searched in parallel. Random access memory (RAM) is a memory device where any word can be accessed at random at any time. The random access memory can be further categorized into read/write memory and read-only memory.
35.	**How memory classified based on the capability of information retention?** BTL4 According to the capability of information retention, semiconductor memory may also be cast into volatile and non-volatile memories. The volatile memory, such as static RAM and dynamic RAM, will lose its information once the power supply is interrupted while the non-volatile memory, such as the ROM family, ferroelectric RAM (FRAM) and magneto resistance RAM (MRAM), still retain their information even when the power supply is removed.
36.	**What is serial access memory?** BTL2 Serial access memory mainly contains shift registers and queues. The former can be further subdivided into serial in parallel out and parallel in serial in, while the later contains first in first out and first in last out. A FIFO is generally called a queue or a buffer and a FILO is referred to as a stack.
37.	**What is RAM?** BTL2 Random Access memory (RAM) is a memory device in which any word can be accessed at random in a constant time. The random access memory can be classified into read/write memory and read only memory. Read/write memory can be further subdivided into two types: static RAMs (SRAMs) and Dynamic RAMs(DRAMs). SRAM is mainly used as the main memory for those computer systems needing a small memory capacity, and as the cache memory for large computer systems, such as desktop computers and servers. DRAM is used as the main memory for those computer

	systems requiring a large memory capacity.
38.	**What is SRAM?** BTL2 The SRAM cell consists of a bi stable device accompanied with two access transistors and thus stores its information in a form of circuit state.
39.	**What is DRAM?** BTL2 The DRAM cell comprises an access transistor and a capacitor, and retains information in the form of charge. Due to the leakage current of the access transistor, the capacitor in a DRAM cell is gradually losing its charge and eventually its information. To remedy this, a DRAM cell must be read and rewritten periodically, even when the cell is not accessed. This process is known as refresh.
40.	**What is CAM?** BTL2 Content Addressable memory (CAM) is a device with the capability of parallel search; namely, it behaves like a lookup table in which all entries can be searched in parallel. A CAM cell is fundamentally a SRAM cell to store information with the addition of some extra circuits to facilitate the operation of parallel interrogation and indicate the result. CAM proceeds the reverse operation of SRAM; namely, it receives as an input data and output a matched address when the data matches one in the CAM.
41.	**What is sequential search in CAM?** BTL2 One approach is to search the table in a way such that the keyboard is compared against tags in the table one by one. Such an approach is called a sequential search and is the usual way performed in most computer systems using a software algorithm as the unsorted data are stored in the table. Of course, this sequential search can also be realized with a RAM and a finite machine without the use of a more powerful microprocessor.
42.	**What is parallel search in CAM?** BTL2 The other approach is to compare the keyword with all tags in the table at the same time. This results in a concept and technique known as a parallel search. To facilitate such a capability, a special hardware is needed. The table is composed of two parts: a tag part and a data item part. Both parts are a kind of memory array. However, the tag part needs the capability of a parallel search whereas the data item part does not. The data item part simply outputs a data item whenever its associated tag matches the keyword. A memory array capable of a parallel search is referred to as a content-addressable memory (CAM). It is also called associative memory because the data associated with a tag is referenced whenever the stored tag matches the interrogating keyword.
43.	**What is synchronizers? (May/June 2014, May/June 2013)**BTL2 A synchronizer is a circuit that accepts an input that can change at arbitrary times and produces an output aligned to the synchronizer's clock. Because the input can change during the synchronizer's aperture, the synchronizer has a non zero probability of producing a metastable output.
44.	**What is arbiter?** BTL2 An arbiter is a circuit designed to determine which of several signals arrive first. Arbiters are used in asynchronous circuits to order computational activities for shared resources to prevent concurrent incorrect operations.
45.	**What is Arbitration?** BTL2 A closely related problem for synchronization is arbitration. Arbitration is necessary when two or more modules would like exclusive access to a shared resource.
46.	**What is synchronous interconnect?** BTL2 A synchronous signal is one that has the exactly same frequency as a local clock, and maintains fixed phase offset to that clock.
47.	**What is mesochronous interconnect?** BTL2 A mesochronous signal is one that has the exactly same frequency as a local clock, and maintains unknown phase offset to that clock.

48.	**What is plesiochronous interconnect?** BTL2 A plesiochronous signal is one that has almost the same frequency as a local clock, resulting in slowly drifting phase offset to that clock.
49.	**What is asynchronous interconnect?** BTL2 An asynchronous interconnect is one that can have transition arbitrarily at any time and it is independent of local clock.
50.	**What is clock jitter?** BTL2 Clock jitter refers to the temporal variation of the clock period at a given point- that is, the clock period can reduce or expand on a cycle-by-cycle basis. It is strictly a temporal uncertainity measure and is often specified at a given point on the chip.
51.	**How is a latch different from a register? (Nov/Dec 2014)** BTL4 A latch is level sensitive circuit that passes the D input to the Q output when the clock signal is high. Contrary to level sensitive latches, edge triggered registers only sample the input on a clock transition, that is $0 \rightarrow 1$ for a positive edge triggered register and $1 \rightarrow 0$ for a negative edge triggered register.
52.	**Draw the switch level schematic of multiplexer based nMOS latch using nMOS only pass transistors for multiplexers. (May/June 2016)** BTL3  (a) Schematic diagram
53.	**What is clocked CMOS Register? (May/June 2016)** BTL2 **Clocked CMOS Register**  Figure shows an ingenious positive edge-triggered register, based on a master-slave concept insensitive to clock overlap. This circuit is called the C2MOS (Clocked CMOS) register. The overall circuit operates as a positive edge-triggered master-slave register very similar to the transmission gate based register. However, there is an important difference: A C2MOS register with CLKCLK' clocking is insensitive to overlap, as long as the rise and fall times of the clock edges are sufficiently small.
54.	**What is meant by pipelining? (April / May 2017)** BTL2 Pipelining allows different functional units of a system to run concurrently. Pipelining cannot decrease the processing time required for a single task. The advantage of pipelining is that it increases the throughput of the system when processing a stream of tasks.
55.	**Compare and contrast synchronous design and asynchronous design. (April / May 2017)** BTL4

	<table><tr><th>Asynchronous design</th><th>Synchronous Design</th></tr><tr><td>Clock pulse is given to first circuit and the output of first circuit acts as a clock to the next and so on.</td><td>Simultaneous clock pulse is given to all the circuits.</td></tr><tr><td>Slow as compare to synchronous circuits</td><td>Fast as compare to asynchronous circuits.</td></tr><tr><td>Circuit is simple as compared to synchronous circuits.</td><td>Additional combinational circuit is required for its designing. This circuit becomes complex.</td></tr></table>
	PART * B
1.	**Elaborate on the differences between latches and registers with necessary timing diagrams. (13M) (Nov/Dec2016)** BTL4 **Answer: Page 3.5-3.16 –Dr.R.Uma** **Sequencing Methods**- Flip Flops-Transparent Latches- Pulsed Latches (3M) **Max Delay Constraints**- Flip flop max delay constraint- Two phase latch max delay constraint- Pulsed latch max delay constraint (4M) **Min Delay constraints**- Flip flop latch min delay constraint- Two phase latch min delay constraint- Pulsed latch min delay constraint (4M) **Diagram** (2M)
2.	**Explain the NORA-CMOS logic style for pipelined structures. Is this topology race free? (13M) (Nov/Dec 2016)** BTL2 **Answer: Page 3.31-3.34-Dr.R.Uma** C^2MOS based pipelined circuit is race free as long as all the logic function between the latches are non-inverting. Each module consists of a block of combinational logic that can be a mixture of static and dynamic logic followed by a C^2MOS latch. (6M) **Operation modes for NORA logic modules** (7M)
3.	**Explain the methodology of sequential circuit design of latches and flip-flops. (13M) (May/June 2014)** BTL2 **Answer: Page 3.16-3.25-Dr.R.Uma** Conventional Latches and Flip flops (2M) Pulsed Latches (2M) Resettable Latches and Flip flops (1M) Enabled Latches and Flip flops (2M) Klass Semi-dynamic Flip flop (2M) Differential Flip flops (2M) True Single Phase Clock (TSPC) Latches and Flip flops (2M)
4.	**Discuss the operation of a pipeline concepts used in sequential circuits. (13M) (May/June 2013) (Apr/May 2016) (NOV/DEC 2017)** BTL4 **Answer: Page 3.25-3.34-Dr.R.Uma** Pipelining Concept (2M) Types of Pipelining (1M) Synchronous pipelining (2M) Asynchronous Pipelining (2M) Wave pipelining (2M) Latch versus Register based pipeline (2M) NORA-CMOS –A logic style for Pipelined Structures (2M)

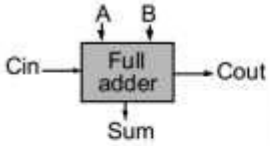
5.	**Explain the operation of master slave based edge triggered register. (13M) (May/June 2016)** BTL2 **Answer: Page 3.17-3.18- Dr.R.Uma** Master Latch- First one followed by Slave Latch-Nine inverters- Four Transmission Gates-Master latch is Transparent (7M) Slave Latch – Enabled – Update its state-negative edge triggered flip flop. (6M)
6.	**Explain the memory architecture. (13M)** BTL2 **Answer: Page 3.38-3.59-Dr.R.Uma** Memory- Memory Classification-Types of Data Access-Memory Organization-Memory Access Timing (3M) Static Random Access Memory- Basic RAM Cell Structures- Low Power SRAM Cells- Operation of SRAM- Dynamic Random Access Memory-Cell Structure- 3T RAM Cell-1T RAM Cell- Structures of DRAM Memory Array (6M) Read Only Memory- Active Programming ROM (2M) Content Addressable Memory- Operation of CAM- CAM Organization-CAM Cells (2M)
7.	**Explain the memory control circuits. (13M)** BTL2 **Answer: Page 3.44-3.59-Dr.R.Uma** Read Cycle Analysis- Write Cycle Analysis- Word Line RC Time Constant (3+3)M Read Only Memory- Active Programming ROM (4M) Content Addressable Memory- Operation of CAM- CAM Organization-CAM Cells (3M)
8.	**Explain synchronizers in detail. (13M)** BTL2 **Answer: Page 3.59-3.63-Dr.R.Uma** Synchronizer- A simple Synchronizer-Basic structure-Common synchronizer mistakes (7M) Arbiter- Mutually Exclusive element- arbitration (6M)
	PART * C
1.	**(Explain the timing basics and clock distribution techniques in synchronous design in detail. (15M) (Nov/Dec 2017,2019)** BTL4 **Answer: Page 3.34-3.38-Dr.R.Uma** The Schmitt Circuit-Circuit- Timing diagram (4M) CMOS implementation of Schmitt Trigger (3M) Monostable Sequential circuits- Astable Circuits (3+3M)
2	**(a)Explain the operation of true single phase clocked register** **(b)Draw and explain the operation of conventional, pulsed and resettable latches. (15M) (April/May 2017,2019)**BTL2 **Answer: Page 3.16-3.24- Dr.R.Uma** Conventional Latches and Flip flops- Pulsed Latches – Resettable Latches and Flip flop (8M) True Single Phase Clocked Register- Non- overlapping Clocks- single external Clock- Timing Diagram- TSPC Dynamic D flip flops (7M)
3	**Explain the concept of timing issue and pipelining. (15M) (April/May 2017,2018)**BTL4 **Answer: Page 3.25-3.30-Dr.R.Uma** Pipelining- Types of Pipelines-Synchronous Pipelining (10M) Asynchronous Pipelining-Source initiated transfer- Ready- Data valid- Data acceptance- Acknowledge- Destination initiated Transfer- Request- Data Valid- Data Acceptance- Acknowledge (5M) Wave Pipelining (5M)

UNIT IV – DESIGN OF ARITHMETIC BUILDING BLOCKS AND SUBSYSTEM

Arithmetic Building Blocks: Data Paths, Adders, Multipliers, Shifters, ALUs, power and speed tradeoffs, Case Study: Design as a tradeoff. Designing Memory and Array structures: Memory Architectures and Building Blocks, Memory Core, Memory Peripheral Circuitry.

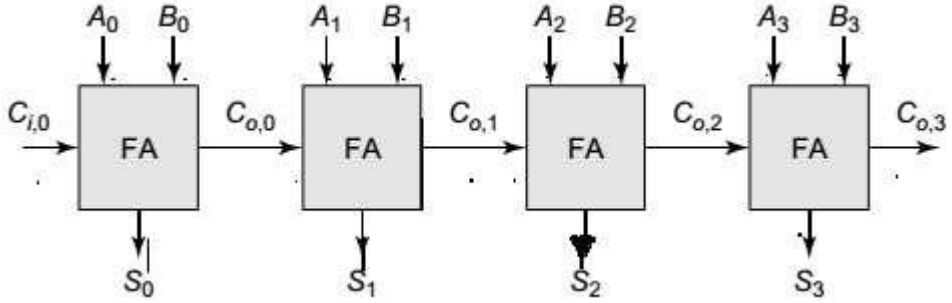
PART * A

Q.No.	Questions
1.	**What is datapath? (Nov/Dec 2019)** BTL2 A datapath is the data processing section of a processor. It consists of several multiple-bit data path elements or operators such as arithmetic units (adder, multiplier, shifter, comparator) or logical operators (AND, OR, NAND) arranged horizontally and connected with buses. Control signals connect to the datapath at the top and bottom.
2.	**What are the advantages of datapath operator? (Nov/Dec 2019)** BTL2 The advantage of datapath operators are: • To implement the logic function using n-identical circuits. • Data may be arranged to flow in one direction, while any control signals are introduced in the orthogonal direction to the data flow.
3.	**What is bit slice operation? (April/May 2019)** BTL2 Bit slicing is a technique for constructing a particular word length of block from modules of smaller bit width. Each of these components processes one bit field or "slice" of an operand. The grouped processing components would then have the capability to process the chosen full word-length.
4.	**What are the advantages of full adder design using static CMOS? (April/May 2019)** BTL2 The primary advantages of this static CMOS full adder are: • It has full swing outputs that increase noise margin and reliability. • It functions well at low power supply voltages because it does not have threshold loss problem. • The adder can be manufactured by a basic conventional CMOS process with some mobility loss.
5.	**What are the disadvantages of full adder design using static CMOS? (Nov/Dec 2018)** BTL2 The major shortfalls associated with the static CMOS full adder are: • Large PMOS transistor in pull up network result in high input capacitances, which cause high delay and dynamic power. • The critical path delay of SUM sub-circuit depends on the signal statistics of CARRY sub-block and inverter delay. Therefore the propagation delay is high in the static CMOS full adder realization. • The intrinsic load capacitance of the CARRY signal is high which is contributed by the gates capacitances C1, C2, C3, C4, C5 and C6, diffusion capacitances in stage 1 and stage 2 and wiring capacitance. • This adder realization consumes a large area and it could possible to fabricate in twin-tub CMOS process to avoid mobility degradation and latch up condition.
6.	**Define Logical optimization. (Nov/Dec 2018)** BTL2 Logical optimization can be achieved by transforming one logic circuit to another that is functionally equivalent. Logical optimization techniques use logical restricting rules to transform on network to

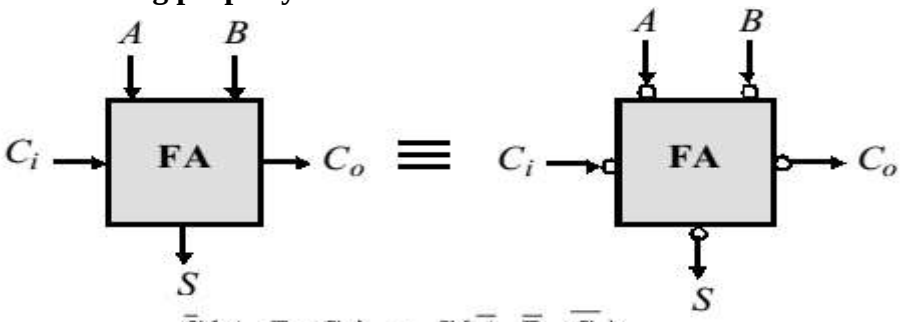
	another that I functionally equivalent to produce effective power optimization for reduced supply voltages.
7.	**Draw the truth table of a binary full adder and write the expressions for sum and carry output. (April/May 2018)** BTL3 

A	B	C_i	S	C_o	Carry status
0	0	0	0	0	delete
0	0	1	1	0	delete
0	1	0	1	0	propagate
0	1	1	0	1	propagate
1	0	0	1	0	propagate
1	0	1	0	1	propagate
1	1	0	0	1	generate
1	1	1	1	1	generate

$$S = A \oplus B \oplus C_i$$
$$= A\bar{B}\bar{C}_i + \bar{A}B\bar{C}_i + \bar{A}\bar{B}C_i + ABC_i$$
$$C_o = AB + BC_i + AC_i$$

8.	**Write the expressions for the intermediate signals: generate, delete and propagate for a binary adder and express sum and carry out in terms of the above. (April/May 2018)** BTL5 $Generate\ (G) = AB$ $Propagate\ (P) = A \oplus B$ $Delete = \overline{A}\,\overline{B}$ $C_o(G,P) = G + PC_i$ $S(G,P) = P \oplus C_i$
9.	**Draw the topology of a four bit ripple carry adder.**BTL3 
10.	**What is the worst case propagation delay in an N bit ripple carry adder?** BTL2 $t_{adder} = (N-1)t_{carry} + t_{sum}$
11.	**What are the main stages of an array multiplier?** BTL1 The main stages of an array multiplier are: partial product generation, partial product accumulation and final addition.
12.	**What is meant by clustered voltage-scaling?** BTL2 Clustered voltage-scaling is a method of distributing a wide range of supply voltages inside a block. In this technique, each path starts with the high supply voltage and switches to the low supply when delay slack is available.

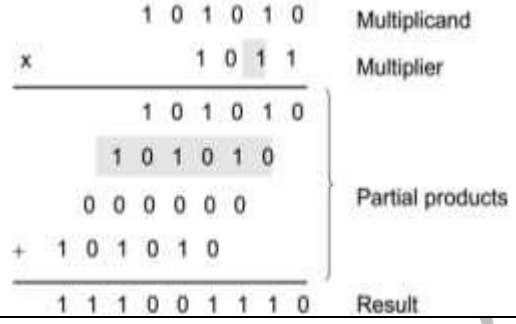
13. **Write the inverting property associated with a full adder.** BTL3



$$\bar{S}(A,B,C_i) = S(\bar{A},\bar{B},\bar{C_i})$$

$$\overline{C_o}(A,B,C_i) = C_o(\bar{A},\bar{B},\bar{C_i})$$

14. **Illustrate binary multiplication using a simple example. Specify the bit size of the inputs and the partial products.**BTL3



15. **What is booth's recoding? Draw a partial product selection table for the same.** BTL2

Booth's recoding reduces the number of partial products to at most half. It ensures that for every two consecutive bits at most one bit will be 1 or -1. Reducing the number of partial products is equivalent to reduce the number of additions, which leads to a speedup as well as an area reduction.

Partial Product Selection Table

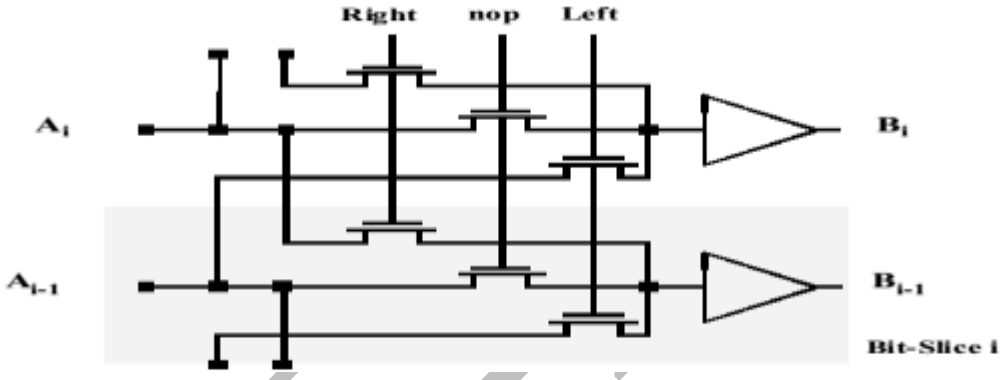
Multiplier Bits	Recoded Bits
000	0
001	+Multiplicand
010	+Mutiplicand
011	+2xMultiplicand
100	-2xMultiplicand
101	-Multiplicand
110	-Multiplicand
111	0

16. **What is the necessity of a level converter? Draw a simple circuit of the same.** BTL3

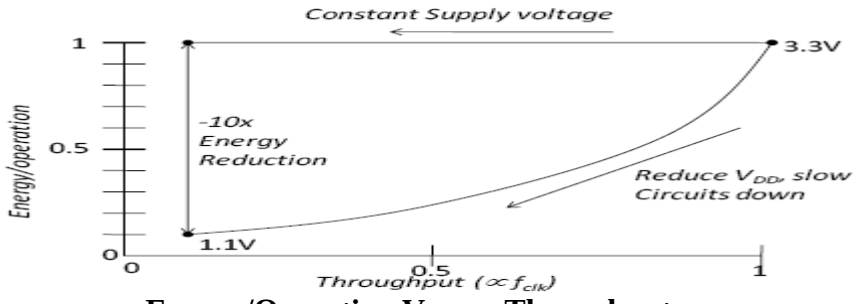
When combining multiple supply voltages on a die, level converters are required whenever module at the lower power supply has to drive a gate at the higher voltage. If a gate supplied by VDDL drives agate at VDDH, the PMOS transistor never turns off, resulting in static current and reduced output swing. A level conversion performed at the boundaries of supply voltage domains prevents these problems.

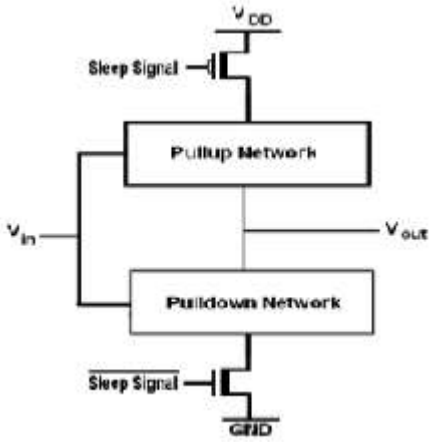
17. **What method is adopted to reduce power in idle mode?** BTL4

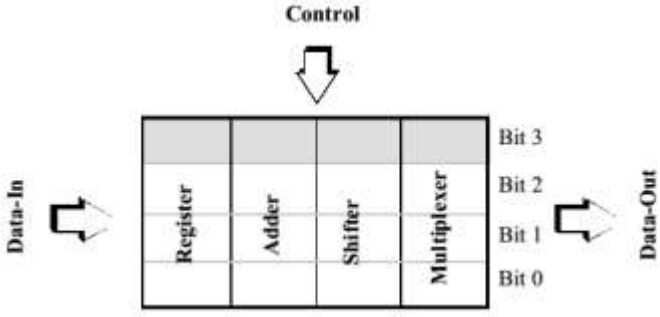
A common method to reduce power in idle mode is clock gating. In this method, the main clock connection to a module is turned off (or gated) whenever the block is idle. However clock gating

	does not reduce leakage current in idle module.
18.	**List the different considerations for designing a Ripple carry adder.** BTL1 • Propogation delay of ripple carry adder is linearly proportional to N. • It is important to optimize tcarry than tsum. • Inverting all i/ps to a full adder results in inverted values for all o/ps.
19.	**What are the draw backs of a static adder circuit?** BTL1 • Consumes large area. • Circuit is slow.
20.	**What is the advantage of Dynamic Supply Voltage Scaling (DVS)?** BTL2 Lowering the clock frequency when executing the reduced workloads reduces the power but does not save energy- every operation is still executed at the high voltage level. However if both supply voltage and frequency are reduced simultaneously, the energy is reduced. In order to maintain the required throughput for high workloads and minimize energy for low workloads, both supply and frequency must be dynamically varied according to the requirements application that is currently being executed. This technique is called Dynamic Supply Voltage Scaling (DVS).
21.	**Draw the circuit of one bit programmable shifter.** BTL3 
22.	**Tabulate various power minimization techniques in datapath structures.** BTL4

	Design Time	Sleep Mode	Run Time
Active Transistors	Lower V_{DD}, Multi V_{DD} Tansistor Sizing Logic Optimization	Clock Gating	Dynamic Voltage Scaling
Leakage Transistors	Multi V_{th}	Sleep transistors	Variable V_{th}

23.	**Draw the energy/operation versus throughput curve for constant and variable supply voltage operation.** BTL4  **Energy/Operation Versus Throughput**

24.	**What are the parts of a DVS system?** BTL3 A practical implementation of the DVS system consists of the following: • A processor that operate at a wide variety of supply voltages. • A power regulation loop that sets the minimum voltage necessary for operation at a desired • frequency • An operating system that calculates the desired frequencies to meet required throughputs and task completion deadlines.
25.	**Illustrate threshold voltage control in an inverter.** BTL4 Substrate bias is the control knob that allows us to vary the threshold voltages dynamically. In order to do so, we have to operate the transistors as four- terminal devices. Variable threshold voltage scheme can accomplish a variety of goals: • It can lower the leakage in standby mode • It can compensate for threshold voltage variations across the chip during normal operation of the circuit • It can throttle the throughput of the circuit to lower both the active and leakage power based on performance requirements
26	**What is the total time delay for a ripple carry Adder?** BTL2 Tadder = (N-1) tcarry + tsum.
27	**Write down the Expression for the total propogation delay in an n bit carry bypass Adder.** BTL2 Tp = tset up + M tcarry + (N/M-1) tbypass + M tcarry + tsum.
28.	**Why is static adder circuit slow?** BTL2 A static adder ckt is slow as, • Long chains of series PMOS transistors are present in both carry & Sum generation circuit. • Intrinsic load capacitance of the Co signal is large & consists of 2 diffusion & 6 gate capacitances plus the wiring g capacitances. • Carry generation ckt requires 2 inverting stages per bit. • Sum generation ckt requires an extra logic stage
29.	**Draw the structure of a sleep transistor.**BTL4 
30.	**What is the advantage of Dynamic adder design?** BTL2 Reduced capacitance of dynamic circuitry results in substantial speed up over static implementation.
31.	**Determine propagation delay of n-bit carry select adder. (May/June 2016)** BTL3 tadd = tsetup + M tcarry + (N / M) tmax + tsum where tsetup,tsum,tmax are fixed delays. N and M represents the total number of bits and no.of bits per stage respectively. tcarry is the delay of carry through a single full adder cell.

32.	**Give the application of high speed adder. (April / May 2017).** BTL4 High speed Adders will reduce the hardware complexity and make justice with Speed Power,Area and Accuracy metrics. Adders are one of the key components in arithmetic circuits. Approximation can increase performance or reduce power consumption with a simplified or inaccurate circuit in application contexts where strict requirements are relaxed. The potential application is in the DSP application for portable devices such as cell phones and laptops.
33.	**Draw a bit sliced datapath organization / What is meant by bit-sliced data path organization? List out the components of data path. (April / May 2017).** BTL2 Datapaths are often arranged in bit sliced organization instead of operating on single-bit digital signals. The data in a processor are arranged in a word based fashion. A 32 bit processor operates as data words that are 32bits word wide. This is reflected in the organization of datapath. Since the same operation frequently has to be performed on each bit of the data word, the datapaths consist of 32 bit slices, each operating on single bit, hence the term bit-sliced. 
34.	**Write the principle of any one fast multiplier? (Nov/Dec 2016)** BTL2 Booth multiplier is a radix -4 multiplication scheme , which examines 3 bits of the multiplicand at a time to determine whether to add 0,1,-1,2,-2 of that rank of the multiplicand.
35.	**Define throughput.** BTL2 A metric called throughput is often used as a measure of the utilization of a microprocessor system. The throughput is the number of operations for the number of instructions performed over a unit period of time. The throughput is typically described in terms of either millions of operations per second or million of instructions per second.
	PART * B
1.	**Explain the concept of a carry look ahead adder with neat diagram.(13M)(May/June 2014,2016) (Nov/Dec 2016,2019)** BTL3 **Answer: Page 4.25-4.28-Dr.R.Uma** Carry Look ahead Adder- Cicuit-carry look ahead generator (4M) Definition of carry generate and carry propagate (5M) Manchester carry style- static circuit- dynamic circuit (4M)
2.	**Discuss the details about power and speed trade off.(13M) (April/May 2017,2018)** BTL2 **Answer: Page 4.56-4.71-Dr.R.Uma** **Optimization during Enable time- Optimization of targeted dissipation source** (3M) **Design time power Reduction Techniques** (8M) Reducing supply voltage-Logical Optimization- Architectural optimization-power Reduction using pipelining-Multiple Supply Voltage- Module level voltage reduction- Multiple threshold circuits-Reducing switching capacitance through transistor sizing-Reducing switching activity by resource allocation- Reducing glitching through path balancing- Multiple supply voltage **Run time power Management** (2M) Dynamic supply voltage Scaling-Variable threshold CMOS (VTCMOS)

3.	**Explain the concept of a high speed adder.(13M) (Nov/Dec 2016,2019) (May/June 2016)**BTL2 **Answer: Page 4.15-4.34-Dr.R.Uma** Binary Adder- Logic Design consideration-Ripple carry Adder Carry Bypass Adder-Delay Calculation- Advantages of CByA- Disadvantages of CByA Carry Skip Adder- Delay Calculation- Advantages of CSA-Disadvantages of CSA Carry Select Adder- Delay Calculation- Advantages of CSelA- Disadvantages of CSelA	 (3M) (4M) (3M) (3M)
4.	**Explain the structure of a Barrel Shifter.(13M) (April/May 2015,2018, Nov/Dec 2015,2018)** BTL2 **Answer: Page 4.51- 4.56- Dr.R.Uma** Shift and Rotate Operation- 4 bit rotate right network 4 bit rotate left network Barrel shifter working operation	 (4M) (3M) (3M) (3M)
5.	**Design a divider circuit and write down its working function and discuss their features.(13M)** BTL5 Restoring Division-Algorithm for restoring Division Block diagram for 4 bit binary divider restoring divider Cycles of operation Non restoring Division- Algorithm for Non restoring Division Block Diagram for non-restoring division algorithm Cycles of Operation	 (3M) (2M) (2M) (3M) (2M) (1M)
	PART * C	
1.	**Design a 4 X 4 array multiplier and write down the equation for delay.(15M) (May/June 2016,2018)** BTL6 **Answer: Page 4.35-4.38-Dr.R.Uma** Multiplier- Parallel array multiplier design- Basic Principles of Multiplication Unsigned 4x4 array multiplier using RCAs Unsigned 4x4 array multiplier using CSAs Delay Calculation	 (4M) (4M) (4M) (3M)
2	**Explain the operation of booth multiplication with suitable examples? Justify how booth algorithms speed up the multiplication process. (15M) (Nov/Dec 2016,2019)** BTL2 **Answer: Page 4.41-4.43- Dr.R.Uma** Booth Multiplier Concepts Actions during booth Multiplication Structure of Booth Multiplier Justification for speed up process	 (4M) (4M) (3M) (4M)
3	**Explain the concept of modified booth multiplier with suitable example. (15M)(April/May 2017,2018)**BTL2 **Answer: Page 4.41-4.43- Dr.R.Uma** Booth Multiplier Concepts Actions during booth Multiplication Structure of Booth Multiplier Justification for speed up process	 (4M) (4M) (3M) (4M)

UNIT V – IMPLEMENTATION STRATEGIES AND TESTING

FPGA Building Block Architectures, FPGA Interconnect Routing Procedures. Design for Testability: Ad Hoc Testing, Scan Design, BIST, IDDQ Testing, Design for Manufacturability, Boundary Scan.

PART * A

Q.No.	Questions
1.	**What is an FPGA? (Nov/Dec 2014,2019)** BTL2 FPGA is Field Programmable Gate Array that consists of an array of anywhere from 64 to 1000s of logic gate groups that are sometimes called configurable logic blocks.
2.	**What is SOG? (Nov/Dec 2019)** BTL2 A channelless gate-array is called sea-of-gates (SOG) array. The core area of the die is completely filled with an array of base cells (the base array).
3.	**Compare FPGA and CPLD? (April/May 2019)** BTL4 **CPLD's** have a much higher capacity than simple PLDs, permitting more complex logic circuits to be programmed into them. A typical CPLD is equivalent of from 2 to 64 simple PLDs. The development of these devices followed simple PLD as advances in technology permitted higher density chips to be implemented. There are several forms of CPLD, which vary in complexity and programming capability. CPLDs typically come in 44 to 160 pin packages depending on the complexity. **FPGA** are different from simple PLDs and CPLDs in their internal organization and have the greatest logic capacity. FPGAs are consists of an array of anywhere from 64 to 1000s of logic gate groups that are sometimes called logic blocks. Two basic classes of FPGAs are fine grained and course grained .The course grained FPGA has large logic blocks and fine grained FPGAs has much smaller logic blocks. FPGAs are come in packages up to 1000 pins or more.
4.	**Differentiate CBIC & Gate array logic? (April/May 2019)** BTL4

CBIC	Gate array logic
Cell-based IC uses predesigned logic cells (AND gates, OR gates, multiplexers, and flip-flops, for example)	In a gate array (GA) or gate-array–based ASIC the transistors are predefined on the silicon wafer.
CBIC means a standard-cell–based ASIC	it is often called a masked gate array (MGA).
The standard-cell areas in a CBIC are built of rows of standard cells. The standard-cell areas may be used in combination with larger predesigned cells, known as megacells.	The logic cells in a gate-array library are often called macros.

5.	**List out three main parts of FPGA & what is PMS? (Nov/Dec 2018)** BTL1 • CLB-Configurable Logic Block • IOB-Input Output Block • PMS-Programmable Switch Matrix
6.	**List the types of ASIC?/ State the different types of ASICs. (May/June 2014) (Nov/Dec 2018)** BTL1 • Full-Custom ASICs • Semicustom ASICs : – Standard-Cell–Based ASICs

– Gate-Array–Based ASICs
- Channeled Gate Array
- Channelless Gate Array
- Structured Gate Array

Programmable ASICs , for which all of the logic cells are predesigned and none of the mask layers are customized.
– Programmable Logic Devices
- – Field-Programmable Gate Arrays

7. **What is Full custom ASIC?/What are the features of full custom ASIC? (April/May 2015,2018) (May/June 2016)** BTL2

To modify according to a customer's individual requirements, All mask layers are customized in a full custom ASIC
- Generally, the designer lays out all cells by hand
- Some automatic placement and routing may be done
- Critical (timing) paths are usually laid out completely by hand

Full-custom design offers the highest performance and lowest part cost (smallest die size) for a given design. The manufacturing lead time (the time it takes just to make an IC—not including design time) is typically eight weeks for a full-custom IC.

8. **Write the objectives and Goals of System Partitioning. (April/May 2018)** BTL1

The goal of partitioning is to divide this part of the system so that each partition is a single ASIC. To do this we may need to take into account any or all of the following objectives:
- A maximum size for each ASIC
- A maximum number of ASICs
- A maximum number of connections for each ASIC
- A maximum number of total connections between all ASICs

9. **What is JTAG?** BTL2

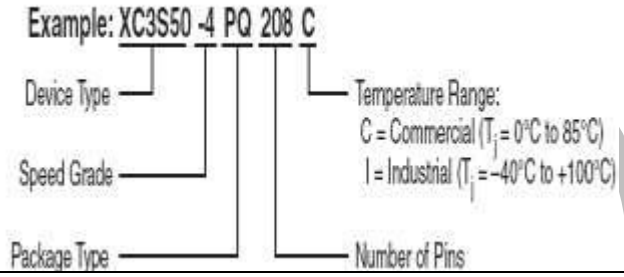
Joint Test Action Group *(JTAG)*

10. **What is fully PCI in Spartan-II FPGA?** BTL2

Fully Peripheral Component Interface (PCI) used to interface components.

11. **Differentiate fine-grain and coarse-grain architecture of FPGA** BTL4

Fine-grained Architecture	Coarse-grained Architecture
Manipulate data at the bit level	Manipulate groups of bits via complex functional units such as ALUs (arithmetic logic units) and multipliers
Designers can implement bit manipulation tasks without wasting reconfigurable resources	Reconfigurable resources are wasted during data manipulation
For large and complex calculations numerous fine-grained PEs are required to implement a basic computation	Fewer coarse-grained PEs are required to implement a basic computation
Much slower clock rates	Faster
Extremely costly relative to coarse-grained architectures	Less Expensive
Supports partial array configuration and is dynamically reconfigurable during application execution.	Both partially and dynamically reconfigurable

12.	**State the Xilinx FPGA design flow.**BTL1 • Specification • VHDL description - Functional simulation • Synthesis - Post-synthesis simulation • Implementation - Timing simulation • Configuration - On chip testing
13.	**What are the different types of interconnections present in Xilinx FPGA?**BTL2 **Direct interconnect:** Adjacent CLBs are wired together in the horizontal or vertical direction. The most efficient interconnect. **General-purpose interconnect:** used mainly for longer connections or for signals with a moderate fanout. **Long line interconnect:** for time critical signals (e.g. clock signal need be distributed to many CLBs)
14.	**What is meant by speed grading?**BTL2 Most of the FPGA header short chip according to speed is called speed binning or speed grading. According to Xilinx FPGA product, The speed grade specify the transistor switching speed that determines how quickly internal clocked circuits can be activated. 
15.	**What is meant by BIDA?**BTL2 The Bidirectional Interconnect Buffers (BIDA) restore the logic level and logic strength on long interconnect paths.
16.	**Define OEM?** BTL2 For any ASIC, a designer needs design-entry software, a cell library and physical design software. Often designers buy that software from FPGA vendor. This is called an Original Equipment Manufacturer (OEM) arrangement.
17.	**What are the advantages and disadvantages of FPGA compared to ASIC?**BTL4

FPGA	ASIC
Faster time-to-market since none of the mask layers are customized	Full custom capability for design since device is manufactured to design specs
Simpler design cycle due to software that handles much of the routing, placement, and timing	Design cycle is not simple.
Field reprogramability - A new bit stream can be uploaded remotely	Field reprogramability is not possible
Design turnaround is a few hours	Two days to two weeks

18.	**Define segmented Channel routing?**BTL2 FPGA is a channeled architecture. The logic modules which implement various types of logic functions are placed in predefined rows. Channels are defined in between rows of logic modules for routing of nets. The rows of logic modules are called tracks. The tracks are divided into different segments which can be connected together by programming a horizontal antifuse. Each input and output of a logic module is connected to a dedicated vertical segment. Cross antifuses are located at

	the crossing of each horizontal and vertical segment. Programming these antifuses produces a bi-directional connection between the horizontal and vertical segments for routing of nets via channels. This structure of FPGA is called segmented channel routing.
19.	**Differentiate between Altera MAX 9000 and Altera FLEX interconnects architecture.** BTL4 The MAX 9000 is a coarse-grained architecture. Complex PLDs with arrays that are themselves arrays of macrocells have a dual-grain architecture. The FLEX architecture is of finer grain than the MAX arrays because of the difference in programming technology. The FLEX horizontal interconnect is much denser than the vertical interconnect creating an aspect ratio of 10:1.
20.	**List the advantages of Global routing. (May/June 2014)** BTL2 We typically global route the whole chip (or large pieces if it is a large chip) before detail routing the whole chip (or the pieces). There are two types of areas to global route: inside the flexible blocks and between blocks. The goal of global routing is to provide complete instructions to the detailed router on where to route every net. The objectives of global routing are one or more of the following: • Minimize the total interconnect length. • Maximize the probability that the detailed router can complete the routing. • Minimize the critical path delay.
21.	**What are feedthrough cells? State their uses. (May/June 2016)**BTL2 The term feedthrough cells can refer either to a piece of metal that is used to pass a signal through a cell or to a space in a cell, waiting to be used as a feed through.
22.	**What is the standard cell-based ASIC design?(Nov/Dec 2016)** BTL2 In cell based design, the designer reuses the cells that have already been designed and stored in the library as a part of the current design. Cell – based IC used predesigned logic cells(AND gates, OR gates, multiplexers and flip flop). CBIC means standard cell based ASIC. The standard-cell areas in a CBIC are built of rows of standard cells. The standard-cell areas may be used in combination with larger predesigned cells known as mega cells.
23.	**What is an antifuse? State its merits and demerits. (Nov/Dec 2016)** BTL2 An antifuse is an electrical device that performs the opposite function to a fuse. Whereas a fuse starts with a low resistance and is designed to permanently break an electrically conductive path (typically when the current through the path exceeds a specified limit), an antifuse starts with a high resistance and is designed to permanently create an electrically conductive path (typically when the voltage across the antifuse exceeds a certain level). **Demerits:** The size of an antifuse is limited by the resolution of the lithography equipment used to makes ICs. The Actel antifuse connects diffusion and polysilicon, and both these materials are too resistive for use as signal interconnects. To connect the antifuse to the metal layers requires contacts that take up more space than the antifuse itself, reducing the advantage of the small antifuse size. However, the antifuse is so small that it is normally the contact and metal spacing design rules that limit how closely the antifuses may be packed rather than the size of the antifuse itself. **Merits:** There are two advantages of a metal–metal antifuse over a poly–diffusion antifuse. The first is that connections to a metal–metal antifuse are direct to metal—the wiring layers. Connections from a poly–diffusion antifuse to the wiring layers require extra space and create additional parasitic capacitance. The second advantage is that the direct connection to the low-resistance metal layers makes it easier to use larger programming currents to reduce the antifuse resistance. Average QuickLogic metal– metal antifuse resistance is approximately 80 W (with a standard deviation of about 10 W) using a programming current of 15 mA as opposed to an average antifuse resistance of 500 W (with a programming current of 5 mA) for a poly–diffusion antifuse.
24.	**What is meant by CBIC? (April/May 2017)** BTL2 Cell – based IC used predesigned logic cells (AND gates, OR gates, multiplexers and flipflop). CBIC

	means standard cell based ASIC. The standard-cell areas in a CBIC are built of rows of standard cells. The standard-cell areas may be used in combination with larger predesigned cells known as megacells.
25.	**Name the elements in a Configurable Logic Block (April/May 2017)**. BTL1 Flip flops to store data and Look up tables and Multiplexers to implement logic.
	PART * B
1.	**Explain about the different types of ASIC with neat diagram. (13M) (April/May 2017,2019)** BTL2 **Answer: Page: 5.2-5.15- Dr.R.Uma** Application Specific Integrated Circuits- Examples- Advantages- Types (3M) Full custom ASIC- Semi-custom ASIC- Standard Cell Based ASICs- Gate array based ASICs (4M) Channelled Gate Array- Channelless Gate Array- Structured Gate Array (2M) Field Programmable Gate Array- Programmable Logic Devices Structure-Programmable Array Logic- Programmable Logic Devices (4M)
2.	**Describe the architecture of FPGA with Configurable Logic Block and Programmable interconnect technology. (13M) (April/May 2015,2018) (Nov/ Dec 2016,2019)**BTL2 **Answer: Page: 5.22-5.38- Dr.R.Uma** FPGA building block Architectures- Input Output Blocks (3M) Programmable Interconnects- Direct Interconnects between Adjacent CLB (3M) ACT 1 Series FPGA- ACT 1 Logic Module-ACT 2 Family- IO pad Drivers- Clock Networks-ALTERA-Logic Array Blocks- Macrocells (3M) Configurable Logic Blocks- Function Generators- I/O Blocks- Programmable Interconnect-Programmable Switch Matrix (4M)
3.	**With a neat Flowchart, explain the ASIC design flow. (13M) (May/June 2014)**BTL4 **Answer: Page: 5.38-5.40-Dr.R.Uma** Design Entry- Logic Synthesis- System Partitioning- Pre layout simulation- Floor Planning-Placement- Routing- Extraction- Post layout simulation (9M) Flow chart Diagram (4M)
4.	**Write explanatory notes on FPGA (13M) (May/June 2014)** BTL2 **Answer: Page: 5.22-5.38- Dr.R.Uma** FPGA building block Architectures- Input Output Blocks (4M) ACT 1 Series FPGA- ACT 1 Logic Module-ACT 2 Family- IO pad Drivers- Clock Networks-ALTERA-Logic Array Blocks- Macrocells (4M) Configurable Logic Blocks- Function Generators- I/O Blocks- Programmable Interconnect-Programmable Switch Matrix (5M)
5.	**Explain features of semi-custom ASIC and its types.(13M) (April/May 2015)**BTL2 **Answer: Page: 5.2-5.15- Dr.R.Uma** Semi-custom ASIC- Standard Cell Based ASICs- Gate array based ASICs (5M) Channelled Gate Array- Channelless Gate Array- Structured Gate Array (4M) Field Programmable Gate Array- Programmable Logic Devices Structure-Programmable Array Logic- Programmable Logic Devices (4M)
	PART * C
1.	**Write brief notes on** **a. Semi-custom ASIC** **b. Full Custom ASIC. (15M)(May/June 2016) (Nov/ Dec 2016,2019)** BTL2 **Answer: Page: 5.2-5.15- Dr.R.Uma**

	Application Specific Integrated Circuits- Examples- Advantages- Types (4M) Full custom ASIC- Semi-custom ASIC- Standard Cell Based ASICs- Gate array based ASICs (5M) Channelled Gate Array- Channelless Gate Array- Structured Gate Array (2M) Field Programmable Gate Array- Programmable Logic Devices Structure-Programmable Array Logic- Programmable Logic Devices (4M)
2	**With neat sketch explain the CLB,IOB and programmable interconnects of an FPGA device. (15M) (May/June 2016)** BTL2 **Answer: Page: 5.22-5.38- Dr.R.Uma** FPGA building block Architectures- Input Output Blocks (3M) Programmable Interconnects- Direct Interconnects between Adjacent CLB (3M) ACT 1 Series FPGA- ACT 1 Logic Module-ACT 2 Family- IO pad Drivers- Clock Networks-ALTERA-Logic Array Blocks- Macrocells (3M) Configurable Logic Blocks- Function Generators- I/O Blocks- Programmable Interconnect-Programmable Switch Matrix (4M)
3	**Write short notes on routing procedures involved in FPGA interconnect. (15M)(April/May 2017)**BTL2 **Answer: Page: 5.17-5.22-Dr.R.Uma** Routing Procedures- ACTEL Anti fuse Interconnect- (5M) Metal-Metal anti fuse- (4M) Actel Act Interconnect Scheme (4M)