JEPPIAAR INSTITUTE OF TECHNOLOGY

"Self-Belief | Self Discipline | Self Respect"

DEPARTMENT

OF

ELECTRICAL AND ELECTRONICS ENGINEERING

LECTURE NOTES

EE8451 – LINEAR INTEGRATED CIRCUITS AND APPLICATIONS

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UNIT IV SPECIAL ICs **9**

Functional block, characteristics of 555 Timer and its PWM application - IC-566 voltage-controlled oscillator IC; 565-phase locked loop IC, AD633 Analog multiplier ICs.

The 555 Timer IC

The 555 is a monolithic timing circuit that can produce accurate & highly stable time delays or oscillation. The timer basically operates in one of two modes: either
(i) Monostable (one - shot) multivibrator or
(ii) Astable (free running) multivibrator
The important features of the 555 timer are these:
(i) It operates on +5v to +18 v supply voltages
(ii) It has an adjustable duty cycle
(iii) Timing is from microseconds to hours
(iv) It has a current o/p

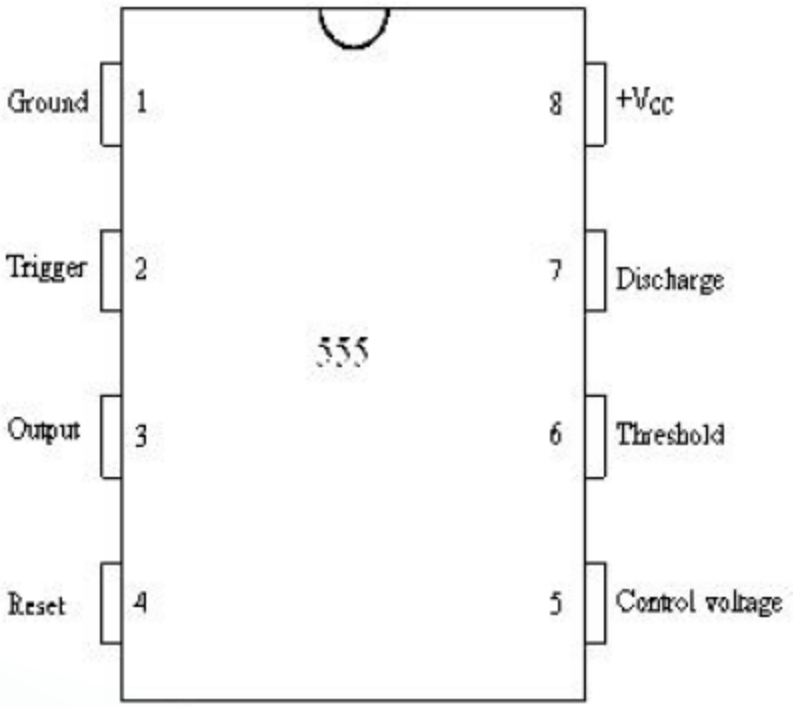


Fig. 5.16 Pin configuration of 555 timer

Pin description:

Pin 1: Ground**:**
All voltages are measured with respect to this terminal.
Pin 2: Trigger:
The o/p of the timer depends on the amplitude of the external trigger pulse applied to this pin.
Pin 3: Output:

There are 2 ways a load can be connected to the o/p terminal either between pin3 & ground or between pin 3 & supply voltage (Between Pin 3 & Ground ON load) (Between Pin 3 & + Vcc OFF load)

(i) When the input is low:

The load current flows through the load connected between Pin 3 & +Vcc in to the output terminal & is called the sink current.

(ii) When the output is high:

The current through the load connected between Pin 3 & +Vcc (i.e. ON load) is zero. However the output terminal supplies current to the normally OFF load. This current is called the source current.

Pin 4: Reset:

The 555 timer can be reset (disabled) by applying a negative pulse to this pin. When the reset function is not in use, the reset terminal should be connected to +Vcc to avoid any false triggering.

Pin 5: Control voltage:

An external voltage applied to this terminal changes the threshold as well as trigger voltage. In other words by connecting a potentiometer between this pin & GND, the pulse width of the output waveform can be varied. When not used, the control pin should be bypassed to ground with 0.01 capacitor to prevent any noise problems.

Pin 6: Threshold:

This is the non inverting input terminal of upper comparator which monitors the voltage across the external capacitor.

Pin 7: Discharge:

This pin is connected internally to the collector of transistor Q1.

When the output is high Q1 is OFF.

When the output is low Q is (saturated) ON.

Pin 8: +Vcc:

The supply voltage of +5V to +18V is applied to this pin with respect to ground.

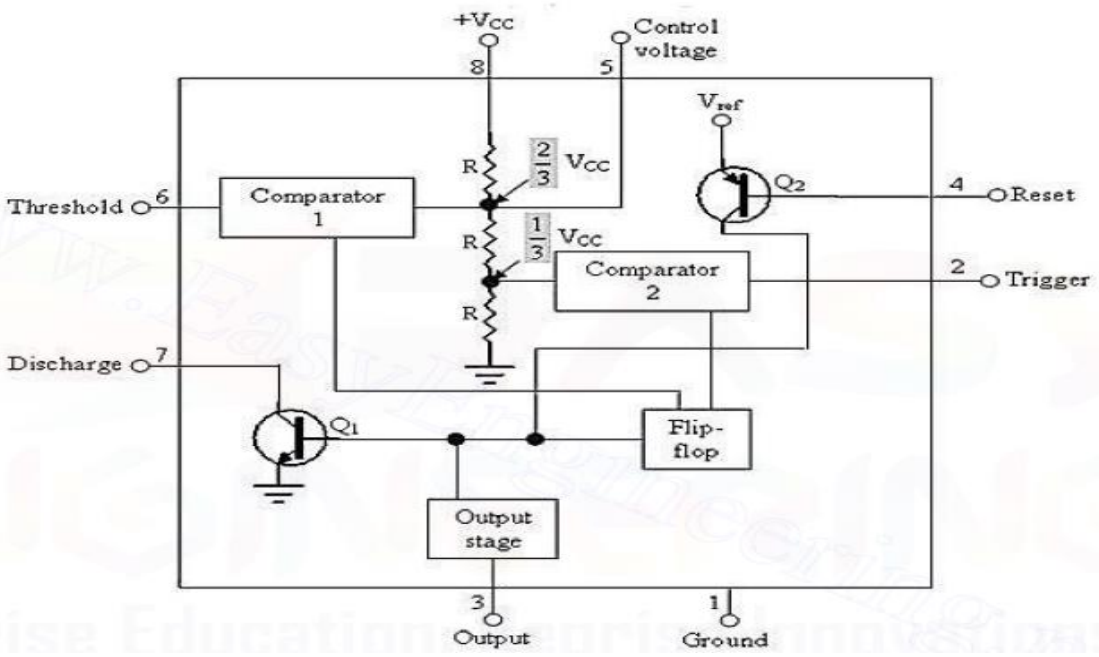


Fig.5.17 Block **Diagram of 555 Timer IC**

From the above figure, three 5k internal resistors act as voltage divider providing bias voltage of 2/3 Vcc to the upper comparator & 1/3 Vcc to the lower comparator. It is possible to vary time electronically by applying a modulation voltage to the control voltage input terminal (5).
(i) In the Stable state:
The output of the control FF is high. This means that the output is low because of power amplifier which is basically an inverter. Q = 1; Output = 0
(ii) At the Negative going trigger pulse:
The trigger passes through (Vcc/3) the output of the lower comparator goes high & sets the FF. Q = 1; Q = 0
(iii) At the Positive going trigger pulse: It passes through 2/3Vcc, the output of the upper comparator goes high and resets the FF. Q = 0; Q = 1
The reset input (pin 4) provides a mechanism to reset the FF in a manner which overrides the effect of any instruction coming to FF from lower comparator.

- **Monostable Operation:**

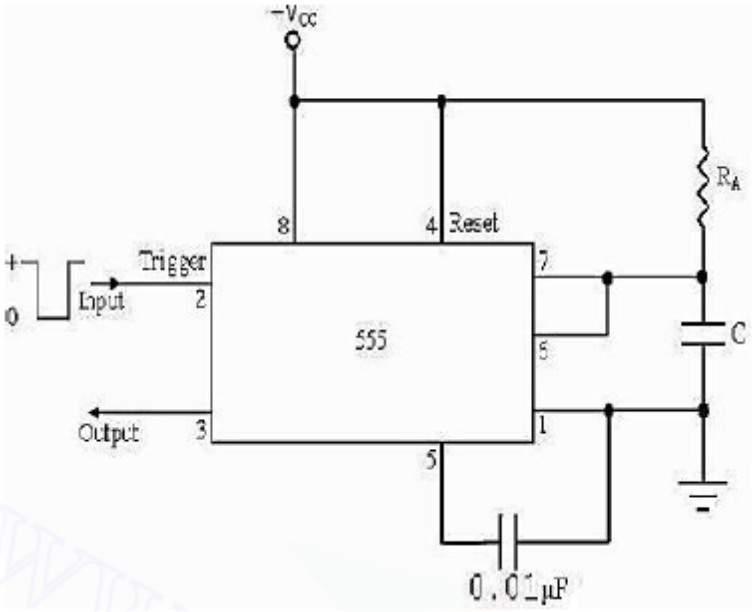


Fig. 5.18 555 connected as a Monostable Multivibrator

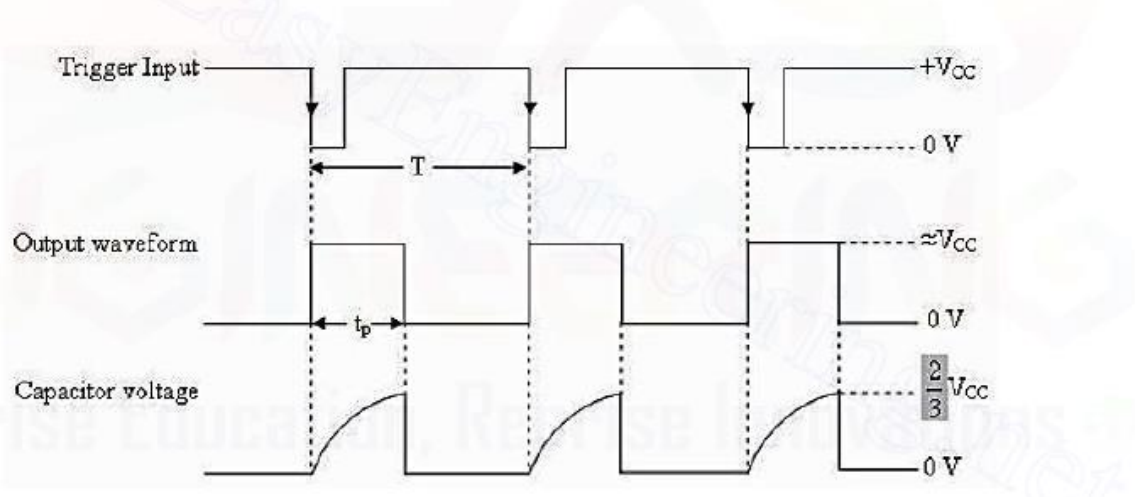


Fig. 5.19 Waveforms of monostable multivibrators

Initially when the output is low, i.e. the circuit is in a stable state, transistor Q1 is ON & capacitor C is shorted to ground. The output remains low. During negative going trigger pulse, transistor Q1 is OFF, which releases the short circuit across the external capacitor C & drives the output high. Now the capacitor C starts charging toward Vcc through RA. When the voltage across the capacitor equals 2/3 Vcc, upper comparator switches from low to high. i.e. Q = 0, the transistor Q1 = OFF ; the output is high.
Since C is unclamped, voltage across it rises exponentially through R towards Vcc with a time constant RC (fig b) as shown in below. After the time period, the upper comparator resets the FF, i.e. Q = 1, Q1 = ON; the output is low.[i.e discharging the capacitor C to ground potential (fig c)]. The voltage across the capacitor as in fig (b) is given by

$$V_c = V_{cc}(1 - e^{-t/RC}) \quad \ldots\ldots (1)$$

Therefore At t = T, Vc = 2/3 Vcc

$$\frac{2}{3} V_{cc} = V_{cc}(1 - e^{-T/RC})$$

or

$$T = RC \ln(1/3)$$

Or

$$T = 1.1RC \text{ seconds} \quad \ldots\ldots\ldots\ldots (2)$$

If the reset is applied Q2 = OFF, Q1 = ON, timing capacitor C immediately discharged. The output now will be as in figure (d & e). If the reset is released output will still remain low until a negative going trigger pulse is again applied at pin 2.

Applications of Monostable Mode of Operation:

(a) Frequency Divider:

The 555 timer as a monostable mode. It can be used as a frequency divider by adjusting the length of the timing cycle tp with respect to the time period T of the trigger input. To use the monostable multivibrator as a divide by 2 circuit, the timing interval tp must be a larger than the time period of the trigger input. [Divide by 2, tp > T of the trigger]
By the same concept, to use the monostable multivibrator as a divide by 3 circuit, tp must be slightly larger than twice the period of the input trigger signal & so on,
[divide by 3tp > 2T of trigger]

(b) Pulse width modulation:

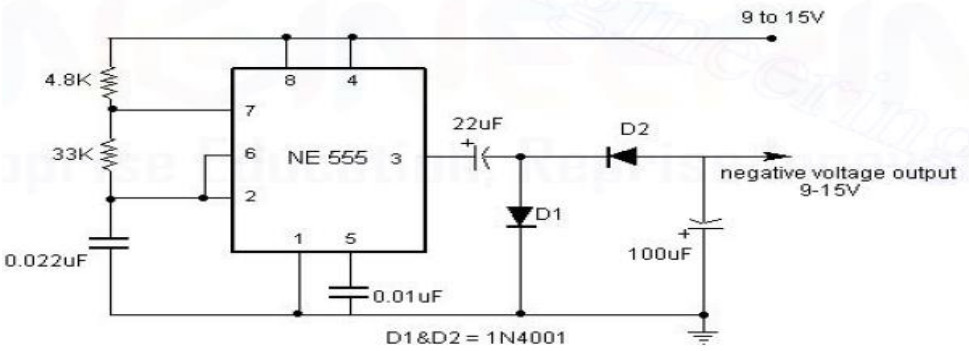


Fig.5.20 Pulse Width Modulation

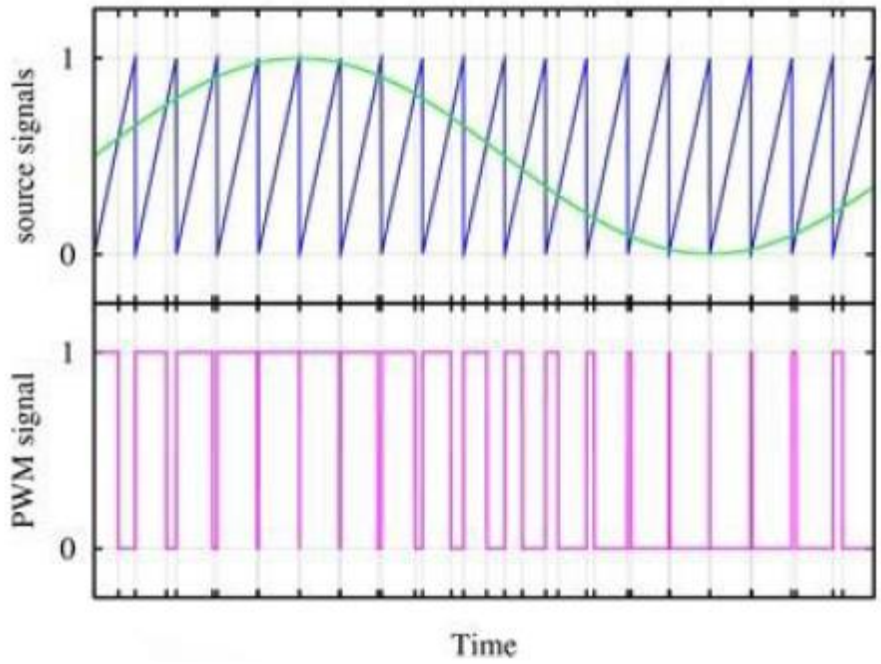


Fig. 5.21 Output Waveform

Pulse width of a carrier wave changes in accordance with the value of a incoming (modulating signal) is known as PWM. It is basically monostable multivibrator. A modulating signal is fed in to the control voltage (pin 5). Internally, the control voltage is adjusted to 2/3 Vcc externally applied modulating signal changes the control voltage level of upper comparator. As a result, the required to change the capacitor up to threshold voltage level changes, giving PWM output.

(c) Pulse Stretcher:

This application makes use of the fact that the output pulse width (timing interval) of the monostable multivibrator is of longer duration than the negative pulse width of the input trigger. As such, the output pulse width of the monostable multivibrator can be viewed as a stretched version of the narrow input pulse, hence the name "Pulse stretcher".

Often, narrow –pulse width signals are not suitable for driving an LED display, mainly because of their very narrow pulse widths. In other words, the LED may be flashing but not be visible to the eye because its on time is infinitesimally small compared to its off time. The 55 pulse stretcher can be used to remedy this problem. The LED will be ON during the timing interval tp = 1.1RAC which can be varied by changing the value of RA & C.

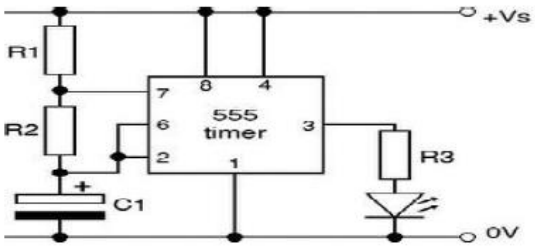


Fig.5.23 Pulse Stretcher

The 555 timer as an Astable Multivibrator:

An Astable multivibrator, often called a free running multivibrator, is a rectangular wave generating circuit. Unlike the monostable multivibrator, this circuit does not require an external trigger to change the state of the output, hence the name free running. However, the time during which the output is either high or low is determined by 2 resistors and capacitors, which are externally connected to the 555 timer.

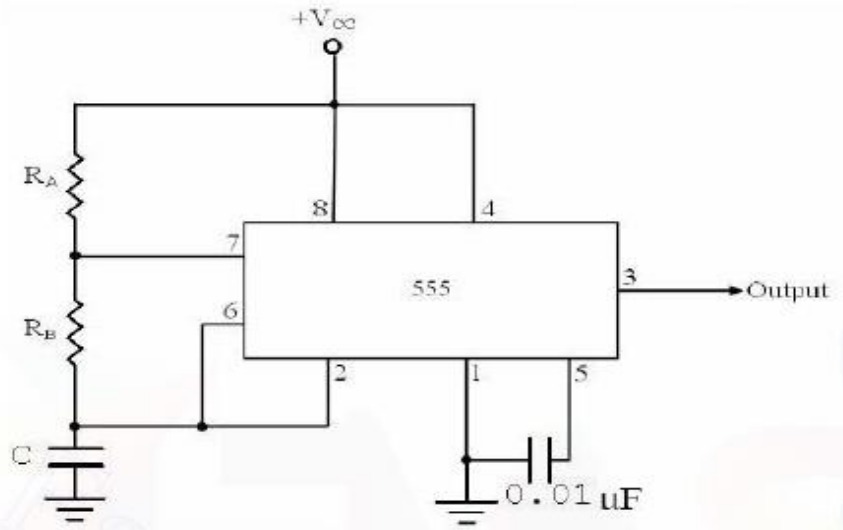


Fig.5.24 Astable Multivibrator

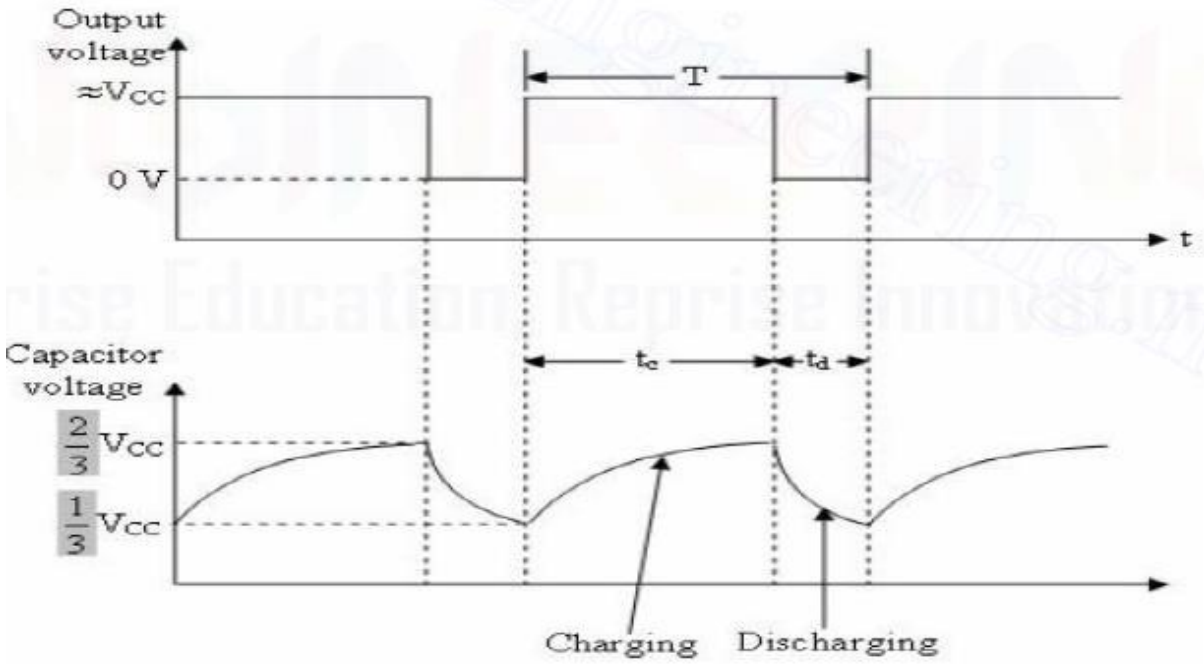


Fig. 5.25 Waveforms of Astable multivibrator

The above figures show the 555 timer connected as an astable multivibrator and its model graph

Initially, when the output is high :

Capacitor C starts charging toward Vcc through RA & RB. However, as soon as voltage across the capacitor equals 2/3 Vcc. Upper comparator triggers the FF & output switches low.

When the output becomes Low:

Capacitor C starts discharging through RB and transistor Q1, when the voltage across C equals 1/3 Vcc, lower comparator output triggers the FF & the output goes high. Then cycle repeats. The capacitor is periodically charged & discharged between 2/3 Vcc & 1/3 Vcc respectively. The time during which the capacitor charges from 1/3 Vcc to 2/3 Vcc equal to the time the output is high & is given by

$$tc = (RA+RB)C \ln 2 \quad \text{(1) Where } [\ln 2 = 0.69]$$
$$= 0.69 (RA+RB) C$$

Where RA & RB are in ohms. And C is in farads.

Similarly, the time during which the capacitors discharges from 2/3 Vcc to 1/3 Vcc is equal to the time, the output is low and is given by,

$$tc = RB\ C \ln 2$$
$$td = 0.69\ RB\ C \quad \text{..(2)}$$

where RB is in ohms and C is in farads.

Thus the total period of the output waveform is

$$T = tc + td = 0.69 (RA+2RB) C \quad \text{.(3)}$$

This, in turn, gives the frequency of oscillation as,

$$f\,0 = 1/T = 1.45/(RA+2RB)C \quad \text{(4)}$$

Equation 4 indicates that the frequency f 0 is independent of the supply voltage Vcc.

Often the term duty cycle is used in conjunction with the astable multivibrator. The duty cycle is the ratio of the time tc during which the output is high to the total time period T. It is generally expressed as a percentage.

$$\% \text{ duty cycle} = (tc / T) * 100$$
$$\% DC = [(RA+RB)/ /(RA+2RB)] * 100$$

Astable Multivibrator Applications:

(a) Square wave oscillator:

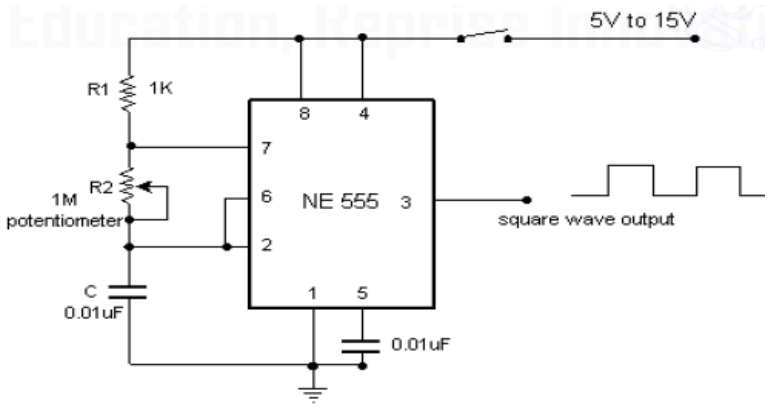
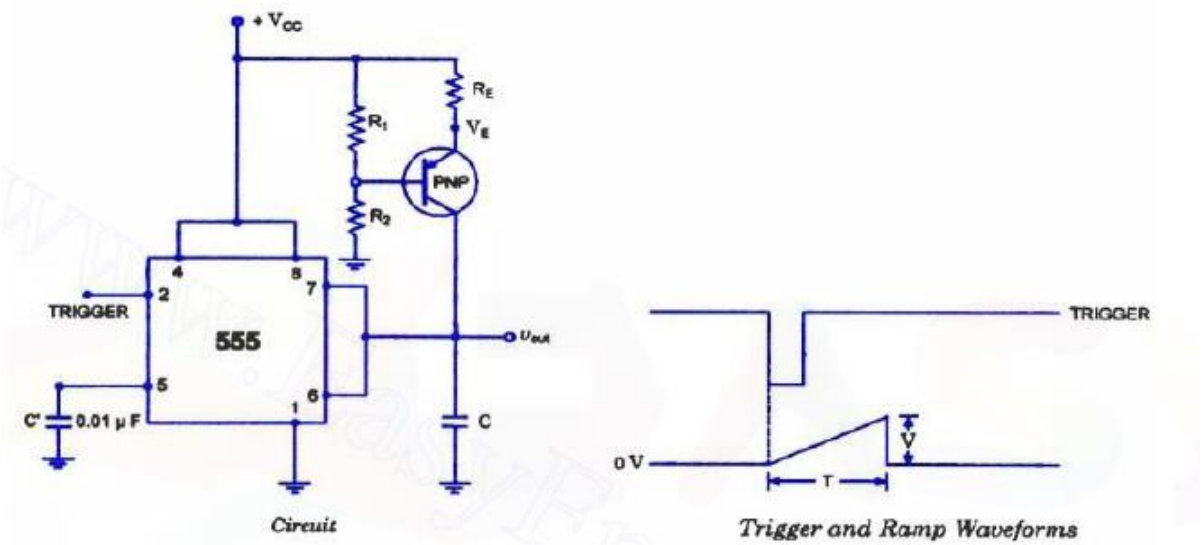


Fig.5.26 Square Wave Oscillator

Without reducing RA = 0 ohm, the astable multivibrator can be used to produce square wave output. Simply by connecting diode D across Resistor RB. The capacitor C charges through RA & diode D to approximately 2/3Vcc & discharges through RB & Q1 until the capacitor voltage equals approximately 1/3Vcc, then the cycle repeats.
To obtain a square wave output, RA must be a combination of a fixed resistor & potentiometer so that the potentiometer can be adjusted for the exact square wave.

(b) Free – running Ramp generator:



Ramp Generator Using The Timer 555

- The astable multivibrator can be used as a free – running ramp generator when resistor RA & RB is replaced by a current mirror.
- The current mirror starts charging capacitor C toward Vcc at a constant rate.
- When voltage across **C equals to 2/3 Vcc**, upper comparator turns transistor Q1 ON & C rapidly discharges through transistor Q1.
- When voltage across **C equals to 1/3 Vcc**, lower comparator switches transistor OFF & then capacitor C starts charging up again.
- Thus the charge – discharge cycle keeps repeating.
- The discharging time of the capacitor is relatively negligible compared to its charging time.
- The time period of the ramp waveform is equal to the charging time & is approximately is given by,

$$T = VccC/3IC$$

(1) $IC = (Vcc - VBE)/R$ = constant current

Therefore the free – running frequency of ramp generator is

$$f0 = 3IC/ Vcc\ C$$

Phase Locked Loop

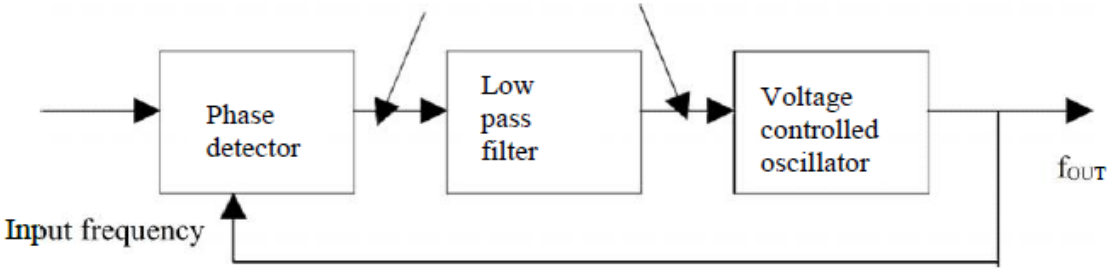


Fig 3.17 Block diagram of PLL

The PLL consists of i) Phase detector ii) LPF iii) VCO. The phase detector or comparator compares the input frequency fIN with feedback frequency fOUT.

- The output of the phase detector is proportional to the phase difference between fIN & fOUT. The output of the phase detector is a dc voltage & therefore is often referred to as the error voltage.
- The output of the phase detector is then applied to the LPF, which removes the high frequency noise and produces a dc level. This dc level in turn, is input to the VCO.
- The output frequency of VCO is directly proportional to the dc level. The VCO frequency is compared with input frequency and adjusted until it is equal to the input frequencies.
- PLL goes through 3 states, i) free running ii) Capture iii) Phase lock.

Before the input is applied, the PLL is in free running state. Once the input frequency is applied the VCO frequency starts to change and PLL is said to be in the capture mode. The VCO frequency continuous to change until it equals the input frequency and the PLL is in phase lock mode. When Phase locked, the loop tracks any change in the input frequency through its repetitive action. If an input signal vs of frequency fs is applied to the PLL, the phase detector compares the phase and frequency of the incoming signal to that of the output vo of the VCO. If the two signals differ in frequency of the incoming signal to that of the output vo of the VCO. The phase detector is basically a multiplier and produces the sum (fs + fo) and difference (fs - fo) components at its output. The high frequency component (fs + fo) is removed by the low pass filter and the difference frequency component is amplified then applied as control voltage vc to VCO. The signal vc shifts the VCO frequency in a direction to reduce the frequency difference between fs and fo. Once this action starts, we say that the signal is in the capture range. The VCO continues to change frequency till its output frequency is exactly the same as

the input signal frequency. The circuit is then said to be locked. Once locked, the output frequency fo of VCO is identical to fs except for a finite phase difference φ. This phase difference φ generates a corrective control voltage vc to shift the VCO frequency from f0 to fs and thereby maintain the lock. Once locked, PLL tracks the frequency changes of the input signal. Thus, a PLL goes through three stages (i) free running, (ii) capture and (iii) locked or tracking.

Capture range: the range of frequencies over which the PLL can acquire lock with an input signal is called the capture range. This parameter is also expressed as percentage of fo.

Pull-in time: the total time taken by the PLL to establish lock is called pull-in time. This depends on the initial phase and frequency difference between the two signals as well as on the overall loop gain and loop filter characteristics.

3.5.1 Phase Detector

Phase detector compares the input frequency and VCO frequency and generates DC voltage i.e., proportional to the phase difference between the two frequencies. Depending on whether the analog/digital phase detector is used, the PLL is called either an analog/digital type respectively. Even though most monolithic PLL integrated circuits use analog phase detectors.

Ex for Analog: Double-balanced mixer

Ex for Digital: Ex-OR, Edge trigger, monolithic Phase detector.

✓ Ex-OR Phase Detector:

This uses an exclusive OR gate. The output of the Ex-OR gate is high only when fIN or fOUT is high.

The DC output voltage of the Ex-OR phase detector is a function of the phase difference between its two outputs. The maximum dc output voltage occurs when the phase difference is Π radians or 180 degrees. The slope of the curve between 0 or Π radians is the conversion gain kp of the phase detector for eg; if the Ex-OR gate uses a supply voltage Vcc = 5V, the conversion gain Kp is

$$k_p = \frac{5}{\pi} = 1.59\ rad$$

.

Advantages of Edge Triggered Phase Detector over Ex-OR are

i) The dc output voltage is linear over 2Π radians or 360 degrees, but in Ex-OR it is Π radians or 180 degrees.

ii) Better Capture, tracking & locking characteristics.

Edge triggered type of phase detector using RS Flip – Flop. It is formed from a pair of cross coupled NOR gates.

RS FF is triggered, i.e., the output of the detector changes its logic state on the positive edge of the inputs fIN & fOUT

✓ Monolithic Phase detector:

- It consists of 2 digital phase detector, a charge pump and an amplifier.
- Phase detector 1 is used in applications that require zero frequency and phase difference at lock.
- Phase detector 2, if quadrature lock is desired, when detector 1 is used in the main loop, detector can also be used to indicate whether the main loop is in lock or out of lock.

3.5.2 Low – Pass filter

The function of the LPF is to remove the high frequency components in the output of the phase detector and to remove the high frequency noise. LPF controls the characteristics of the phase locked loop. i.e., capture range, lock ranges, bandwidth

- Lock range(Tracking range):

The lock range is defined as the range of frequencies over which the PLL system follows the changes in the input frequency fIN.

- Capture range:

Capture range is the frequency range in which the PLL acquires phase lock. Capture range is always smaller than the lock range.

- Filter Bandwidth:

Filter Bandwidth is reduced, its response time increases. However reduced Bandwidth reduces the capture range of the PLL. Reduced Bandwidth helps to keep the loop in lock through momentary losses of signal and also minimizes noise.

3.5.4 Voltage Controlled Oscillator (VCO):

The third section of PLL is the VCO; it generates an output frequency that is directly proportional to its input voltage. The maximum output frequency of NE/SE 566 is 500 Khz.

3.5.5 Feedback path and optional divider:

Most PLLs also include a divider between the oscillator and the feedback input to the phase detector to produce a frequency synthesizer. A programmable divider is particularly useful in radio Transmitter applications, since a large number of transmit frequencies can be produced from a single stable, accurate, but expensive, quartz crystal–controlled reference oscillator. Some PLLs also include a divider between the reference clock and the reference input to the phase detector. If this divider divides by *M*, it allows the VCO to multiply the reference frequency by *N* / *M*. It might seem simpler to just feed the PLL a lower frequency, but in some cases the reference frequency may be constrained by other issues, and then the reference divider is useful. Frequency multiplication in a sense can also be attained by locking the PLL to the 'N'th harmonic of the signal. The equations governing a phase-locked loop with an analog multiplier as the phase detector may be derived as follows. Let the input to the phase detector be *xc*(*t*) and the output of the voltage- controlled oscillator (VCO) is *xr*(*t*) with frequency ω*r*(*t*), then the output of the phase detector *xm*(*t*) is given by

$$x_m(t) = x_c(t) \cdot x_r(t)$$

the VCO frequency may be written as a function of the VCO input *y*(*t*) as

$$\omega_r(t) = \omega_f + g_v y(t)$$

where *gv* is the *sensitivity* of the VCO and is expressed in Hz / V.

Hence the VCO output takes the form

$$x_r(t) = A_r \cos\left(\int_0^t \omega_r(\tau)\, d\tau\right) = A_r \cos(\omega_f t + \varphi(t))$$

where

$$\varphi(t) = \int_0^t g_v y(\tau)\, d\tau$$

The loop filter receives this signal as input and produces an output

$$xf(t) = F\text{filter}(xm(t))$$

where Filter is the operator representing the loop filter transformation.

When the loop is closed, the output from the loop filter becomes the input to the VCO thus

$$y(t) = xf(t) = F\text{filter}(xm(t))$$

We can deduce how the PLL reacts to a sinusoidal input signal:

$$x_C(t) = A_C \sin(\omega_C t).$$

The output of the phase detector then is:

$$x_m(t) = A_c \sin(\omega_c t) A_r \cos(\omega_f t + \varphi(t)).$$

This can be rewritten into sum and difference components using trigonometric identities:

$$x_m(t) = \frac{A_c A_f}{2} \sin(\omega_c t - \omega_f t - \varphi(t)) + \frac{A_c A_f}{2} \sin(\omega_c t + \omega_f t + \varphi(t))$$

As an approximation to the behaviour of the loop filter we may consider only the difference frequency being passed with no phase change, which enables us to derive a small-signal model Of the phase-locked loop. If we can make $\omega_f \approx \omega_c$ then the sin(.)can be approximated by its argument resulting in: $y(t) = x_f(t) \simeq -A_c A_f \varphi(t)/2$. The phase-locked loop is said to be locked if this is the case.

3.6 Control System Analysis/ Closed Loop Analysis Of PLL

Phase locked loops can also be analyzed as control systems by applying the Laplace transform. The loop response can be written as:

$$\frac{\theta_o}{\theta_i} = \frac{K_p K_v F(s)}{s + K_p K_v F(s)}$$

Where

- θo is the output phase in radians
- θi is the input phase in radians
- Kp is the phase detector gain in volts per radian
- Kv is the VCO gain in radians per volt-second
- $F(s)$ is the loop filter transfer function (dimensionless)

The loop characteristics can be controlled by inserting different types of loop filters. The simplest filter is a one-pole RC circuit. The loop transfer function in this case is:

filter is a one pole RC circuit. The loop transfer function in this case is:

$$F(s) = \frac{1}{1 + sRC}$$

The loop response becomes:

$$\frac{\theta_o}{\theta_i} = \frac{\frac{K_p K_v}{RC}}{s^2 + \frac{s}{RC} + \frac{K_p K_v}{RC}}$$

This is the form of a classic harmonic oscillator. The denominator can be related to that of a second order system:

$$s^2 + 2s\zeta\omega_n + \omega_n^2$$

Where

- ζ is the damping factor
- ωn is the natural frequency of the loop.

For the one-pole RC filter,

$$\omega_n - \sqrt{\frac{K_p K_v}{RC}}$$

$$\zeta = \frac{1}{2\sqrt{K_p K_v RC}}$$

The loop natural frequency is a measure of the response time of the loop, and the damping factor is a measure of the overshoot and ringing. Ideally, the natural frequency should be high and the damping factor should be near 0.707 (critical damping). With a single pole filter, it is not possible to control the loop frequency and damping factor independently. For the case of critical damping,

$$RC = \frac{1}{2K_p K_v}$$
$$\omega_c = K_p K_v \sqrt{2}$$

A slightly more effective filter, the lag-lead filter includes one pole and one zero. This can be realized with two resistors and one capacitor. The transfer function for this filter is

$$F(s) = \frac{1 + sCR_2}{1 + sC(R_1 + R_2)}$$

This filter has two time constants

$$\tau 1 = C(R1 + R2)\ \tau 2$$
$$= CR2$$

Substituting above yields the following natural frequency and damping factor

$$\omega_n - \sqrt{\frac{K_p K_v}{\tau_1}}$$

$$\zeta = \frac{1}{2\omega_n \tau_1} + \frac{\omega_n \tau_2}{2}$$

The loop filter components can be calculated independently for a given natural frequency and damping factor

$$\tau_1 = \frac{K_p K_v}{\omega_n^2}$$

$$\tau_2 = \frac{2\zeta}{\omega_n} - \frac{1}{K_p K_v}$$

Real world loop filter design can be much more complex eg using higher order filters to reduce various types or source of phase noise.

Applications of PLL:

The PLL principle has been used in applications such as

- FM stereo decoders
- motor speed control
- tracking filters

- FM modulation and demodulation
- FSK modulation
- Frequency multiplier
- Frequency synthesis etc.,

Example PLL ICs:560 series (560, 561, 562, 564, 565 & 567)

Analog Multiplier ICs

Analog multiplier is a circuit whose output voltage at any instant is proportional to the product of instantaneous value of two individual input voltages. Important applications of these multipliers are multiplication, division, squaring and square – rooting of signals, modulation and demodulation. These analog multipliers are available as integrated circuits consisting of op-amps and other circuit elements. The Schematic of a typical analog multiplier, namely, AD633 is shown in figure.

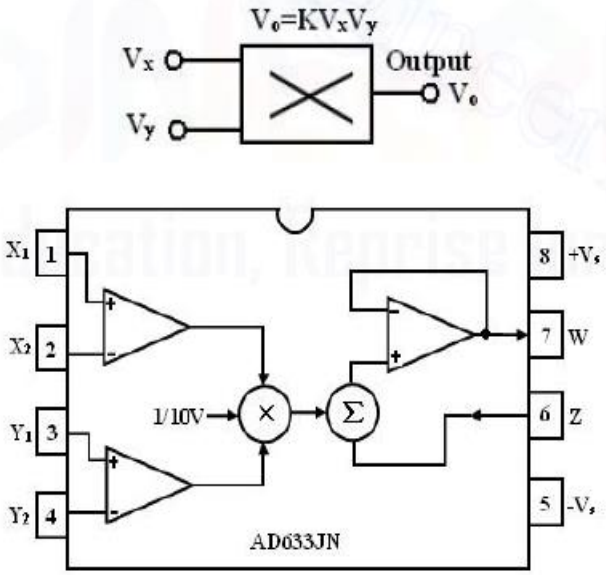


Fig. 3.10 Multiplier IC and its symbol

- The AD633 multiplier is a four – quadrant analog multiplier.
- It possesses high input impedance; this characteristic makes the loading effect on the signal source negligible.

- It can operate with supply voltages ranging from ±18V. The IC does not require external components.
- The typical range of the two input signals is ±10V.

Schematic representation of a multiplier:

The schematic representation of an analog multiplier is shown in figure. The output V0 is the product of the two inputs Vx and Vy is divided by a reference voltage Vref. Normally, the reference voltage Vref is internally set to 10V. Therefore, V0 =VxVy/10. In other words, the basic input – output relationship can be defined by KVx Vy when K = 1/10, a constant. Thus for peak input voltages of 10V, the peak magnitude of output voltage is 1/10 *10 *10 =10V. Thus, it can be noted that, as long as Vx < 10V and Vy < 10V, the multiplier output will not saturate.

Multiplier quadrants:

The transfer characteristics of a typical four-quadrant multiplier are shown in figure. Both the inputs can be positive or negative to obtain the corresponding output as shown in the transfer characteristics.

Applications of Multiplier ICs:

The multiplier ICs are used for the following purposes:

1. Voltage Squarer
2. Frequency doublers
3. Voltage divider
4. Square rooter
5. Phase angle detector
6. Rectifier

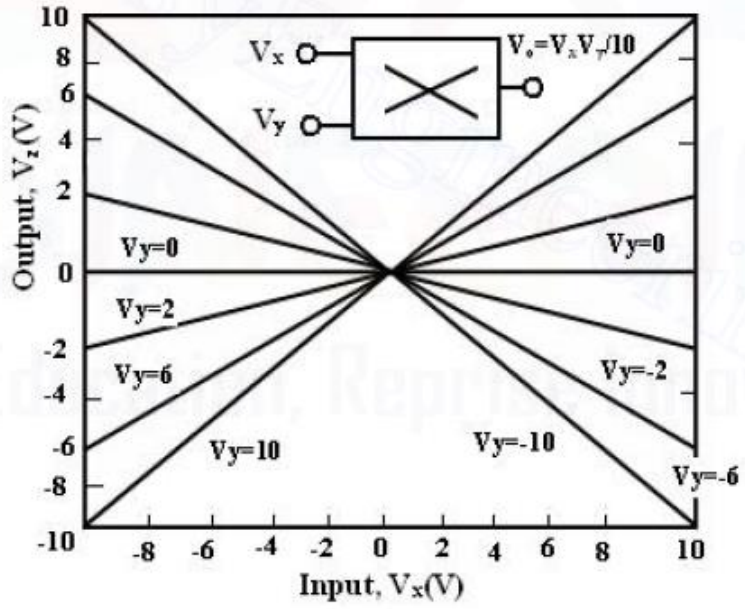


Fig.3.11 Transfer characteristics of a typical four-quadrant multiplier

Voltage Squarer:

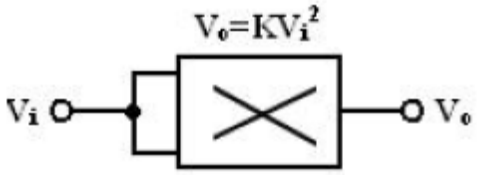


Fig. 3.12 voltage squarer circuit

Figure shows the multiplier IC connected as a squaring circuit. The inputs can be positive or negative, represented by any corresponding voltage level between 0 and 10V. The input voltage Vi to be squared is simply connected to both the input terminals, and hence we have, Vx = Vy = Vi and the output is V0 = KVi2. The circuit thus performs the squaring operation. This application can be extended for frequency doubling applications.

Frequency doublers:

Figure shows the squaring circuit connected for frequency doubling operation. A sine-wave signal Vi has a peak amplitude of Av and frequency of f Hz. Then, the output voltage of the doublers circuit is given by

$$v_0 = \frac{A_v \sin 2\pi ft * A_v \sin 2\pi ft}{10} = \frac{A_v^2}{10}\sin^2 2\pi ft = \frac{A_v^2}{20}(1 - \cos 4\pi ft)$$

Assuming a peak amplitude Av of 5V and frequency f of 10KHz, V0 =1.25–1.25 cos2 20000) t. The first term represents the dc term of 1.25V peak amplitude. The input and output waveforms are shown in figure. The output waveforms ripple with twice the input frequency in the rectified output of the input signal. This forms the principle of application of analog multiplier as rectifier of ac signals.

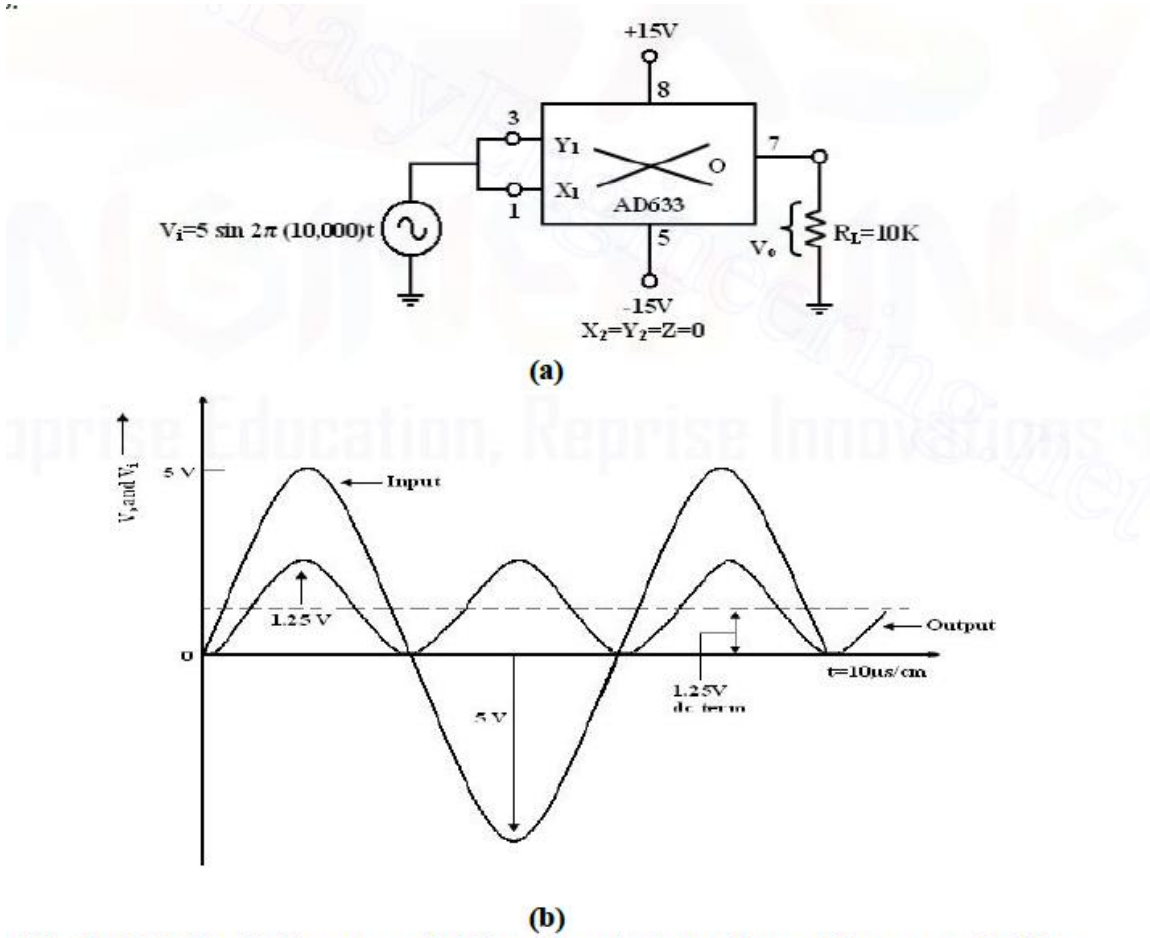


Fig. 3.13 (a) circuit diagram and (b) input –output waveform of frequency doubler

The dc component of output V0 can be removed by connecting a 1μF coupling capacitor between the output terminal and a load resistor, across which the output can be observed.

Voltage Divider:

In voltage divider circuit the division is achieved by connecting the multiplier in the feedback loop of an op-amp.

The voltages Vden and Vnum represent the two input voltages, Vdm forms one input of the multiplier, and output of op-amp VoA forms the second input.

The output VOA forms the second input. The output VOM of the multiplier is connected back of op- amp in the feedback loop. Then the characteristic operation of the multiplier gives

Vom = KVOA Vdm (1)

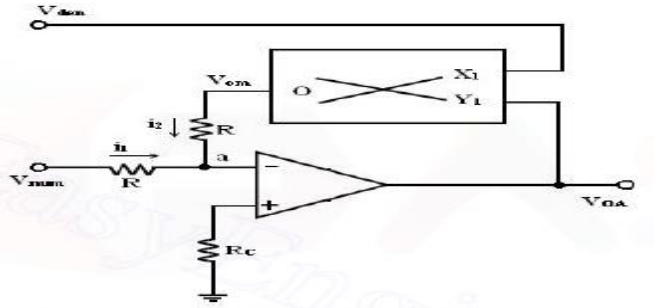


Fig 3.14 divider circuit

As shown in figure, no input signal current can flow into the inverting input terminal of op-amp, which is at virtual ground. Therefore, at the junction a, i1 +i2 =0, the current i1 = Vnum / R, where R is the input resistance and the current i2 = Vom /R. With virtual ground existing at a,

*i*1+*i*2 = Vnum / R + Vom /R = 0

KV OA V den = - V num or

$voA = -v_{num}/Kv_{den}$

where *Vnum* and *Vden* are the numerator and denominator voltages respectively. Therefore, the voltage division operation is achieved. *Vnum* can be a positive or negative voltage and *Vden* can have only positive values to ensure negative feedback. When *Vdm* is changed, the gain 10/*Vdm* changes, and this feature is used in automatic gain control (AGC) circuits.

✓ Square Rooter:

The divider voltage can be used to find the square root of a signal by connecting both inputs of the multiplier to the output of the op-amp. *Substituting* equal in magnitude but opposite in polarity (with respect to ground) to Vi. But we know that Vom is one- term (Scale factor) of V0 *

V0 or -Vi = Vom = V_2/1 0

Solving for V0 and eliminating √-1 yields. V0 = √10|Vi | Eqn. states that V0 equals the square root of 10 times the absolute magnitude of Vi. The input voltage Vi must be negative, or else,

the op-amp saturates. The range of Vi is between -1 and -10V. Voltages less than -1V will cause inaccuracies in the result. The diode prevents negative saturation for positive polarity Vi signals. For positive values of Vi the diode connections are reversed.

✓ Phase Angle detector:

The multiplier configured for phase angle detection measurement is shown in figure. When two sine-waves of the same frequency are applied to the inputs of the multiplier, the output V0 has a dc component and an AC component.

The trigonometric identity shows that Sin A sin B =1/2 (cos (A-B) – cos (A+B)).

When the two frequencies are equal, but with different phase angles, e.g. A=2πft +θ for signal Vx and B= 2πft for signal Vy, then using the identity [sin (2 *ft*+)][sin2 *ft*)]=1/2[cos -cos(4 *ft* +)]=1/2(dc- the double frequency term) Therefore, when the two input signals Vx and Vy are applied to the multiplier, V0 (dc) is given by

$$v_v(dc) = \frac{v_{xp}v_{yp}}{20}\cos\theta$$

where *Vxp* and *Vyp* are the peak voltage amplitudes of the signals Vx and Vy. Thus, the output V0(dc) depends on the factor cos θ. A dc voltmeter can be calibrated as a phase angle meter when the product of Vxp and Vyp is made equal to 20. Then, a (0-1) V range dc voltmeter can directly read cos θ, with the meter calibrated directly in degrees from a cosine table. The input and output waveforms are shown in figure.

Then the above eqn becomes V0 (dc) = cos θ, if we make the product Vxp Vyp = 20 or in other words, Vxp – Vyp = 4.47V.

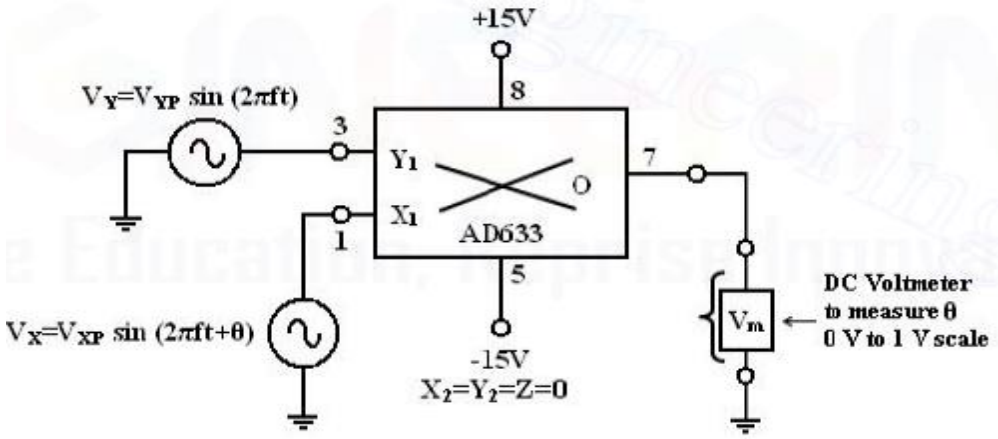


Fig 3.15 Phase angle measurement circuit diagram

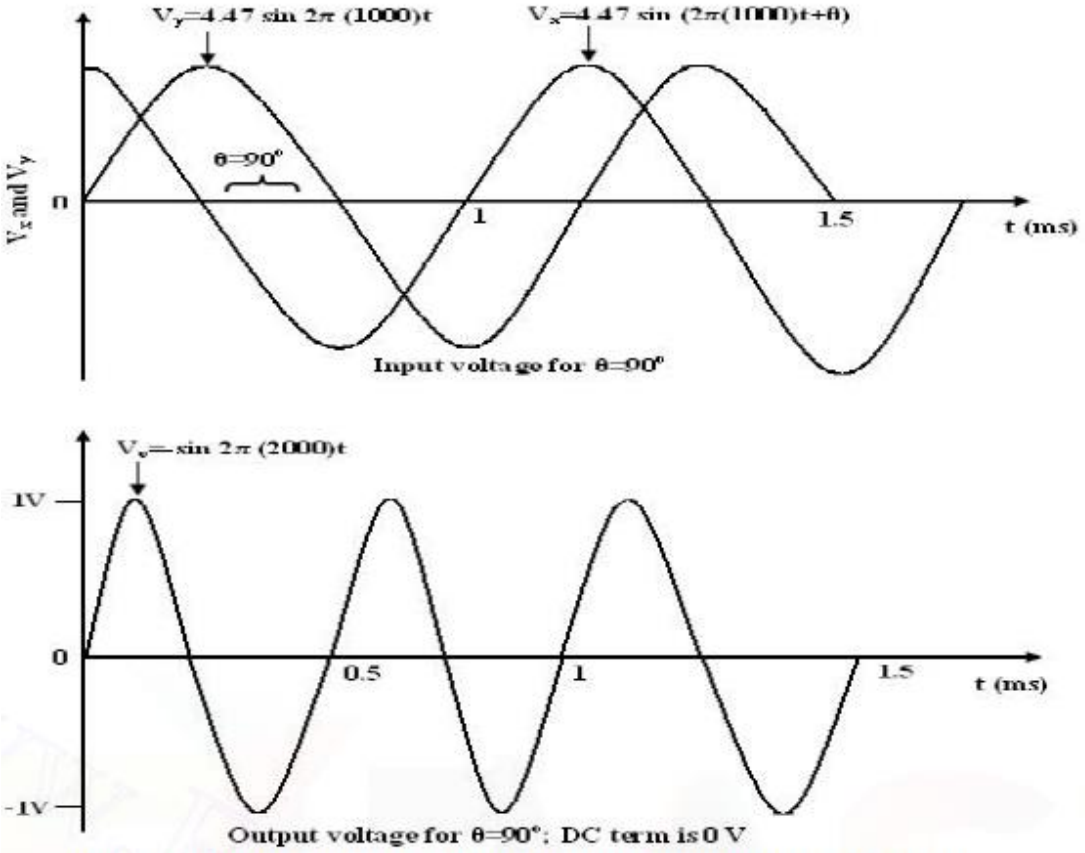


Fig. 3.16 input- output waveforms of phase angle detector