JEPPIAAR INSTITUTE OF TECHNOLOGY

"Self-Belief | Self Discipline | Self Respect"

DEPARTMENT

OF

ELECTRICAL AND ELECTRONICS ENGINEERING

LECTURE NOTES

EE8451 – LINEAR INTEGRATED CIRCUITS AND APPLICATIONS

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UNIT II CHARACTERISTICS OF OPAMP 9

Ideal OP-AMP characteristics, DC characteristics, AC characteristics, differential amplifier; frequency response of OP-AMP; Basic applications of op-amp – Inverting and Non-inverting Amplifiers, summer, differentiator and integrator-V/I & I/V converters.

Ideal op-amp characteristics:

✓ Infinite voltage gain A.

✓ Infinite input resistance Ri, so that almost any signal source can drive it and there is no loading of the proceeding stage.

✓ Zero output resistance Ro, so that the output can drive an infinite number of other devices.

✓ Zero output voltage, when input voltage is zero.

✓ Infinite bandwidth, so that any frequency signals from o to ∞ HZ can be amplified with out attenuation.

✓ Infinite common mode rejection ratio, so that the output common mode noise voltage is zero.

✓ Infinite slew rate, so that output voltage changes occur simultaneously with input voltage changes.

DC Characteristics of op-amp:

Current is taken from the source into the op-amp inputs respond differently to current and voltage due to mismatch in transistor.

DC output voltages are,

✓ Input bias current

✓ Input offset current

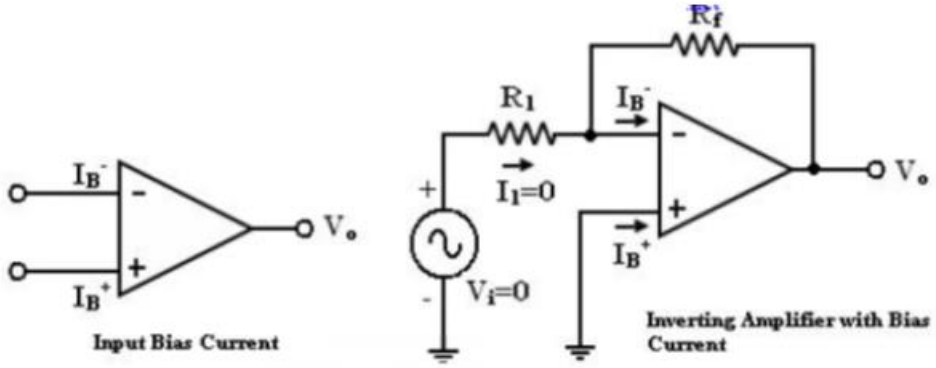
✓ Input offset voltage

✓ Thermal drift

Input bias current:

The op-amp‘s input is differential amplifier, which may be made of BJT or FET.

In an ideal op-amp, we assumed that no current is drawn from the input terminals the base currents entering into the inverting and non-inverting terminals (IB- & IB+ respectively). Even though both the transistors are identical, IB- and IB+ are not exactly equal due to internal imbalance between the two inputs. Manufacturers specify the input bias current I_B



If input voltage Vi = 0V. The output Voltage Vo should also be (Vo = 0) but for IB = 500Na We find that the output voltage is offset by Op-amp with a 1M feedback resistor Vo = 500nA X 1M = 500mV The output is driven to 500mV with zero input, because of the bias currents. In application where the signal levels are measured in mV, this is totally unacceptable. This can be compensated by a compensation resistor Rcomp has been added between the non-inverting input terminal and ground as shown in the figure below.

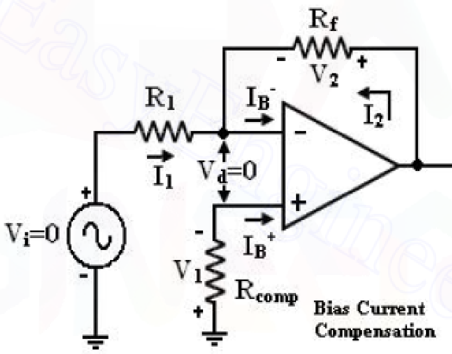


Fig. 1.22 Bias compensated circuit

Current I_B^+ flowing through the compensating resistor R_{comp}, then by KVL we get,

$-V_1+0+V_2-V_o = 0$ (or)

$V_o = V_2 - V_1$ --------- (1)

By selecting proper value of R_{comp}, V_2 can be cancelled with V_1 and the $V_o = 0$. The value of R_{comp} is derived as

$V_1 = I_B^+ R_{comp}$ (or)

$I_B^+ = V_1/R_{comp}$ ________________ (2)

The node 'a' is at voltage ($-V_1$). Because the voltage at the non-inverting input terminal is ($-V_1$). So with $V_i = 0$ we get,

$I_1 = V_1/R_1$ ----------------------- (3)

$I_2 = V_2/R_f$ ----------------------- (4)

For compensation, V_0 should equal to zero ($V_0 = 0$, $V_i = 0$). i.e. from equation (3) $V_2 = V_1$. So that, $I_2 = V_1/R_f$ ——> (5)

KCL at node 'a' gives,

$$I_B^- = I_2 + I_1 = (V_1/R_f) + (V_1/R_1) = V_1(R_1+R_f)/R_1R_f \text{ ----------------------- (5)}$$

Assume $I_B^- = I_B^+$ and using equation (2) & (5) we get

$$V_1 (R_1+R_f)/R_1R_f = V_1/R_{comp}$$

$$R_{comp} = R_1 \parallel R_f \text{ ----------------------- (6)}$$

i.e. to compensate for bias current, the compensating resistor, R_{comp} should be equal to the parallel combination of resistor R_1 and R_f.

Input offset current:

✓ Bias current compensation will work if both bias currents I_B^+ and I_B^- are equal.

✓ Since the input transistor cannot be made identical. There will always be some small difference between I_B^+ and I_B^-. This difference is called the offset current

$$|I_{os}| = I_B^+ - I_B^- \text{ ----------------------- (7)}$$

Offset current I_{os} for BJT op-amp is 200nA and for FET op-amp is 10pA. Even with bias current compensation, offset current will produce an output voltage when $V_i = 0$.

$$V_1 = I_B^+ R_{comp} \text{ ----------------------- (11)}$$

$$\text{And } I_1 = V_1/R_1 \text{ ----------------------- (12)}$$

KCL at node a gives,

$$I_2 = (I_B^- - I_1) = I_B^- - (I_B^+ \frac{R_{comp}}{R_1})$$

Again $V_0 = I_2 R_f - V_1$

$$V_o = I_2 R_f - I_B^+ R_{comp}$$

$$V_o = 1M\Omega \times 200nA$$

$$V_o = 200mV \text{ with } V_i = 0$$

Equation (16) the offset current can be minimized by keeping feedback resistance small.

✓ Unfortunately to obtain high input impedance, R1 must be kept large.

✓ R1 large, the feedback resistor Rf must also be high. So as to obtain reasonable gain. The T-feedback network is a good solution. This will allow large feedback resistance, while keeping the resistance to ground low (in dotted line).

✓ The T-network provides a feedback signal as if the network were a single feedback resistor.

By T to Π conversion,

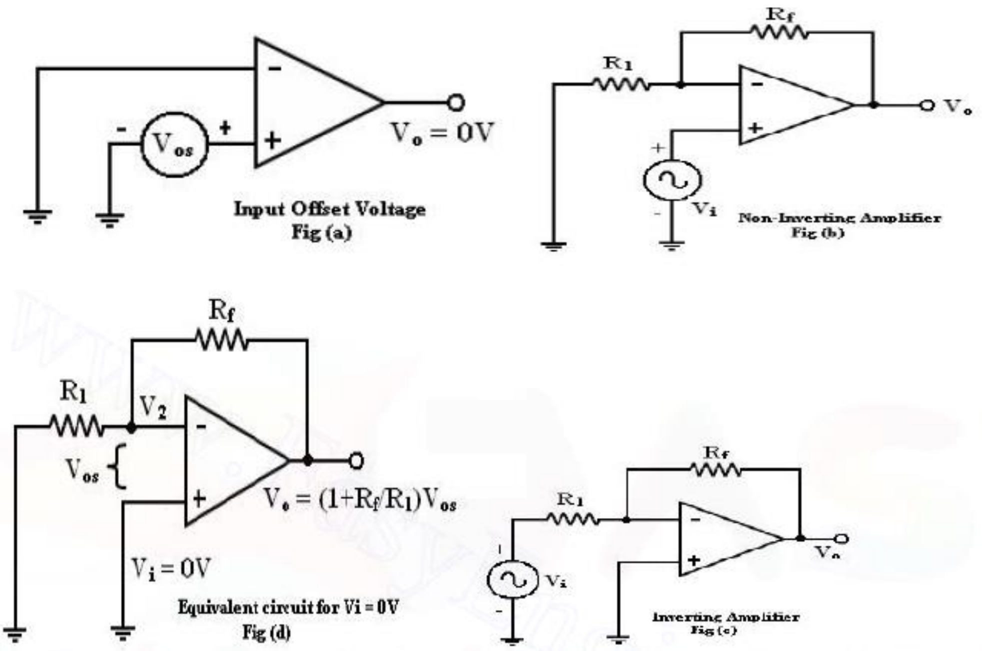
$$R_f = \frac{R_t^2 + 2R_tR_s}{R_s}$$

To design T- network first pick Rt<<Rf/2 and calculate

$$R_s = \frac{R_t^2}{R_f - 2R_t}$$

Input offset voltage:

In spite of the use of the above compensating techniques, it is found that the output voltage may still not be zero with zero input voltage [Vo ≠ 0 with Vi= 0]. This is due to unavoidable imbalances inside the op-amp and one may have to apply a small voltage at the input terminal to make output (Vo) = 0. This voltage is called input offset voltage Vos. This is the voltage required to be applied at the input for making output voltage to zero (Vo = 0).



Let us determine the V_{OS} on the output of inverting and non-inverting amplifier. If Vi = 0 (Fig (b) and (c)) become the same as in figure (d).

Total output offset voltage:

The total output offset voltage VOT could be either more or less than the offset voltage produced at the output due to input bias current (IB) or input offset voltage alone(Vos). This is because IB and Vos could be either positive or negative with respect to ground. Therefore the maximum offset voltage at the output of an inverting and non-inverting amplifier (figure b, c) without any compensation technique used is given by many op amps provide offset compensation pins to nullify the offset voltage. A 10K potentiometer is placed across offset null pins 1&5. The wipes connected to the negative supply at pin 4. The position of the wipes is adjusted to nullify the offset voltage.

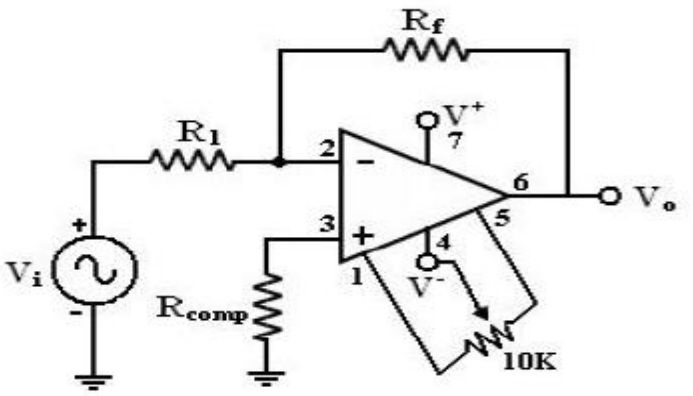


Fig.1.23 Compensation circuit for offset voltage

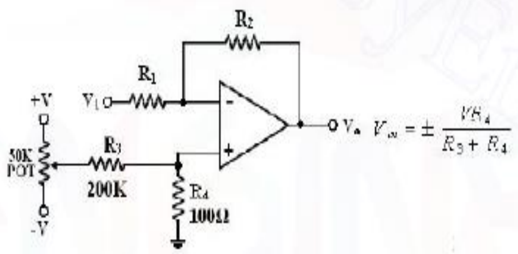
When the given (below) op-amps does not have these offset null pins, external balancing techniques are used.

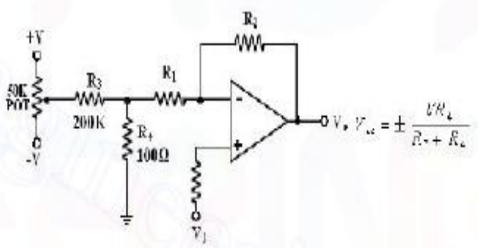
$$V_{OT} = \left(1 + \frac{R_f}{R_1}\right) V_{OS} + R_f I_B$$

With Rcomp, the total output offset voltage

$$V_{OT} = \left(1 + \frac{R_f}{R_1}\right) V_{OS} + R_f I_{OS}$$

Balancing circuit: Inverting amplifier: **Non-inverting amplifier:**





Thermal drift:

Bias current, offset current, and offset voltage change with temperature. A circuit carefully nulled at 25ºC may not remain. So when the temperature rises to 35ºC. This is called drift. Offset current drift is expressed in nA/ºC. These indicate the change in offset for each degree Celsius change in temperature.

Slew Rate

Slew rate is the maximum rate of change of output voltage with respect to time. Specified in V/µs.

Reason for Slew rate:

There is usually a capacitor within 0, outside an op-amp oscillation. It is this capacitor which prevents the o/p voltage from fast changing input. The rate at which the volt across the capacitor increases is given by

$$dVc/dt = I/C \text{ --------(1)}$$

I -> Maximum amount furnished by the op-amp to capacitor C.

Op-amp should have the either a higher current or small compensating capacitors.

For 741 IC, the maximum internal capacitor charging current is limited to about 15μA. So the slew rate of 741 IC is

$$SR = dVc/dt\,|_{max} = I_{max}/C$$

For a sine wave input, the effect of slew rate can be calculated as consider volt follower. The input is large amp, high frequency sine wave.

If Vs =Vm Sinwt then output V0 = Vm sinwt .

The rate of change of output is given by dV0/dt=Vm w coswt.

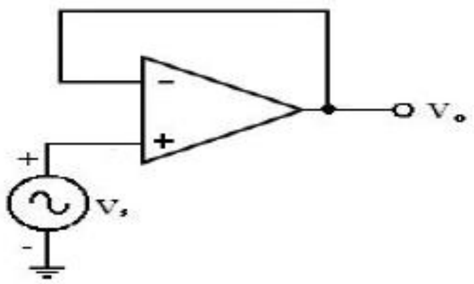


Fig. 1.22 Voltage Follower Circuit

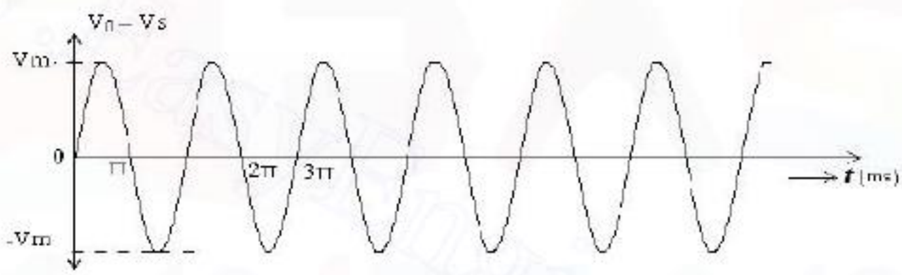


Fig. 1.23 Input and output waveforms of a voltage follower

The max rate of change of output across when coswt =1

(i.e) $SR = dV_0/dt\,|_{max} = wVm.$

$SR = 2\pi fVm$ V/s $= 2\pi fVm$ v/ms.

Thus the maximum frequency fmax at which undistorted output volt of peak value Vm is given by fmax (Hz) = Slew rate/6.28 * Vm called the full power response. It is maximum frequency of a large amplitude sine wave with which op-amp can have without distortion.

AC Characteristics:

For small signal sinusoidal (AC) application one has to know the ac characteristics such as frequency response and slew-rate.

Frequency Response:

The variation in operating frequency will cause variations in gain magnitude and its phase angle. The manner in which the gain of the op-amp responds to different frequencies is called the frequency response. Op-amp should have an infinite bandwidth BW =∞ (i.e.) if its open loop gain in 90dB with dc signal its gain should remain the same 90 dB through audio and onto high radio frequency. The op-amp gain decreases (roll-off) at higher frequency what reasons to decrease gain

after a certain frequency reached. There must be a capacitive component in the equivalent circuit of the op-amp. For an op-amp with only one break (corner) frequency all the capacitors effects can be represented by a single capacitor C. Below fig is a modified variation of the low frequency model with capacitor C at the output.

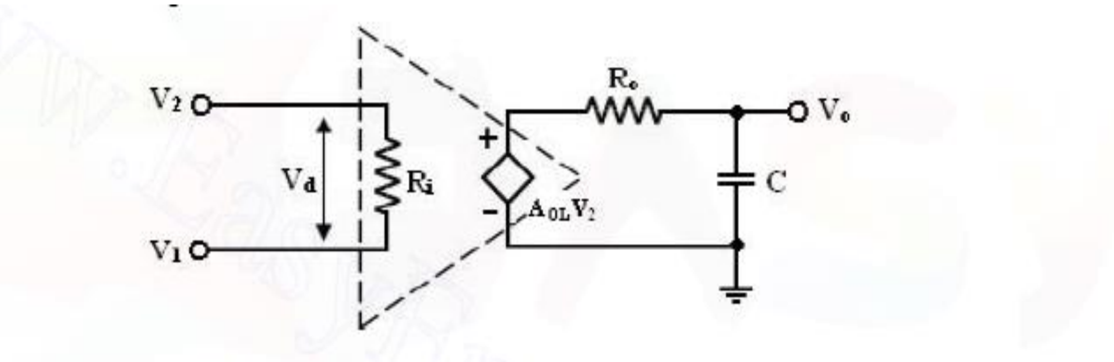


Fig 1.18 Equivalent circuit of practical circuit

There is one pole due to R0 C and one -20dB/decade. The open loop voltage gain of an op-amp with only one corner frequency is obtained from above fig. f1 is the corner frequency or the upper 3 dB frequency of the op-amp. The magnitude and phase angle of the open loop volt gain are f1 of frequency can be written as, The magnitude and phase angle characteristics:

1. For frequency f<< f_1 the magnitude of the gain is 20 log A_{OL} in db.
2. At frequency f = f_1 the gain in 3 dB down from the dc value of A_{OL} in db. This frequency f_1 is called corner frequency.
3. For f>> f_1 the fain roll-off at the rate off -20dB/decade or -6dB/decade.

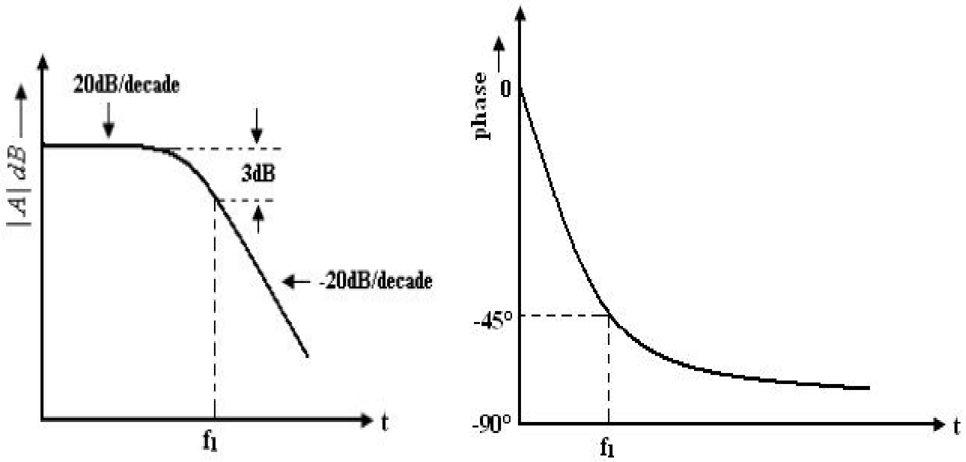


Fig 1.19 Frequency response of op amp

From the phase characteristics that the phase angle is zero at frequency f = 0. At the corner frequency f1 the phase angle is -45 (lagging and an infinite frequency the phase angle is -90 . It shows that a maximum of 90 phase change can occur in an op-amp with a single capacitor C. Zero frequency is taken as the decade below the corner frequency and infinite frequency is one decade above the corner frequency.

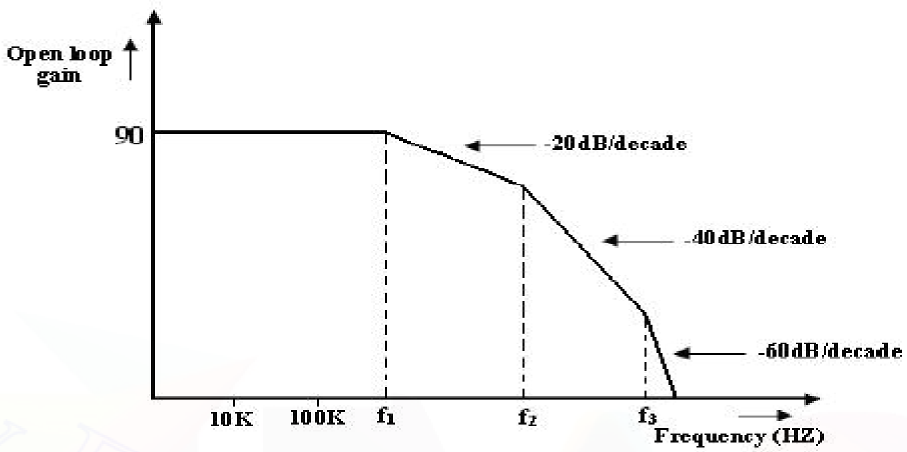


Fig. 1.20 Roll off rate of op amp gain

Circuit Stability:

A circuit or a group of circuit connected together as a system is said to be stable, if its o/p reaches a fixed value in a finite time. A system is said to be unstable, if its o/p increases with time instead of achieving a fixed value. In fact the o/p of an unstable sys keeps on increasing until the system break down. The unstable system is impractical and need be made stable. The criterion gn for stability is used when the system is to be tested practically. In theoretically, always used to test system for stability, ex: Bode plots. Bode plots are compared of magnitude Vs Frequency and phase angle Vs frequency. Any system whose stability is to be determined can represented by the block diagram.

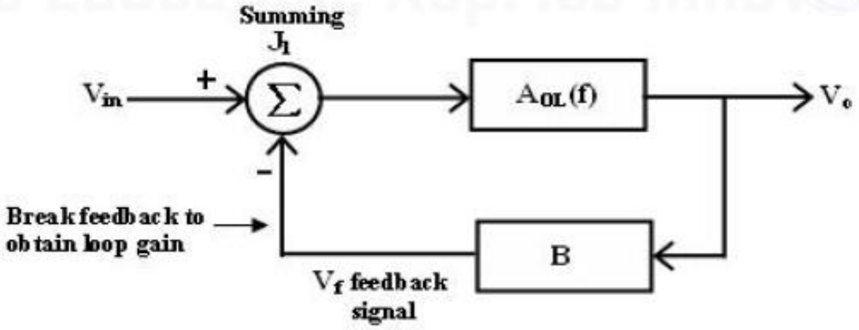


Fig. 1.21 Feedback loop system

The block between the output and input is referred to as forward block and the block between the output signal and f/b signal is referred to as feedback block. The content of each block is referred as transfer frequency. From fig. we represented it by AOL (f) which is given by

$$A_{OL}(f) = V_0 / V_{in} \text{ if } V_f = 0 \text{ ----- (1)}$$

where A_{OL} (f) = open loop volt gain.

The closed loop gain A_f is given by $A_F = V_0 / V_{in}$

$$= A_{OL} \;/\; (1+(A_{OL})(B) \quad \text{----(2)}$$

B = gain of feedback circuit.

B is a constant if the feedback circuit uses only resistive components.

Once the magnitude Vs frequency and phase angle Vs frequency plots are drawn, system stability may be determined as follows

1. Method 1:

Determine the phase angle when the magnitude of (AOL) (B) is 0dB (or) 1.

If phase angle is >-180 , the system is stable. However, the some systems the magnitude may never be 0, in that cases method 2, must be used.

2. Method 2:

Determine the phase angle when the magnitude of (AOL) (B) is 0dB (or) 1.

If phase angle is > - 180 , If the magnitude is –ve decibels then the system is stable. However, the some systems the phase angle of a system may reach -1800, under such conditions method 1 must be used to determine the system stability.

Closed – loop op-amp configuration:

The op-amp can be effectively utilized in linear applications by providing a feedback from the output to the input, either directly or through another network. If the signal feedback is out- of phase by 1800 with respect to the input, then the feedback is referred to as negative feedback or degenerative feedback. Conversely, if the feedback signal is in phase with that at the input, then the feedback is referred to as positive feedback or regenerative feedback. An op – amp that uses feedback is called a closed – loop amplifier. The most commonly used closed – loop amplifier configurations are 1. Inverting amplifier (Voltage shunt amplifier) 2. Non- Inverting amplifier (Voltage – series Amplifier)

Inverting Amplifier:

The inverting amplifier is shown in figure and its alternate circuit arrangement is shown in figure, with the circuit redrawn in a different way to illustrate how the voltage shunt feedback is achieved. The input signal drives the inverting input of the op – amp through resistor R1.The op – amp has an open – loop gain of A, so that the output signal is much larger than the error voltage. Because of the phase inversion, the output signal is 1800 out – of – phase with the input signal. This means that the feedback signal opposes the input signal and the feedback is negative or degenerative.

Practical Inverting amplifier:

The practical inverting amplifier has finite value of input resistance and input current, its open voltage gain A0 is less than infinity and its output resistance R0 is not zero, as against the ideal inverting amplifier with finite input resistance, infinite open – loop voltage gain and zero output resistance respectively. Figure shows the low frequency equivalent circuit model of a practical inverting amplifier. This circuit can be simplified using the Thevenin‘s equivalent circuit shown in figure. The signal source Vi and the resistors R1 and Ri are replaced by their Thevenin‘s equivalent values. The closed – loop gain AV and the input impedance Rif are calculated as follows. The input impedance of the op- amp is normally much larger than the input resistance R1. Therefore, we can assume Veq ≈ Vi and Req ≈ R1 . From the figure

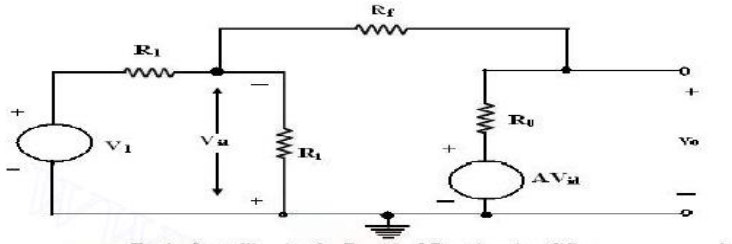
$$V_O = IR_O = AV_{id} \quad \text{and} \quad V_{id} = IR_f = AV_{id}$$

$$V_0 = IR_0 = AV_{id}$$

Substituting the value of I derived from above eqn. and obtaining the closed loop gain. It can be observed from above eqn. that when A>> 1, R0 is negligibly small and the product AR1 >> R0 +Rf , the closed loop gain is given by

$$Av = -\frac{R_f}{R_1}$$

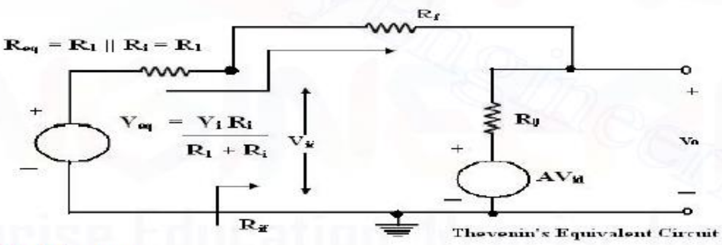
Which as the same form as given in above eqn for an ideal inverter.



Equivalent Circuit of a Practical Inerting Amplifier

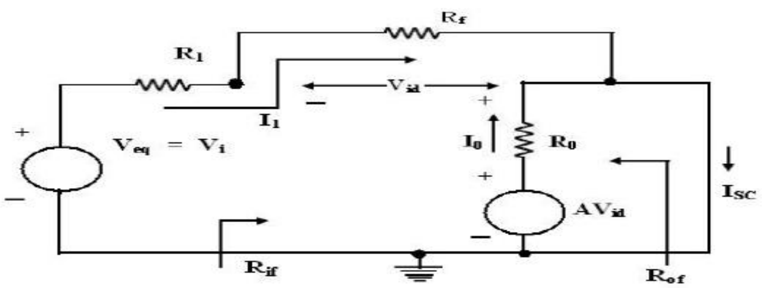
Input Resistance:

$R_{if} = V_{id}/I_1 = (R_f+R_0)/(1+A)$



Thevenin's Equivalent Circuit

Output Resistance:



Equivalent circuit to determine Rof

Figure shows the equivalent circuit to determine Rof. The output impedance Rof without the load resistance factor RL is calculated from the open circuit output voltage Voc and the short circuit output current ISC.

$$R_{of} = \frac{\dfrac{R_0(R_1 + R_f)}{R_0 + R_1 + R_f}}{1 + \dfrac{R_1 A}{R_0 + R_1 + R_f}}$$

Non –Inverting Amplifier:

The non – inverting Amplifier with negative feedback is shown in figure. The input signal drives the non – inverting input of op-amp. The op-amp provides an internal gain A. The external resistors R1 and Rf form the feedback voltage divider circuit with an attenuation factor of β. Since the feedback voltage is at the inverting input, it opposes the input voltage at the non – inverting input terminals, and hence the feedback is negative or degenerative. The differential voltage Vid at the input of the op-amp is zero, because node A is at the same voltage as that of the non- inverting input terminal. As shown in figure, Rf and R1 form a potential divider. Therefore,

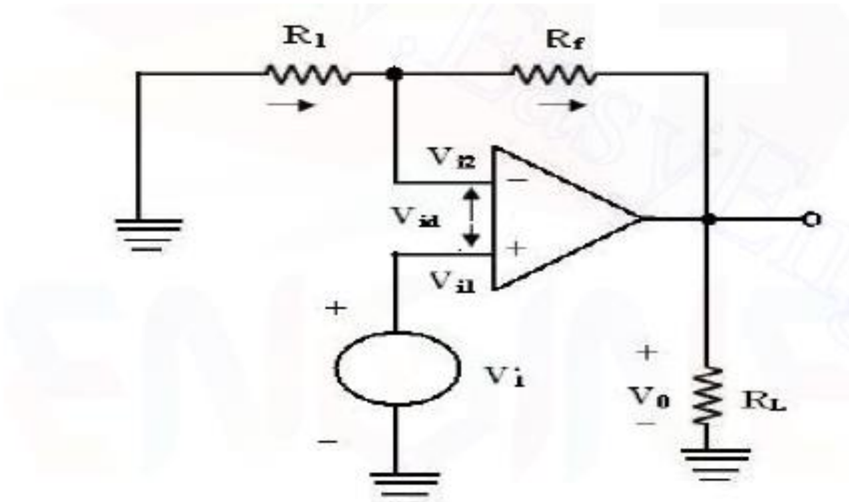


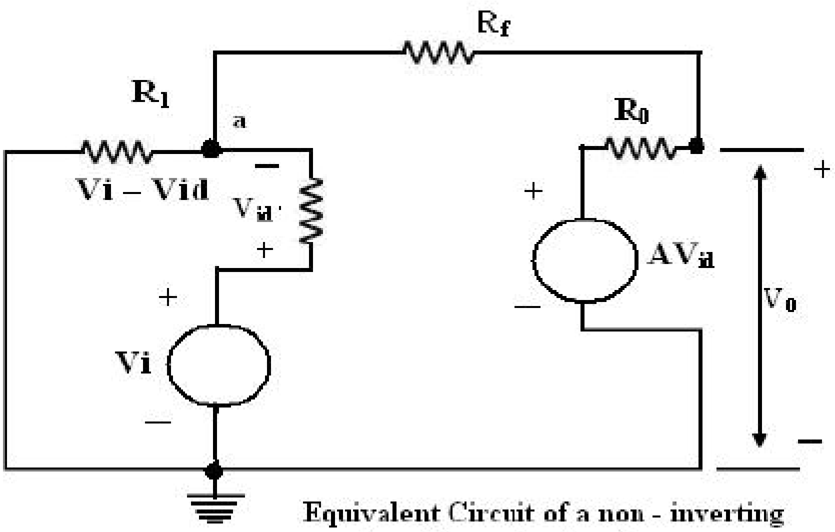
Fig. 1.24 Non –Inverting Amplifier:

Closed Loop Non – Inverting Amplifier

The input resistance of the op – amp is extremely large (approximately infinity,) since the op – amp draws negligible current from the input signal.

Practical Non –inverting amplifier:

The equivalent circuit of a non- inverting amplifier using the low frequency model is shown below in figure. Using Kirchhoff's current law at node a,



Equivalent Circuit of a non - inverting Amplifier using low frequency

$$Av = 1 + \frac{R_f}{R_1}$$

The difference volt is equal to the input volt minus the f/b volt. (or) The feedback volt always opposes the input volt (or out of phase by 1800 with respect to the input voltage) hence the feedback is said to be negative.

It will be performed by computing

1. Closed loop volt gain
2. Input and output resistance
3. Bandwidth

1. Closed loop voltage gain:

The closed loop volt gain is AF = V0 /Vin

V0 = Avid =A(V1 –V2)

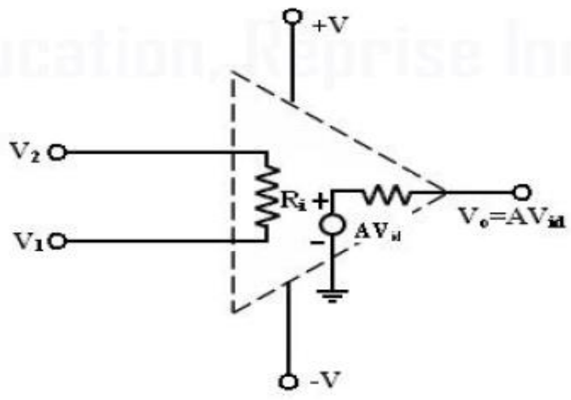


Fig.1.25 equivalent circuit of practical op amp

A = large signal voltage gain.

From the above eqn.

V0 = A(V1 – V2)

Refer fig, we see that,

$$V_1 = V_{in}$$

$$V_2 = V_f = \frac{R_1}{R_1+R_f} V_0 \quad \text{Since } R_i >> R_1$$

$$V_0 = AV_{in} - \frac{R_1 V_0}{R_1+R_f}$$

$$V_0 + \frac{R_1}{R_1+R_f} V_0 = AV_{in}$$

SUMMER/ADDER

Op-amp may be used to design a circuit whose output is the sum of several input signals. Such a circuit is called a summing amplifier or a summer or adder. An inverting summer or a non-inverting summer may be discussed now.

Inverting Summing Amplifier:

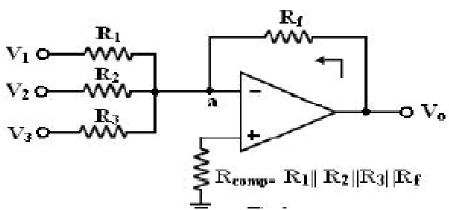


Fig. 2.13 inverting summer

A typical summing amplifier with three input voltages V1, V2 and V3 three input resistors R1, R2, R3 and a feedback resistor Rf is shown in figure 2.

The following analysis is carried out assuming that the op-amp is an ideal one, AOL= ∞. Since the input bias current is assumed to be zero, there is no voltage drop across the resistor Rcomp and hence the non-inverting input terminal is at ground potential.

$I= V_1/R_1+V_2/R_2\ldots..+V_n/R_n$;

$V_o= - R_f\, I=R_f/R(V_1+V_2+\ldots.V_n)$.

To find Rcomp, make all inputs V1 = V2 = V3 = 0.

So the effective input resistance Ri = R1 || R2 || R3.

Therefore, Rcomp = Ri || Rf = R1 || R2 || R3 || R,f.

Non-Inverting Summing Amplifier:

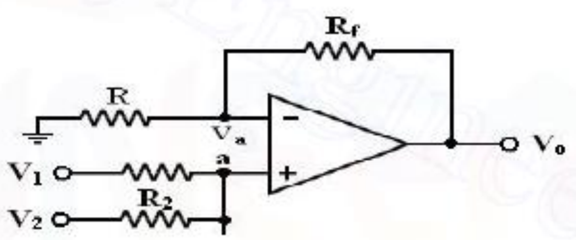


Fig.2.14 Non inverting summer

A summer that gives a non-inverted sum is the non-inverting summing amplifier of figure Let the voltage at the (-) input terminal be Va. which is a non-inverting weighted sum of inputs.

Let R1 = R2 = R3 = R = Rf/2, then Vo = V1+V2+V3

Subtractor:

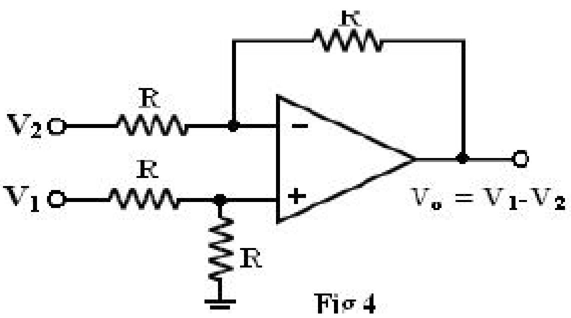


Fig. 2.15 Subtractor

A basic differential amplifier can be used as a subtractor as shown in the above figure. If all resistors are equal in value, then the output voltage can be derived by using superposition principle. To find the output V01 due to V1 alone, make V2 = 0.

Then the circuit of figure as shown in the above becomes a non-inverting amplifier having input voltage V1/2 at the non-inverting input terminal and the output becomes

$V_{01} = V_1/2(1+R/R) = V1$ when all resistances are R in the circuit.

Similarly the output V02 due to V2 alone (with V1 grounded) can be written simply for an inverting amplifier as

$V_{02} = -V_2$

Thus the output voltage Vo due to both the inputs can be written as

$V_0 = V01 - V02 = V1 - V2$

Adder/Subtractor:

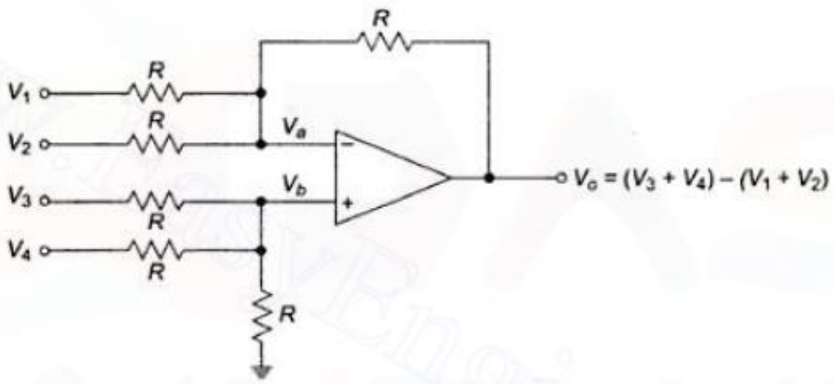


Fig. 2.16 Adder-Subtractor

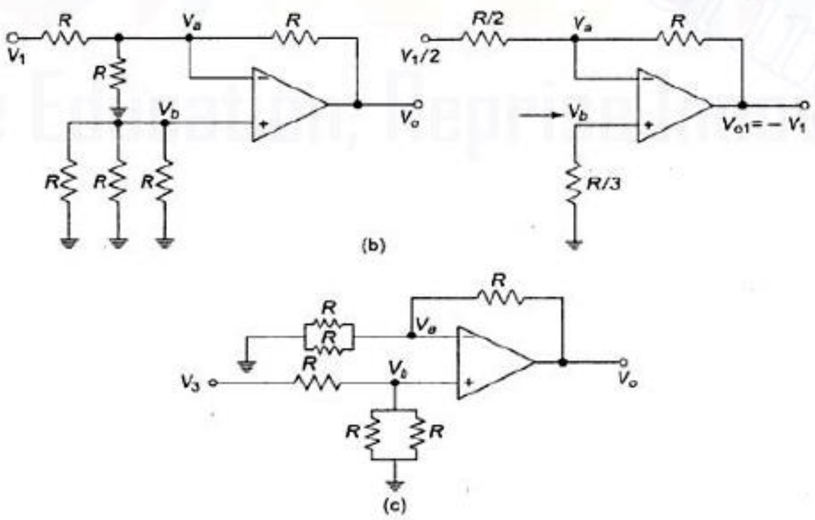


Fig. 2.17 (b) equivalent circuit for $V_2=V_3=V_4=0$ and (c) for $V_1=V_2=V_4=0$

It is possible to perform addition and subtraction simultaneously with a single op-amp using the circuit shown in figure 2.16.

The output voltage Vo can be obtained by using superposition theorem. To find output voltage V01 due to V1 alone, make all other input voltages V2, V3 and V4 equal to zero. The simplified circuit is shown in figure 2.17. This is the circuit of an inverting amplifier and its output voltage is, $V_{01} = -R/(R/2) * V_1/2 = -V_1$ by Thevenin‘s equivalent circuit at inverting input terminal).

Similarly, the output voltage V02 due to V2 alone is,

$V_{02} = -V_2$

Now, the output voltage V03 due to the input voltage signal V3 alone applied at the (+) input terminal can be found by setting V1, V2 and V4 equal to zero.

$V_{03} = V_3$

The circuit now becomes a non-inverting amplifier as shown in fig.(c).

So, the output voltage V03 due to V3 alone is

V03 = V3

Similarly, it can be shown that the output voltage V04 due to V4 alone is

$V04 = V4$

Thus, the output voltage Vo due to all four input voltages is given by

$Vo = V01 = V02 = V03 = V04$

$Vo = -V1 - V2 + V3 + V4$

$V o = (V 3 + V 4) - (V1 + V 2)$

So, the circuit is an adder-subtractor.

Integrator:

A circuit in which the output voltage waveform is the integral of the input voltage waveform is the integrator or Integration Amplifier. Such a circuit is obtained by using a basic inverting amplifier configuration if the feedback resistor RF is replaced by a capacitor CF. The expression for the output voltage V0 can be obtained by KVL eqn. at node V2.

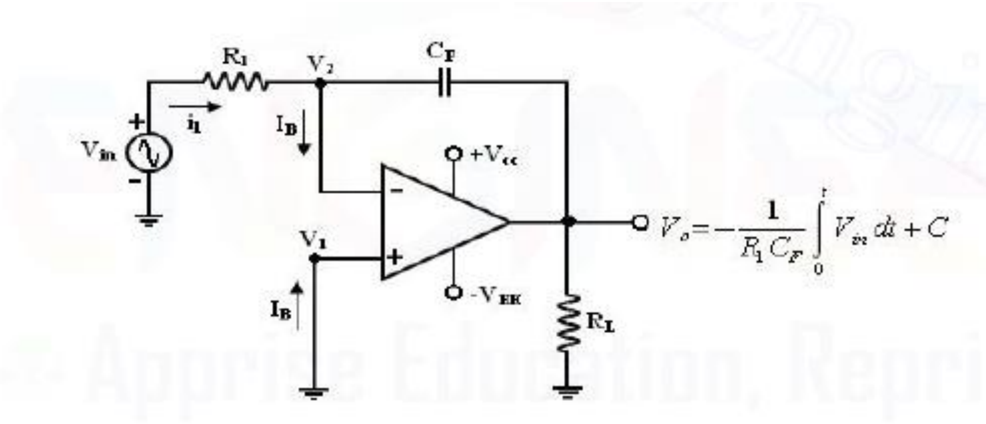


Fig 2.21 Integrator Circuit

$$i_1 = I_B + i_f$$

Since I_B is negligible small, $i_1 = i_F$

Relation between current through and voltage across the capacitor is

iC (t) = Cdvc(t)/dt

V 1=0 because A is very large,

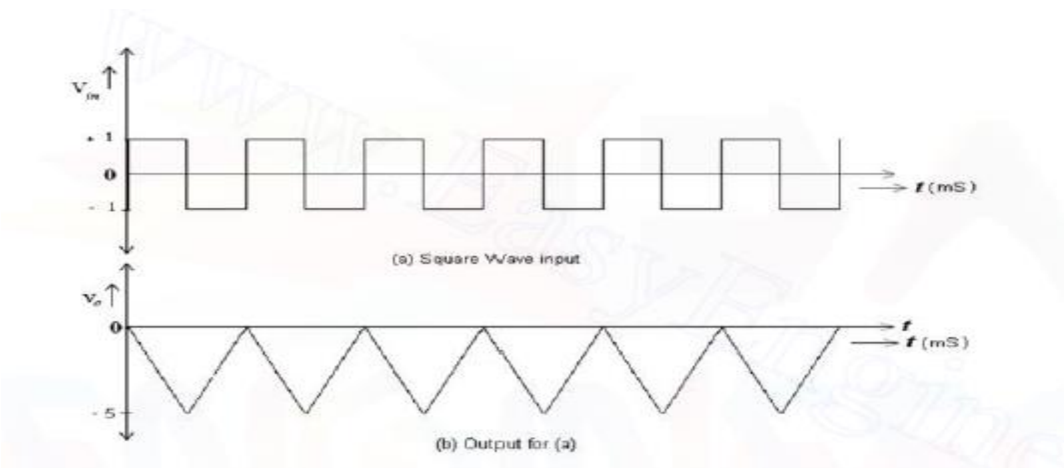
The output voltage can be obtained by integrating both sides with respect to time

$$V_0(jw) = \frac{1}{jwR_1C_f} V_i\ (jw)$$

Indicates that the output is directly proportional to the negative integral of the input volts and inversely proportional to the time constant R1 CF.

Ex: If the input is sine wave -> output is cosine wave.

If the input is square wave -> output is triangular wave.



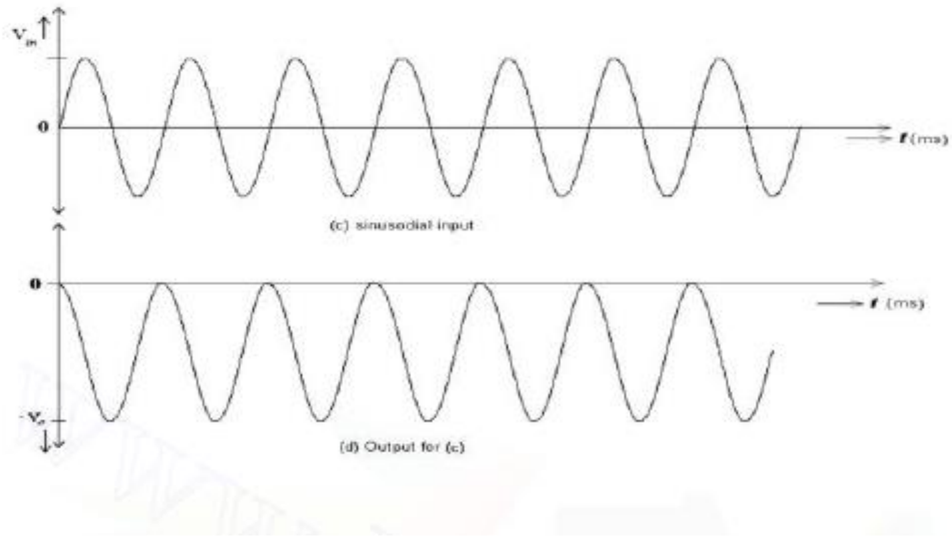


Fig.2.22 Waveforms from Integrator

These waveform with assumption of R1 Cf = 1, Vout =0V (i.e) C =0.

When Vin = 0 the integrator works as an open loop amplifier because the capacitor CF acts an open circuit to the input offset voltage Vio. The Input offset voltage V_{io} and the part of the input is charging capacitor CF produce the error voltage at the output of the integrator.

Practical Integrator:

Practical Integrator to reduce the error voltage at the output, a resistor RF is connected across the feedback capacitor CF. Thus RF limits the low frequency gain and hence minimizes the variations in the output voltages. The frequency response of the basic integrator, shown from this fb is the frequency at which the gain is dB and is given by

$$f_b = \frac{1}{2\pi R_1 C_F}$$

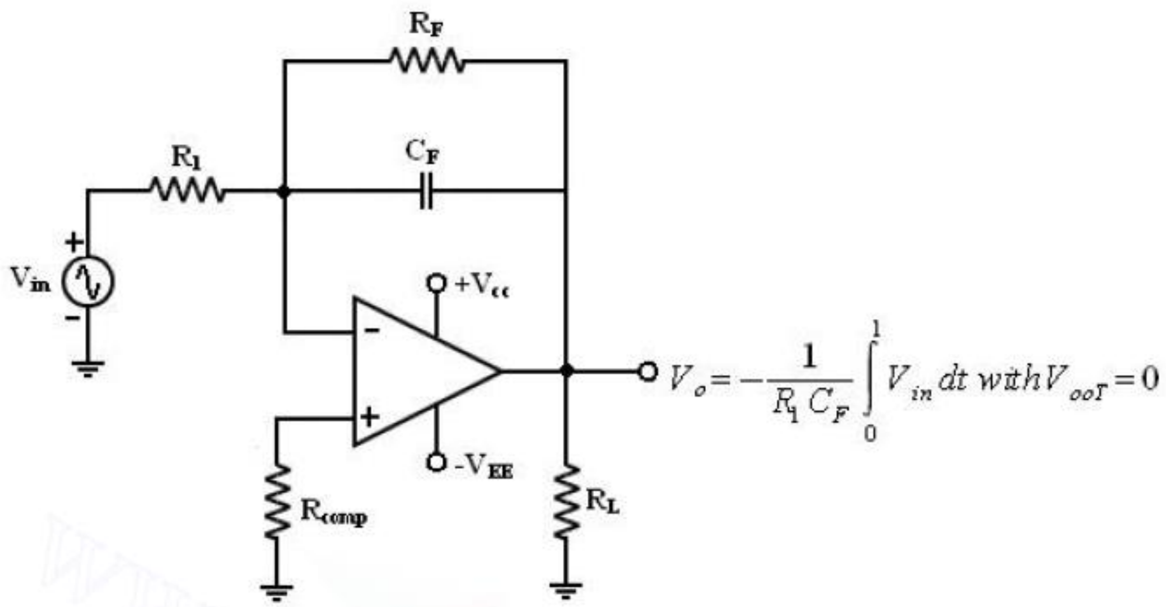


Fig. 2.23 Practical Integrator Circuit

• Both the stability and low frequency roll-off problems can be corrected by the addition of a resistor RF in the practical integrator.

• Stability refers to a constant gain as frequency of an input signal is varied over a certain range.

• Low frequency -> refers to the rate of decrease in gain roll off at lower frequencies.

• From the fig of practical Integrators, f is some relative operating frequency and for frequencies f to fa to gain RF / R1 is constant. After fa the gain decreases at a rate of 20dB/decade or between fa and fb the circuit act as an integrator.

• The gain limiting frequency fa is given by

$$f_a = \frac{1}{2\pi R_1 C_F}$$

• The value of fa and R1 CF and RF CF values should be selected such that fa<fb.

• The input signal will be integrated properly if the time period T of the signal is larger than or equal to RF CF,

$$f_b = \frac{1}{2\pi R_F C_F}$$

Uses:

Most commonly used in

- ✓ analog computers
- ✓ ADC
- ✓ Signal wave shaping circuits.

2.10 Differentiator:

The circuit performs the mathematical operation of differentiation (i.e.) the output waveform is the derivative of the input waveform. The differentiator may be constructed from a basic inverting amplifier if an input resistor R1is replaced by a capacitor C1. Since the differentiator performs the reverse of the integrator function. Thus the output V0 is equal to RF C1 times the negative rate of change of the input voltage Vin with time. The –sign indicates a 180 phase shift of the output waveform V0 with respect to the input signal. The below circuit will not do this because it has some practical problems. The gain of the circuit (RF /XC1) R with R in frequency at a rate of 20dB/decade. This makes the circuit unstable. Also input impedance XC1s with R in frequency which makes the circuit very susceptible to high frequency noise.

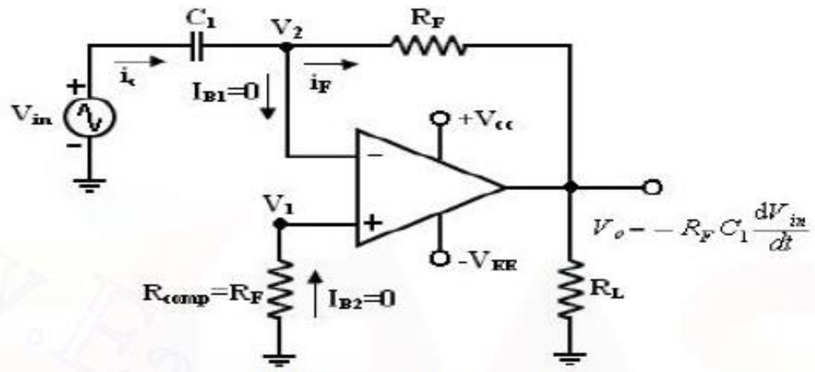


Fig 2.24 Basic Differentiator

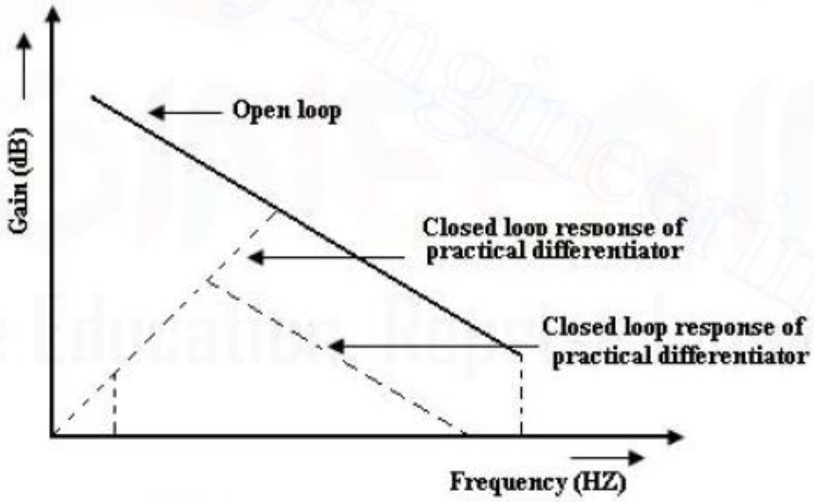


Fig. 2.25 Frequency response of differentiator

From the above fig. fa = frequency at which the gain is 0dB and is given by

$$f_a = \frac{1}{2\pi R_f C_1}$$

Both stability and high frequency noise problems can be corrected by the addition of two components. R_1 and C_F. This circuit is a practical differentiator. From Frequency fa to feedback the gain Rs at 20dB/decade after feedback the gain S at 20dB/decade. This 40dB/ decade change in gain is caused by the $R_1 C_1$ and $R_F C_F$ combinations.

The gain limiting frequency f_b is given by,

$$f_b = \frac{1}{2\pi R_1 C_1}$$

Where $R_1 C_1 = R_F C_F$

$R_1 C_1$ and $R_F C_F$ help to reduce the effect of high frequency input, amplifier noise and offsets. All R1 C1 and RF CF make the circuit more stable by preventing the R in gain with frequency. The input signal will be differentiated properly, if the time period T of the input signal is larger than or equal to $R_F C_1$ (i.e) T > $R_F C_1$ generally, the value of Feedback and in turn $R_1 C_1$ and $R_F C_F$ values should be selected such that

$R_F C_1 >> R_1 C_1$

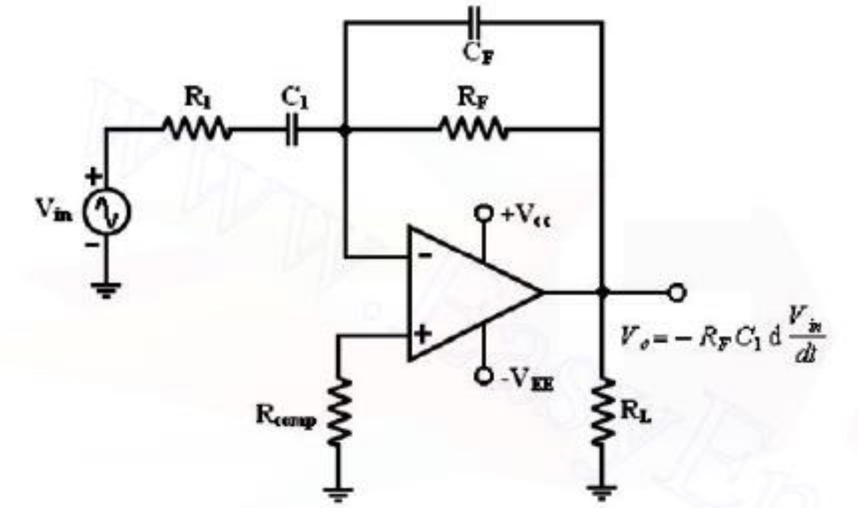


Fig 2.26 Practical Differentiator

A workable differentiator can be designed by implementing the following steps.

1. Select f_a equal to the highest frequency of the input signal to be differentiated then assuming a value of $C_1 < 1\mu f$. Calculate the value of RF.

2. Choose $f_b = 20 f_a$ and calculate the values of R_1 and C_F so that $R_1 C_1 = R_F C_F$.

Uses:

It is used in wave shaping circuits to detect high frequency components in an input signal and alsoas a rate of change and detector in FM modulators.

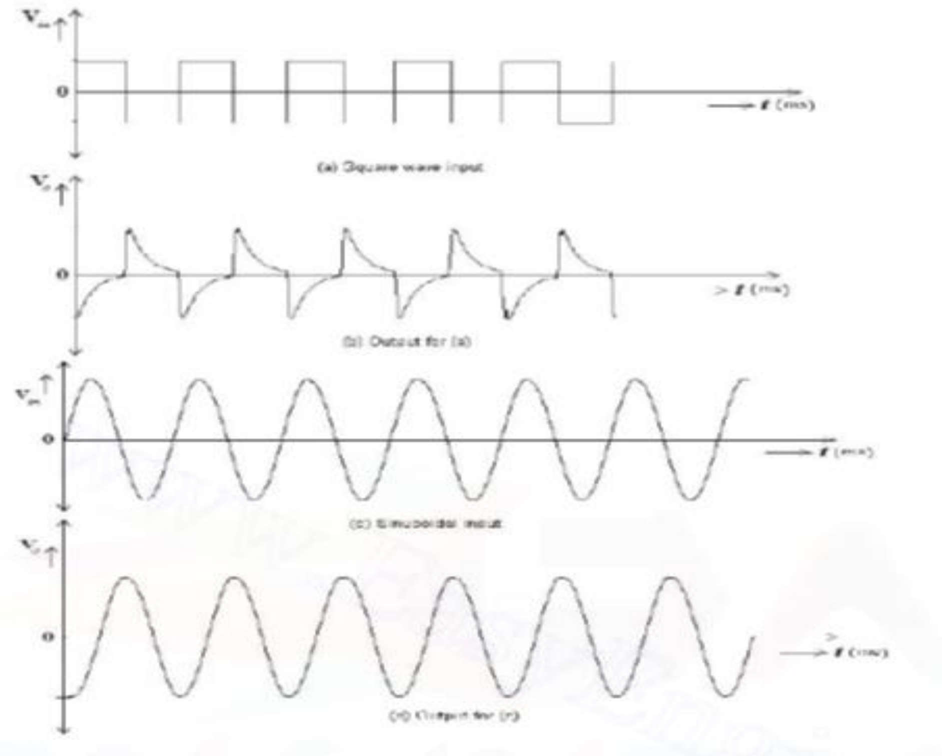


Fig.2.27 Output for practical differentiator.

VOLTAGE FOLLOWER:

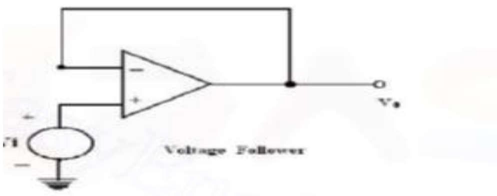


Fig 2.6 Voltage follower

If R1=∞ and R_f =0 in the non inverting amplifier configuration. The amplifier act as a unity-gain amplifier or voltage follower. The circuit consists of an op-amp and a wire connecting the output voltage to the input, i.e. the output voltage is equal to the input voltage, both in magnitude and phase. V0=Vi. Since the output voltage of the circuit follows the input voltage, the circuit is called voltage follower. It offers very
high input impedance of the order of MΩ and very low output impedance.
Therefore, this circuit draws negligible current from the source. Thus, the voltage follower can be used as a buffer between a high impedance source and a low impedance load for impedance matching applications.

2.5 Voltage to Current Converter with floating loads (V/I):

Voltage to current converter in which load resistor RL is floating (not connected to ground). V_{in} is applied to the non- inverting input terminal, and the feedback voltage across R1 devices the inverting input terminal. This circuit is also called as a current – series negative feedback amplifier. Because the feedback voltage across R1 (applied Non-inverting terminal) depends on the output current i0 and is in series with the input difference voltage Vid.

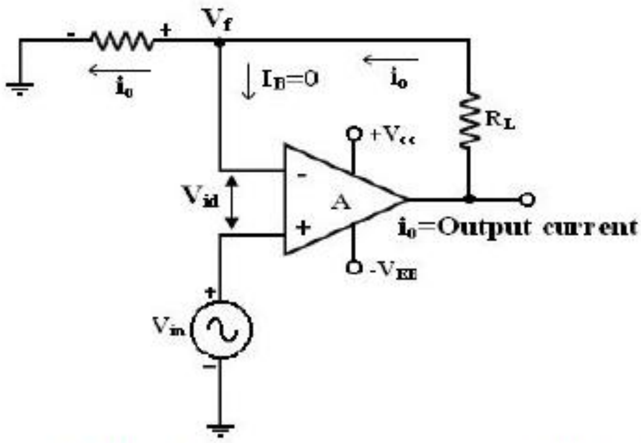


Fig. 2.7 Voltage to Current Converter with floating loads (V/I):

Writing KVL for the input loop,

Voltage $V_{id} = V_f$ and $I_B = 0$, $V_i = R_L i_o$ where $i_o = \frac{V_i}{R_L}$

From the fig input voltage Vin is converted into output current of Vin/R_L [Vin -> i0].

In other words, input volt appears across R1. If R_L is a precision resistor, the output current (i0 = Vin/R1) will be precisely fixed.

Applications:

1. Low voltage ac and dc voltmeters
2. Diode match finders
3. LED and Zener diode testers.

Voltage – to current converter with Grounded load:

This is the other type V – I converter, in which one terminal of the load is connected to ground.

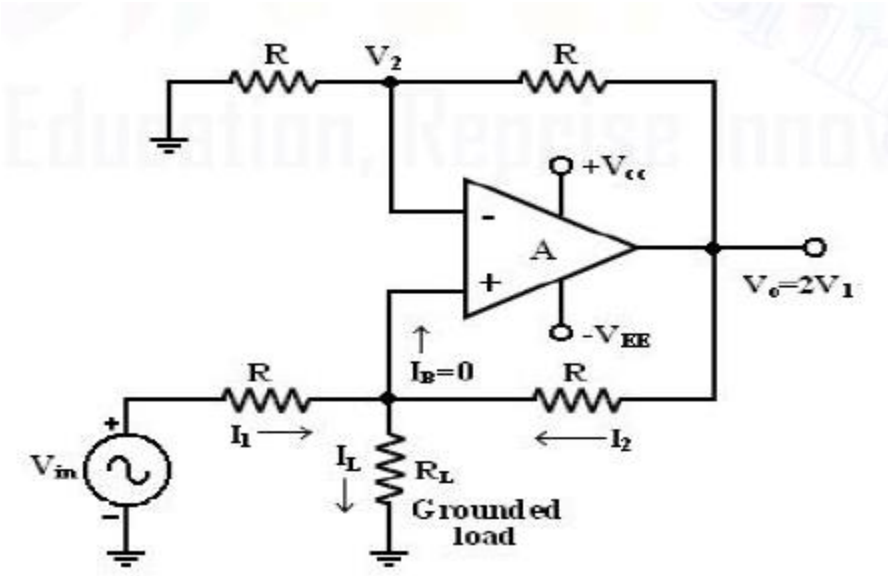


Fig 2.8 V – I converter with grounded load

Analysis of the circuit:

The analysis of the circuit can be done by following 2 steps.

1. To determine the voltage V1 at the non-inverting (+) terminals and

2. To establish relationship between V1 and the load current IL. Applying KCL at node a,

$$R = R_f$$
$$I_1 + I_2 = I_L$$
$$(V_i + V_a)/R + (V_o - V_a)/R = I_L$$
$$V_o = (V_i + V_o - I_L R)/2 \text{ and gain } = 1 + R/R = 2.$$
$$\therefore V_i = I_L R \ ; I_L = V_i/R$$

Current to Voltage Converter (I –V):

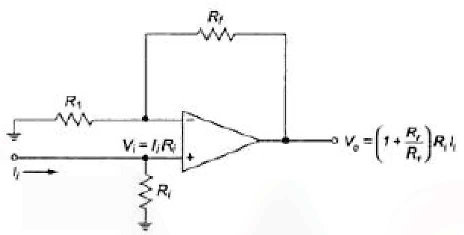


Fig. 2.9 Non inverting current to voltage convertor

Open – loop gain A of the op-amp is very large. Input impedance of the op amp is very high.

Sensitivity of the I – V converter:

1. The output voltage V0 = -RF Iin.

2. Hence the gain of this converter is equal to -RF. The magnitude of the gain (i.e.) is called as sensitivity of I to V converter.

3. The amount of change in output volt ΔV0 for a given change in the input current ΔI_{in} is decide by the sensitivity of I-V converter.

4. By keeping RF variable, it is possible to vary the sensitivity as per the requirements.

Applications of V-I converter with Floating Load:

1. Diode Match finder:

In some applications, it is necessary to have matched diodes with equal voltage drops at a particular value of diode current. The circuit can be used in finding matched diodes and is obtained from fig (V-I converter with floating load) by replacing RL with a diode. When the switch is in position 1: (Diode Match Finder) Rectifier diode (IN 4001) is placed in the f/b loop, the current through this loop is set by input voltage Vin and Resistor R1. For Vin = 1V and R1 = 100Ω, the current through this I0 = Vin/R1 = 1/100 = 10mA. As long as V0 and R1 constant, I0 will be constant. The Voltage drop across the diode can be found either by measuring the volt across it or o/p voltage.

The output voltage is equal to (Vin +VD) V0= Vin + VD.

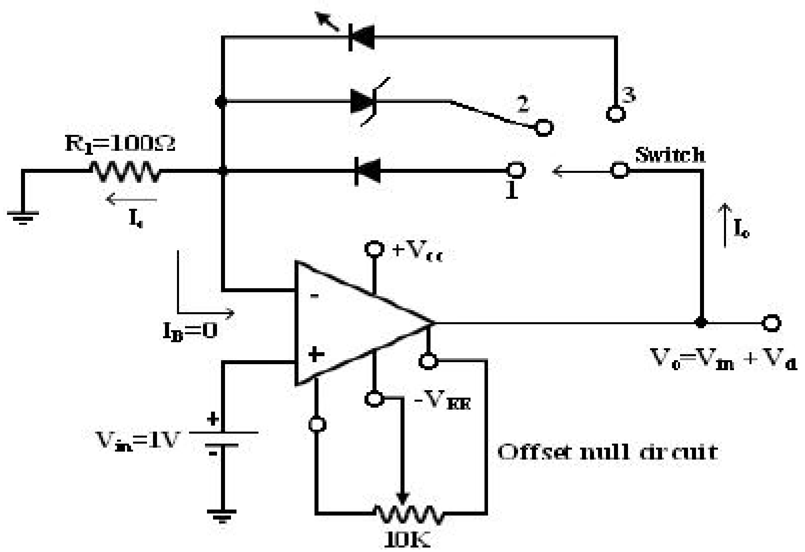


Fig. 2.10 Diode Match finder:

To avoid an error in output voltage the op-amp should be initially nulled. Thus the matched diodes can be found by connecting diodes one after another in the feedback path and measuring voltage across them.

2. Zener diode Tester:

(When the switch position 2) when the switch is in position 2, the circuit becomes a Zener diode tester. The circuit can be used to find the breakdown voltage of Zener diodes. The Zener current is set at a constant value by Vin and R1. If this current is larger than the knee current (I_{ZK}) of the Zener, the Zener blocks (V_Z) volts. For Ex: I_{ZK} = 1mA , V_Z = 6.2V, Vin = 1V, R_1 = 100Ω Since the current through the Zener is , I0 = Vin/R_1 = 1/100 =10mA > I_{ZK} the voltage across the Zener will be approximately equal to 6.2V.

3. When the switch is in position 3: (LED)

The circuit becomes a LED when the switch is in position 3. LED current is set at a constant value by Vin and R1. LEDs can be tested for brightness one after another at this current. Matched LEDs with equal brightness at a specific value of current are useful as indicates and display devices in digital applications.

Applications of I – V Converter:

One of the most common uses of the current to voltage converter is
1. Digital to analog Converter (DAC)
2. Sensing current through Photo detector. Such as photo cell, photo diodes and photovoltaic cells. Photoconductive devices produce a current that is proportional to an incident energy or light (i.e). It can be used to detect the light.

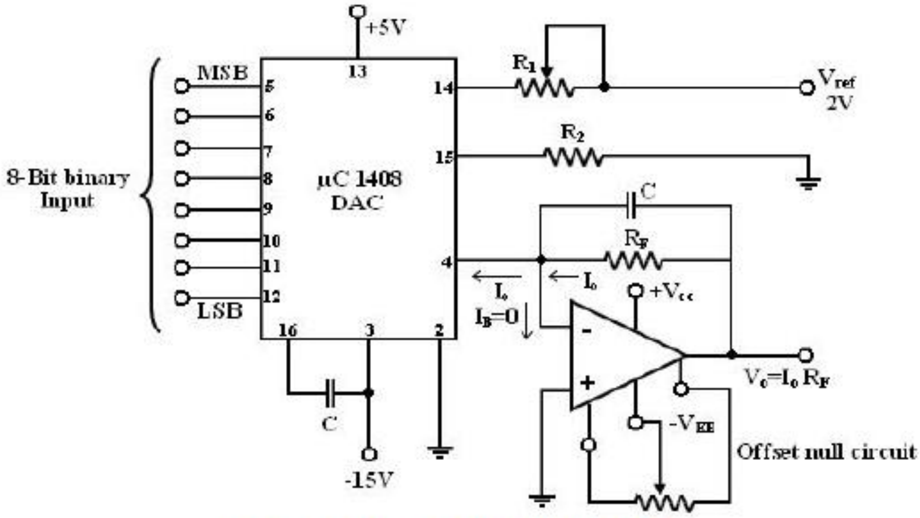


Fig. 2.11 I – V Converter DAC

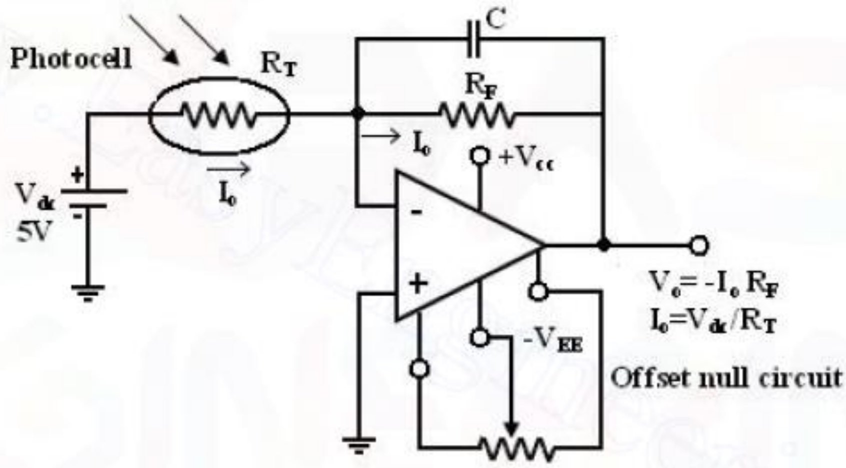


Fig. 2.12 Photo cell detector

Photocells, photodiodes, photovoltaic cells give an output current that depends on the intensity of light and independent of the load. The current through these devices can be converted to voltage by I – V converter and it can be used as a measure of the amount of light. In this fig photocell is connected to the I – V Converter. Photocell is a passive transducer it requires an external dc voltage (Vdc). The dc voltage can be eliminated if a photovoltaic cell is used instead of a photocell. The Photovoltaic Cell is a semiconductor device that converts the radiant energy to electrical power. It is a self-generating circuit because it does not require dc voltage externally.

Ex of Photovoltaic Cell: used in space applications and watches.

2.6 Adder:

Op-amp may be used to design a circuit whose output is the sum of several input signals. Such a circuit is called a summing amplifier or a summer or adder. An inverting summer or a non-inverting summer may be discussed now.

Inverting Summing Amplifier:

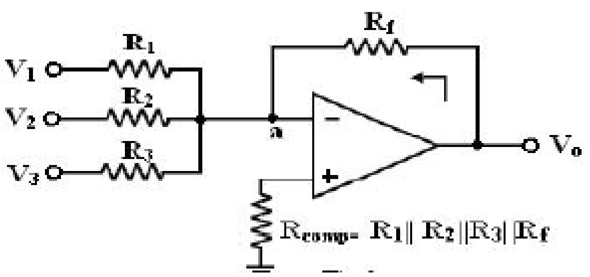


Fig. 2.13 inverting summer

A typical summing amplifier with three input voltages V1, V2 and V3 three input resistors R1, R2, R3 and a feedback resistor Rf is shown in figure 2.

The following analysis is carried out assuming that the op-amp is an ideal one, AOL= ∞. Since the input bias current is assumed to be zero, there is no voltage drop across the resistor Rcomp and hence the non-inverting input terminal is at ground potential.

$I= V_1/R_1+V_2/R_2\ldots..+V_n/R_n$;

$V_o= - R_f\, I=R_f/R(V_1+V_2+\ldots.V_n)$.

To find Rcomp, make all inputs V1 = V2 = V3 = 0.

So the effective input resistance Ri = R1 || R2 || R3.

Therefore, Rcomp = Ri || Rf = R1 || R2 || R3 || R,f.

Non-Inverting Summing Amplifier:

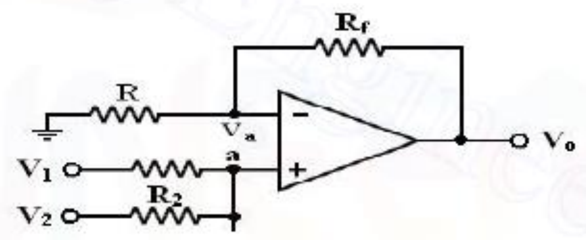


Fig.2.14 Non inverting summer

A summer that gives a non-inverted sum is the non-inverting summing amplifier of figure Let the voltage at the (-) input terminal be Va. which is a non-inverting weighted sum of inputs. Let R1 = R2 = R3 = R = Rf/2, then Vo = V1+V2+V3

2.7 Subtractor:

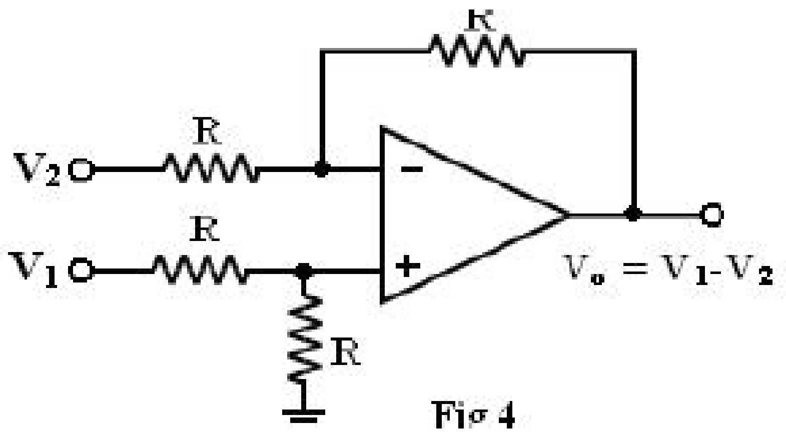


Fig. 2.15 Subtractor

A basic differential amplifier can be used as a subtractor as shown in the above figure. If all resistors are equal in value, then the output voltage can be derived by using superposition principle. To find the output V01 due to V1 alone, make V2 = 0.

Then the circuit of figure as shown in the above becomes a non-inverting amplifier having input voltage V1/2 at the non-inverting input terminal and the output becomes

$V_{01} = V_1/2(1+R/R)$ = V1 when all resistances are R in the circuit.

Similarly the output V02 due to V2 alone (with V1 grounded) can be written simply for an inverting amplifier as

$V_{02} = -V_2$

Thus the output voltage Vo due to both the inputs can be written as

$V_0 = V01 - V02 = V1 - V2$

Adder/Subtractor:

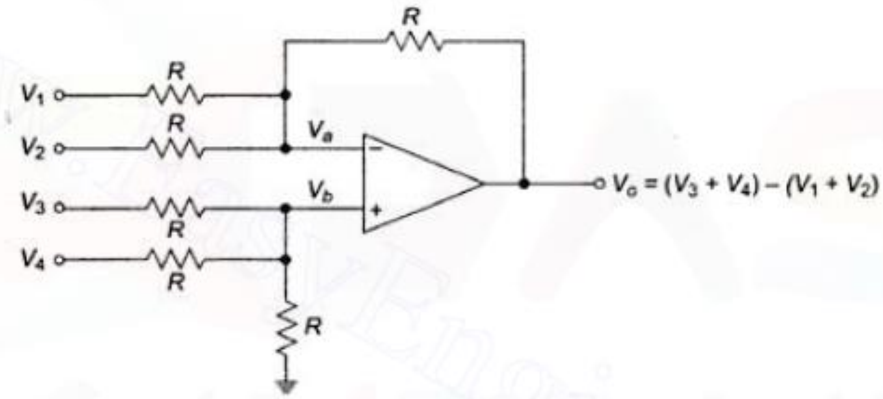


Fig. 2.16 Adder-Subtractor

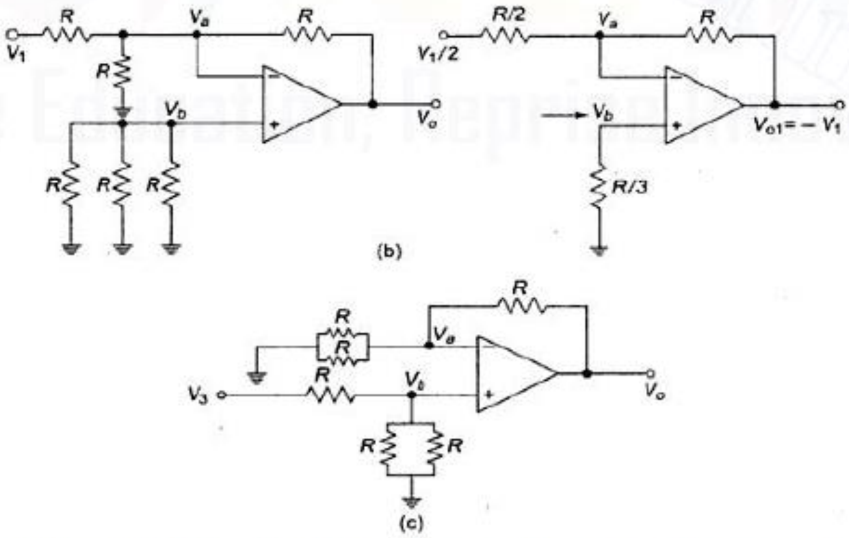


Fig. 2.17 (b) equivalent circuit for $V_2=V_3=V_4=0$ and (c) for $V_1=V_2=V_4=0$

It is possible to perform addition and subtraction simultaneously with a single op-amp using the circuit shown in figure 2.16.

The output voltage Vo can be obtained by using superposition theorem. To find output voltage V01 due to V1 alone, make all other input voltages V2, V3 and V4 equal to zero. The simplified circuit is shown in figure 2.17. This is the circuit of an inverting amplifier and its output voltage is, V_{01}= -R/(R/2) * V $_1$/2= - V_1 by Thevenin's equivalent circuit at inverting input terminal).

Similarly, the output voltage V02 due to V2 alone is,

$V_{02}= - V_2$

Now, the output voltage V03 due to the input voltage signal V3 alone applied at the (+) input terminal can be found by setting V1, V2 and V4 equal to zero.

$V_{03}=V_3$

The circuit now becomes a non-inverting amplifier as shown in fig.(c).

So, the output voltage V03 due to V3 alone is

V03 = V3

Similarly, it can be shown that the output voltage V04 due to V4 alone is

$V04 = V4$

Thus, the output voltage Vo due to all four input voltages is given by

$Vo = V01 = V02 = V03 = V04$

$Vo = -V1 - V2 + V3 + V4$

$V o = (V 3 + V 4) – (V1 + V 2)$

So, the circuit is an adder-subtractor.