UJT (UNIJUNCTION TRANSISTOR)

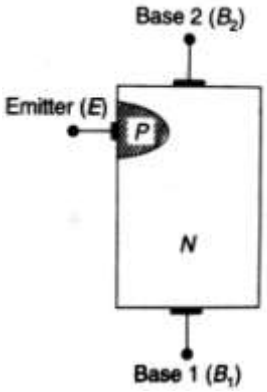
UJT is a **three terminal semiconductor switching device**. As it has only one PN junction and three leads it is commonly called as Unijunction Transistor.

NUTSHELL

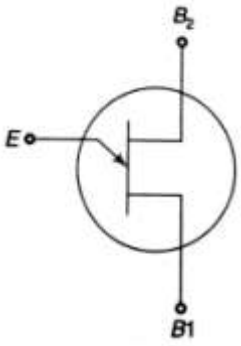
- Three Terminal
- One PN junction

Basic Structure

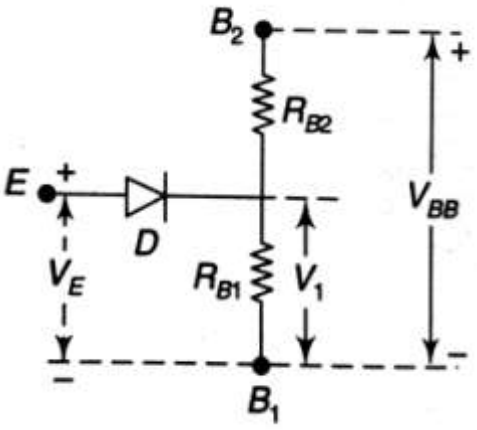
It consists of a lightly doped N – type silicon bar with a heavily doped P – type material alloyed to its one side closer to B_2 for producing single PN junction. The emitter leg is drawn at an angle vertical and the arrow indicates the direction of conventional current.



Basic Structure



Circuit Symbol



Equivalent Circuit

Characteristics of UJT:

NUTSHELL

- Voltage V_1 reverse biased
- Positive voltage V_E
- Negative voltage V_E

Interbase Resistance between B_2 and $B_1$of the silicon bar is$\mathbf{R_{BB} = R_{B1} + R_{B2}}$. With emitter terminal open, if voltage V_{BB} is applied between the two bases, a voltage gradient is established along the N – type bar.

The voltage drop across R_{B1} is $\boldsymbol{V_1 = \eta V_{BB}}$

Intrinsic Stand – off ratio, $\boldsymbol{\eta = \frac{R_{B1}}{R_{B1}+R_{B2}}}$ (typical value of η ranges from 0.56 to 0.75)

The voltage V_1 reverse biases the PN junction and emitter current is cut – off. But a small leakage current flows from B_2 to emitter due to minority carriers.

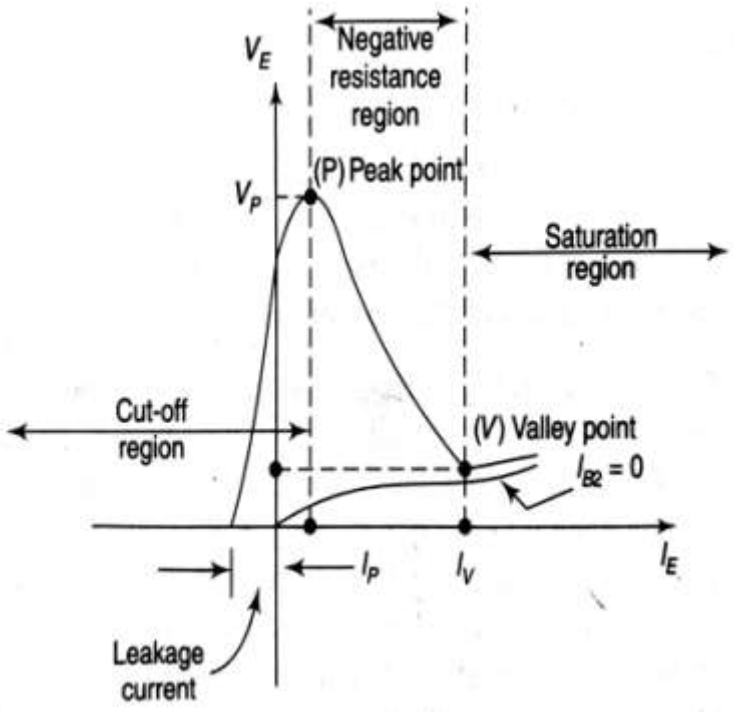
If a **positive voltage V_E is applied to emitter**, the PN junction will remain reverse biased so long as $\mathbf{V_E < V_1}$. If $\mathbf{V_E}$ **exceeds** $\mathbf{V_1}$ by the cut – in voltage V_γ, the diode becomes forward biased. Under this condition, holes are injected into the N – type Bar.

Holes are repelled by the terminal B_2, Holes are attracted by the terminal B_1. The device is in **ON state**

If a **negative voltage V_E is applied to emitter,** the PN junction remains reverse biased and the emitter current is cut – off. The device is now in OFF state.

Input Characteristics of UJT

The diode is reverse biased up to the peak point P. The region to the left of the peak point is called ***cut – off region.*** UJT has a stable firing voltage V_p which depends linearly on V_{BB}.



At P, the Peak Voltage$\mathbf{V_P = \eta V_{BB} + V_\gamma}$, the diode starts conducting and the holes are injected into the N layer. Hence, the resistance decreases thereby decreasing V_E for the increase in I_E.

Negative resistance region: From Peak point P to valley point V. After the valley point, the device is driven into saturation and behaves like a conventional forward biased PN junction diode. The region to the right of the valley point is called saturation region.

Valley Point: Resistance changes from negative to positive.

UJT RELAXATION OSCILLATOR

The relaxation oscillator using UJT which is meant **generating saw tooth waveform.**

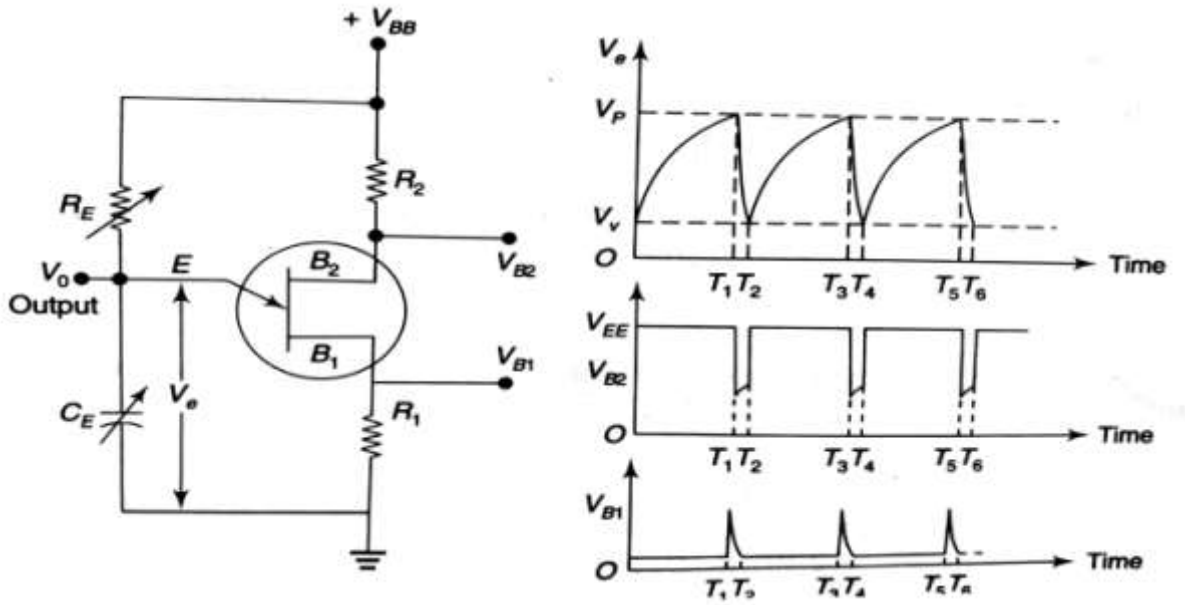


Fig: UJT Relaxation Oscillator

The voltage across the capacitor increases exponentially and the when the **capacitor voltage reaches the peak point voltage V_P**, the **UJT starts conducting** and the capacitor voltage is **discharged rapidly through EB_1 and R_1**. After the peak point voltage of UJT is reached, it provides negative resistance to the discharge path which is useful in the working of the relaxation oscillator. As the capacitor voltage reaches zero, the device then cuts off and capacitor C_E starts to charge again. This cycle is repeated continuously generating a ***saw tooth waveform*** across C_E

By changing the values of capacitances C_E or resistance R_E, the frequency of the output waveform can be changed as desired, since these values control the time constant R_EC_E of the capacitor charging circuit.

Frequency of Oscillation:

Assuming the capacitor is initially uncharged, the voltage V_C across the capacitor prior to breakdown is

$$\mathbf{V_C = V_{BB}\left(1 - e^{-t/R_EC_E}\right)}$$

$R_EC_E = charging\ time\ constant\ of\ resistor -$ Capacitor circuit

The discharge of the capacitor occurs when $V_C = V_p$ (peak – point voltage)

$$V_P = \eta V_{BB} = V_{BB}\left(1 - e^{-t/R_E C_E}\right)$$

$$\eta = 1 - e^{-t/R_E C_E}$$

$$e^{-t/R_E C_E} = (1 - \eta)$$

$$t = R_E C_E log_e \frac{1}{1-\eta}$$

$$\boldsymbol{t = 2.303 R_E C_E log_{10} \frac{1}{1-\eta}}$$

Therefore, frequency of Oscillation of sawtooth wave,

$$\mathbf{f_o = \frac{1}{t} = \frac{1}{2.303 R_E C_E log_{10} \frac{1}{1-\eta}}}$$

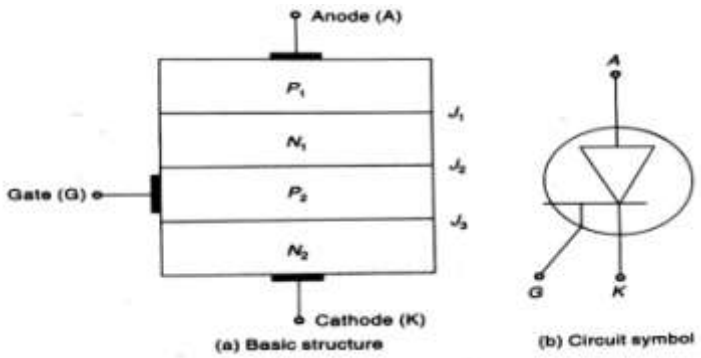
SCR (SILICION CONTROLLED RECTIFIER)

Basic Structure and circuit symbol

NUTSHELL

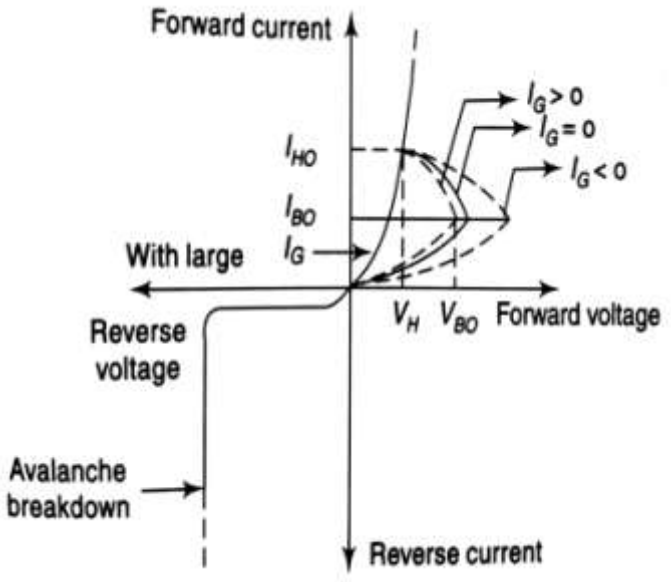
- Four Layer
- Three Terminal
- Gate, Cathode, Anode

It is a four layer, there terminal device in which the end P – layer act as a anode, the end N – layer acts as a cathode and P – layer nearer to cathode acts as gate. As leakage current in silicon so very small compared to germanium, SCR are made of silicon and not germanium.



Characteristics of SCR:

The characteristics of SCR are shown. SCR acts as a switch when it is forward biased. When the gate is kept open, i.e.,



$I_G = 0$: Operation of SCR is similar to PNPN diode.

$I_G < 0$: The amount of reverse bias applied to J_2 is increased. So the break over voltage V_{BO} is increased.

$I_G > 0$: The amount of reverse bias applied to J_2 is decreased, thereby decreasing the break over voltage. With very large positive gate current, break over may occur at a very low voltage such that the characteristics of CSRC is like that of ordinary PN diode.

As the voltage at which the SCR is switched 'ON' can be controlled by varying the gate current I_G is commonly called as **controlled switch**. Once the SCR is turned ON, the gate loses control: i.e., the gate cannot be used to switch the device OFF. One way to turn the device OFF is by lowering the anode current below the holding current I_H by reducing the supply voltage below the holding voltage V_H, keeping the gate open.

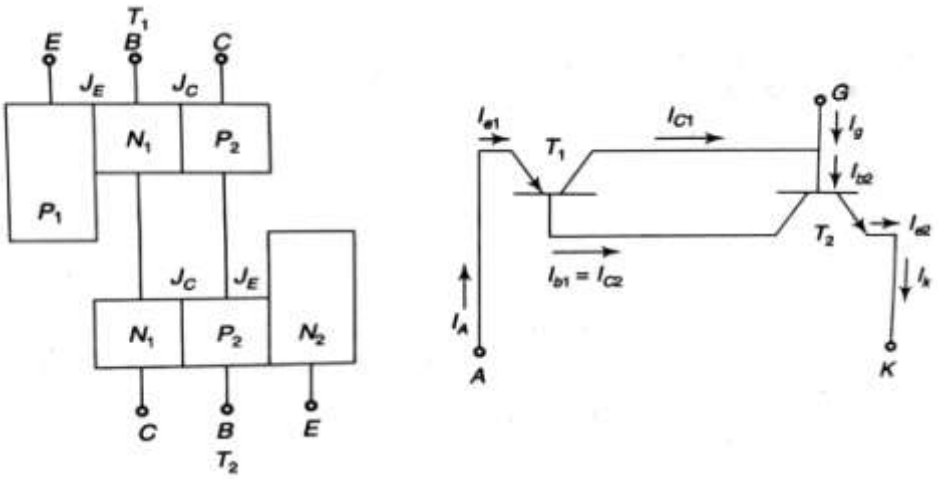
Applications of SCR:

Relay control	Motor control
Phase control	Heater control
Battery chargers	Inverters
Regulated power supplies	Static switches

Two transistor version of SCR:

The operation of SCR can be obtained in a very simple way by considering it in terms of two transistors, called as the two-transistor version of SCR. An SCR can be split into two parts and displaced mechanically from one another but connected electrically. Thus, the

device may be considered to be constituted by two transistors T_1 (PNP) and T_2 (NPN) connected to back to back.



Assuming the leakage current of T_1 to be negligibly small, we obtain

$$I_{b1} = I_A - I_{c1} = I_A - \alpha_1 I_A = (1 - \alpha_1) I_A$$

Also, it is clear that

$$I_{b1} = I_{c2}$$

$$I_{c2} = \alpha_2 I_k$$

Substituting the values

$$(1 - \alpha_1) I_A = \alpha_2 I_k$$

$$I_K = I_A + I_g$$

Substituting

$$(1 - \alpha_1) I_A = \alpha_2 (I_A + I_g)$$

$$(1 - \alpha_1 - \alpha_2) I_A = \alpha_2 I_g$$

$$\mathbf{I_A = \left[\frac{\alpha_2 I_g}{1 - (\alpha_1 - \alpha_2)}\right]}$$

Equation indicates that if $(\alpha_1 + \alpha_2) = 1, then\ I_A = \infty$, i.e., the anode current I_A suddenly reaches a very high value approaching infinity. Therefore, the device suddenly triggers into ON state from the original OFF state. This characteristic of the device is known as its regenerative action.

LASCR (LIGHT ACTIVATED SCR)

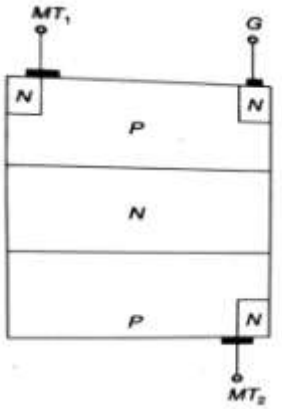
It is triggered by irradiating with light. The arrows represent the incoming light that passes through a window and falls on the depletion layer closer to the middle junction J_2 of SCR. The incident light generates electron – hole pairs in the device thus increasing the number of charge carriers. This leads to the instantaneous flow of current within the device and the device turns ON. For light triggering to occur, the device must have high value of rate of change of voltage with time, dV/dt.

TRIAC (TRIODE AC SWITCH)

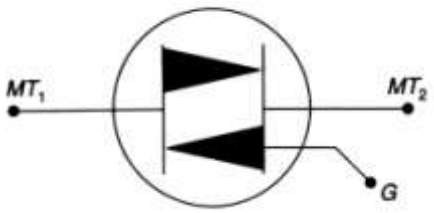
NUTSHELL

- Three terminals
- MT1, MT2 & Gate

TRIAC is a three terminal semiconductor switching device which can control the alternating current in a load. Its three terminals are **MT_1, MT_2**, and the **gate (G)**. The basic structure and circuit symbol of TRIAC are shown. TRIAC is equivalent to two SCR's connected in parallel but in the reverse direction as shown. So a TRIAC will act as a switch for both directions.



Basic Structure



Circuit Symbol

Characteristics of TRIAC:

- Like an SCR, a TRIAC also starts conducting only when the break over voltage is reached. Earlier to that the leakage current which is very small in magnitude flows through the device and therefore remains in the **OFF state**.

- The device, when starts conducting, allows a very large amount of current to flow through it. The high inrush of current must be limited using the external resistance, or it may otherwise damage the device.

  Positive half cycle - MT_1 is positive with respect to MT_2,

  N**egative half cycle** - MT_2 is positive with respect to MT_1

- A TRIAC is **a bidirectional device and can be triggered either by a positive or by a negative gate signal**. By applying proper signal at the gate, break over voltage i.e., firing angle of the device can be changed; thus phase control process can be achieved.

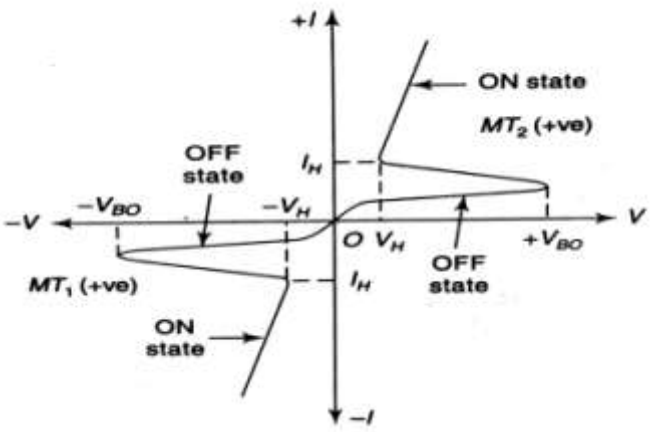


Fig: Characteristics of TRIAC

Applications of TRIAC

Illumination control, temperature control, liquid level control, motor speed control and as static switch to turn AC power ON and OFF.

Limitations

Low power handling capacity.

DIAC (DIODE AC SWITCH)

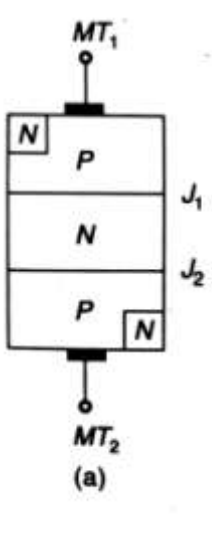
NUTSHELL

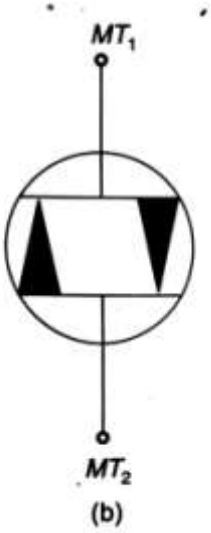
- Three Layer
- Two terminals (MT1 & MT2)

- DIAC is a three-layer, **two terminal semiconductor devices**. MT_1 and MT_2 are the two main terminals which are interchangeable.

- It acts as a **bidirectional Avalanche diode**. It does not have any control terminal. It has two junctions J_1 and J_2. Though the DIAC resembles a bipolar transistor, the central layer is free from any connection with the terminals.

Basic Structure





Circuit Symbol

Characteristics of DIAC:

It acts as a switch in both directions. As the doping level at the two ends of the device is same, the DIAC has identical characteristics for both positive and negative half of an AC cycle.

Positive half cycle - MT_1 is positive with respect to MT_2

Negative half cycle - MT_2 is positive with respect to MT_1.

At voltage less than the breakover voltage, a very small amount of current called the leakage current flows through the device and the device remains in OFF state. When the voltage level reaches the breakover voltage, the device starts conducting and it exhibits negative resistance characteristics, i.e., the current flowing in the device starts increasing and the voltage across it starts decreasing.

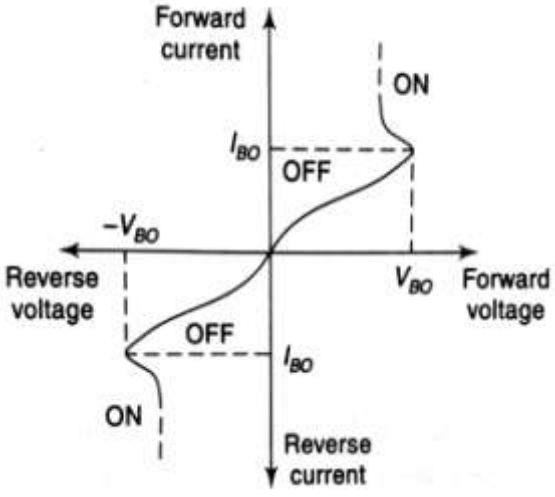


Fig: Characteristics of DIAC

The **DIAC is not a control device**. It is **used as triggering device** in TRIAC phase control circuits.

Applications of DIAC

Light dimming, Motor speed control and Heater control.

POWER AMPLIFIERS

Power dissipation in the output stage of a transistor is a major concern. While analysing and designing the circuit that specified power to a load, the output signal has to be linear.

Consider a multistage amplifier that has to deliver a large amount of power to a passive load. This power may be in the form of a large current delivered to a relatively small load resistance or may be in the form of a large voltage delivered to a relatively large load resistance. The output stage of a power amplifier must be designed to meet the power requirements. **Power amplifiers use transistors like power BJT's and power MOSFET's.**

One of the major concerns in the design of output stage is to deliver the required signal power to the load efficiently. Moreover, the power dissipated in the transistors of the output stage should be as small as possible. The output transistors must be capable of delivering the required current to the load and sustaining the required output voltage.

Power Transistors

Physical transistors have certain limitations in terms of maximum current, voltage and power. These limitations are not considered for normal transistors, because it was assumed that the transistors which can handle the current, voltage and power dissipation within a transistor does not cause any damage to the circuit.

But in the design of power amplifiers, it is necessary to consider the limitations of a transistor.

Limitations are

- Maximum rated current (amp),
- Maximum rates voltage (volts)
- Maximum rated power (watts).

POWER BJT

Construction:

The Structure of a vertically oriented NPN power transistor with the doping levels of a thickness of the layers is shown in the fig. This type of configuration has a large cross-sectional area to handle large currents and minimize the thermal resistance of the transistor. Here, the collector terminal is at the bottom.

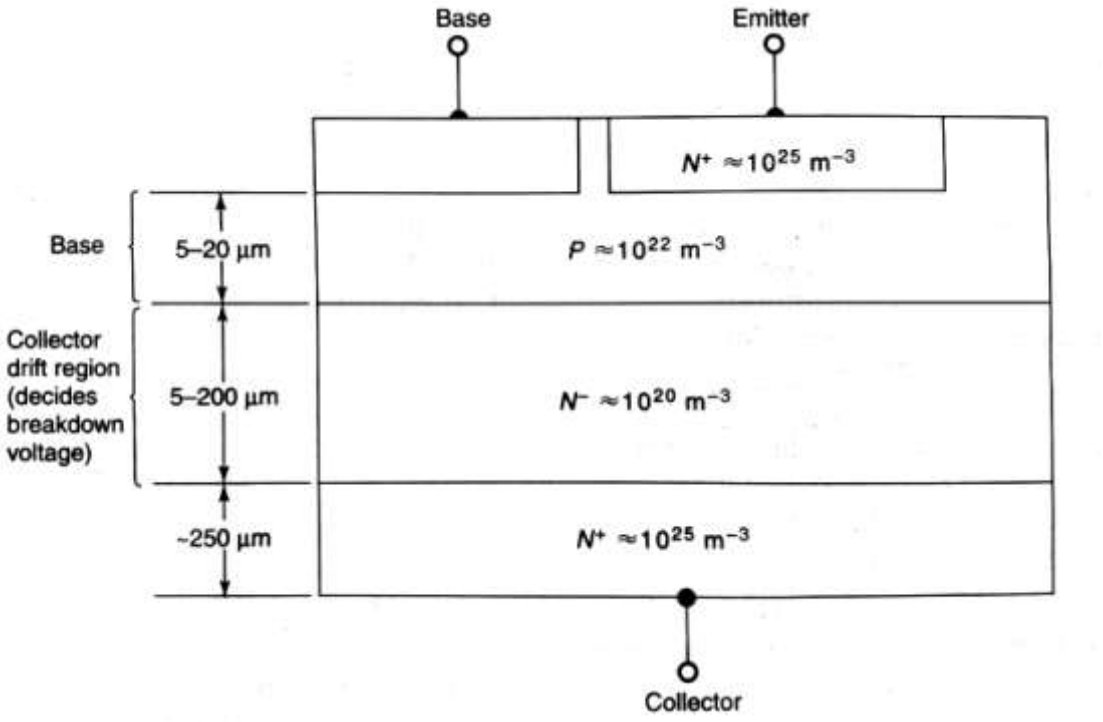


Fig: Cross section of a vertical NPN power BJT

The primary collector N^- region, called **drift region**, has a **low – doped impurity concentration 10^{20} m^{-3}** in such a way that the voltage can be applied across base – collector terminals without initiating breakdown. This region has a **thickness of about 50 – 200 μm.** The **thickness of the drift region determines the breakdown voltage of the transistor.**

Another **N^+ region** has a **higher doping concentration** which reduces the collector resistance and makes contact with the external terminal. This region has **a thickness of around 250 μm**. The doping in the emitter layer is large, whereas the base doping is comparatively less.

A sufficient base width is required to prevent punch – through breakdown. Since the small base thickness of about 5 – 20 μm reduces the breakdown voltage, the amplification

capabilities and the breakdown voltages are to be compromised in power transistors. A large base – collector voltage implies a relatively large space – charge width induced in the collector and base regions.

VI Characteristics

Power transistors are generally large area devices. The properties of power transistors vary from small signal devices in terms of differences in geometry and doping concentrations. The current gain of power transistors is in the range of 5 to 20 which is smaller to that of small – signal BJT's. But the current gain is a strong function of collector current and temperature. The current gain versus collector current characteristics of power BJT at various temperatures is shown. The current gain drops off for high current levels. The parasitic resistance in the base and collector regions region may become significant by affecting the transistor terminal characteristics.

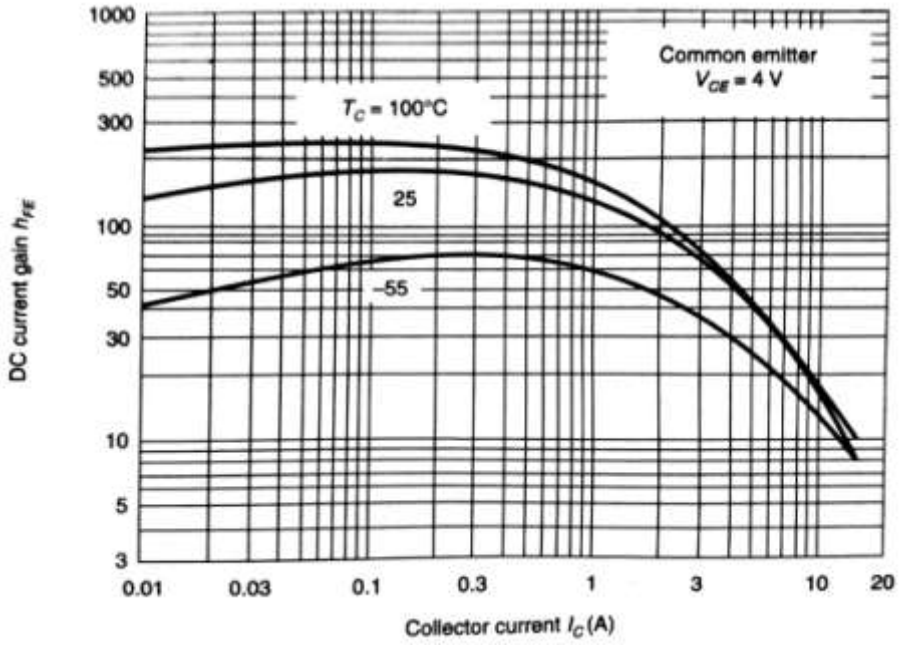


Fig: DC Characteristics of β vs I_C

The maximum rated collector current $I_{c,\ rated}$ is related to the maximum current that the wires connecting the semiconductor to the external terminals can handle or the collector current at which the current gain falls below a minimum specified value or the current that lead to the maximum power dissipation when the transistor is in saturation.

In BJT's the maximum voltage limitations is associated with avalanche breakdown in the reverse – biased base – collector junction. In common – emitter configuration, the breakdown voltage mechanism involves the transistor gain and the breakdown phenomenon on the PN junction. Typical I_C versus V_{CE} characteristic curve of BJT is shown. When the base terminal is open circuited, i.e., $I_B = 0$, the breakdown voltage is V_{CEO}.

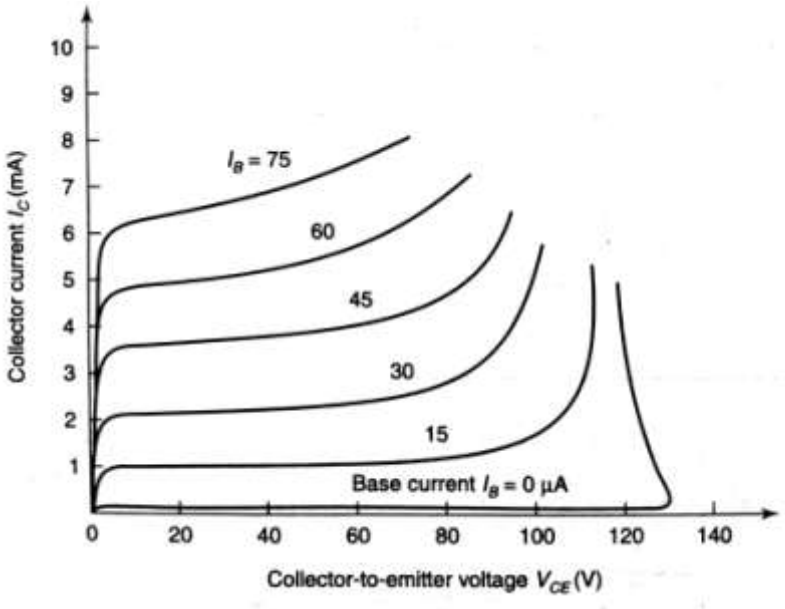


Fig: I_C versus I_E characteristics

When the transistor is biased in the active region, the collector current begins to increase significantly before breakdown voltage V_{CEO} is reached. Once the breakdown has occurred, all the curves tend to merge to the same collector – emitter voltage. The curves merging voltage is denoted as $V_{CE(sus)}$ and it is minimum voltage is necessary to sustain the transistor in breakdown.

When operating BJT at high voltage and at high current, another breakdown effect will occur and it is called second breakdown. Slight non – uniformities in the current density produce an increasing heating of local region. The resistance level of semiconductor material is decreased because of increased heating in the local region.

The effect results in positive feedback, and the current continues to increase, which further increases the temperature, until the semiconductor material may actually be melt.

The instantaneous power dissipation in a BJT is given by,

$$P_Q = V_{CE} I_C + V_{BE} I_B$$

where the base current I_B is generally much smaller than the collector current I_C. Therefore, the instantaneous power dissipation is approximated to

$$P_Q \cong V_{CE} I_C$$

By integrating the above equation over one cycle, the average power is given by,

$$P_Q = \frac{1}{T} \int_0^T V_{CE} I_C dt$$

The average power dissipated in BJT must be kept below a specified maximum value, to ensure that the temperature of the device remains below the maximum value. If the collector current and collector – emitter voltage are DC quantities, then maximum rated power P_T for BJT can be written as

$$P_T = V_{CE} I_C$$

The average power limitation P_T is a hyperbola as per the above equation.

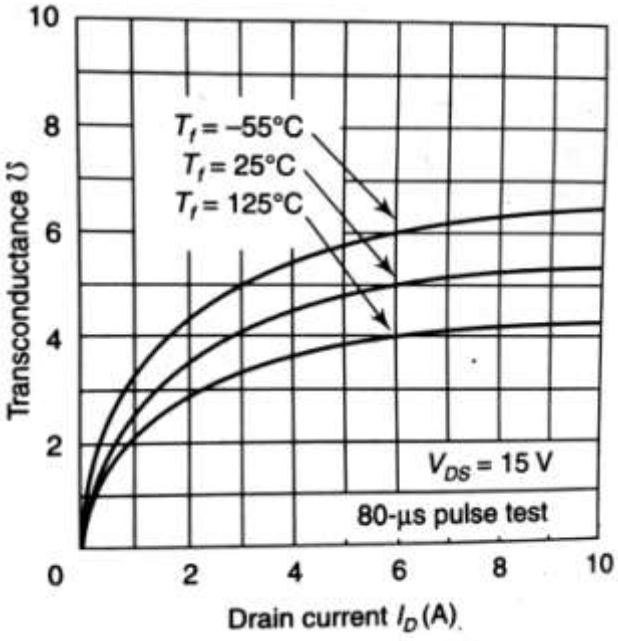
Power transistors which are designed to handle large current require large emitter areas to maintain reasonable current densities. These transistors are usually designed with narrow emitter widths to minimize the parasitic base resistance and fabricated as an interdigitated structure as shown. In each emitter leg, small resistors are incorporated which helps to maintain equal current in each B – E junction.

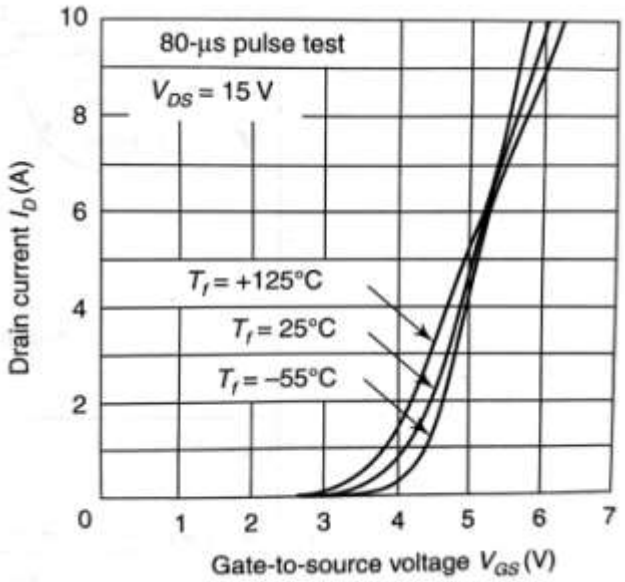
POWER MOSFET

Two N – channel power MOSFETs with parameters are listed. The drain currents are in ampere range and breakdown voltage is in the hundreds of volt range. Power MOSFET is different from bipolar power transistor in terms of operating principles and performance. The performance characteristics of power MOSFETs include faster switching, no second breakdown, stable gain and response time over a wide temperature range. Transconductance versus drain current curves for different temperatures are shown.

The variation with temperature of the MOSFET transconductance is less.

Transconductance vs drain current **I_D versus V_{GS} characteristics for**





The MOSFET has high input impedance and it is a voltage – controlled device like JFET. Unlike the driver circuit of BJT, a MOSFET driver circuit is simple. The MOSFET is a majority carrier device and any increase in temperature of the device affects the mobility of the majority carriers, which results in increase of resistivity of the semiconductor. From it is clear that MOSFETs are more immune to the thermal runaway effects and the second breakdown phenomena experienced in BJT's. The Figure shows the typical I_D versus V_{GS} characteristics at several temperatures. From the characteristics curve, for the given gate – to – source voltage at high current level, the current actually decreases with increase in temperature.

The disadvantage of MOSFET is compensated by changing the construction mode from planar structure to a vertical one.

DMOS

DMOS is a FET structure created specifically for high power applications and it is planar transistor whose name is derived from the double – diffusion process used to construct it. DMOS is also used in switching applications with high – voltage and high – frequency behaviour, like inkjet print head power supplies and automobile control electronics.

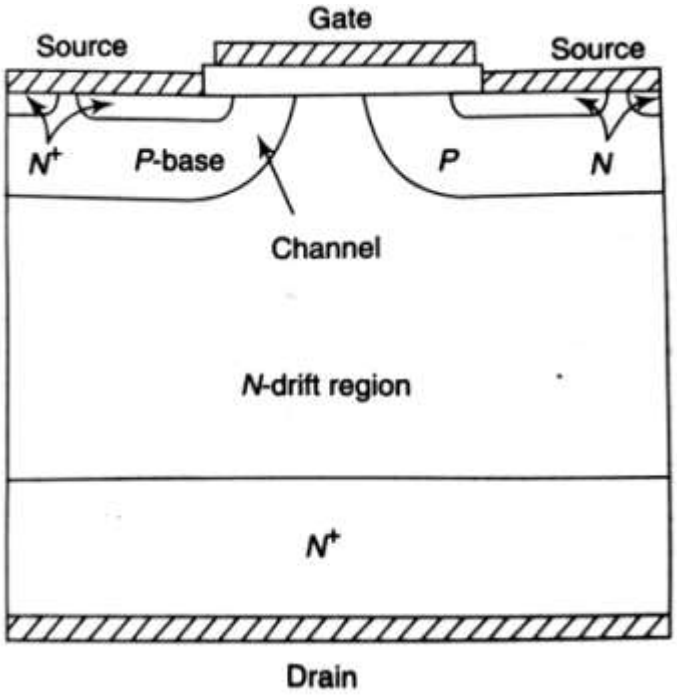


Fig: Cross section of the DMOS structure

The cross – sectional view of a DMOS structure is shown. The P – substrate region and the N^+ source contact are diffused through a common window defined by the edge of the gate. The P – substrate region is diffused deeper than the N^+ source. The surface channel length is defined as the lateral diffusion distance between the P – substrate and the N^+ source.

Electrons outside the source terminal flow laterally through the inversion layer under the gate to the N – drift region. Then, electrons flow vertically through the N – drift region to the drain terminal. The conventional current direction is from the drain to the source. The most important characteristics of DMOS device is their breakdown voltage and on – resistance. DMOS is similar to BJT, due to high – voltage and high – frequency characteristics. A lightly doped drift region between the drain contact and the channel region helps to ensure a very high breakdown voltage. Moreover, the N – drift region must be moderately doped so that the drain breakdown voltage is sufficiently large. The thickness of the N – drift region should be as small as possible to minimize the drain resistance.

VMOS

Elements of the planar MOSFET are present in the vertical metal – oxide – silicon FET (VMOS) as shown. The terminals of the device are connected to the metallic surface. The SiO_2 layer is placed between the gate and the P – type region and between the drain and source for the growth of induced N – channel (enhancement mode operation). The term vertical in VMOS is because of the fact that the channel is formed in the vertical direction rather than horizontal direction in the planar device. Moreover, the channel has the appearance of a "V" cut in the semiconductor base, which is also an important characteristic of the device. The construction of VMOS is simple by leaving out some of the transition levels of doping.

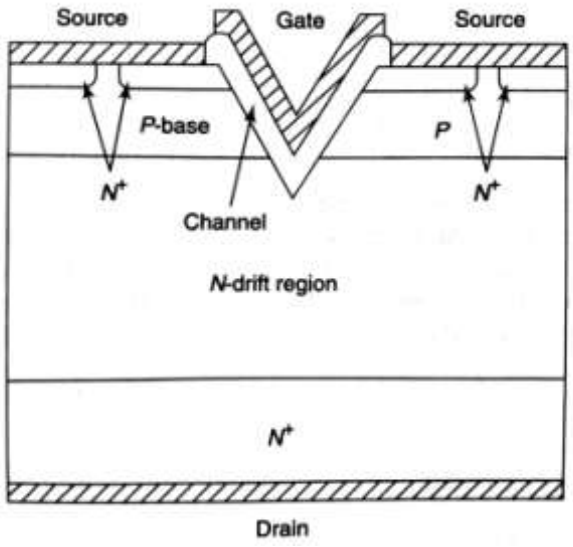


Fig: VMOS Structure

The N – channel is induced or enhanced in the narrow P –type region of the device if a positive voltage is applied to the drain, negative voltage to the source and 0V or same positive voltage level the gate. The vertical height of the P – region defines the length of the channel and this length on a horizontal plane is limited to 1μm to 2μm. Diffusion layers such as P – region of the device can be controlled to small fraction of μm.

Resistance levels and the power dissipation levels of the device at operating current will be reduced because of the reduced channel length. Also, the contact area between the channel and the n^+ region is much increased by the vertical mode construction, which contributes to a further reduction in the resistance level and increased area between doping layers for current flow. Two conduction paths exist between the drain and source. This

conduction path further contributes to a higher current rating. The final result is that VMOS is a device with drain currents that can reach the ampere levels with power levels exceeding low. The VMOS FETs have reduced channel resistance levels, higher current rating and higher power rating when compared to planar MOSFET. Due to its high – current handling capacity, VMOS transistors are useful in power amplifier applications.

Another important characteristic of vertical construction in VMOSFET is to have positive temperature coefficient which overcomes the possibility of thermal runaway. The resistance level of a device increases with increase in temperature of the device because of surrounding medium and current. This causes reduction in drain current of the device, whereas for conventional devices, the drain current will increase. Negative temperature coefficient results in decreased levels of resistance with increase in temperature, which increases the current level, which in turn results in temperature stability and thermal runaway.

The reduced charge storage level in VMOS results in faster switching time when compared to conventional planar construction. The switching time of VMOS device is less than one - half that encountered in conventional BJT transistors.

LIGHT EMITTING DIODE (LED)

The Light Emitting Diode (LED) is a PN junction device which emits light when forward biased, by a phenomenon called **electroluminescence**. In all semiconductor PN junctions, some of the energy will be radiated as heat and some in the form of photons. In silicon and germanium, greater percentage of energy is given out in the form of heat and the emitted light is insignificant. In other materials such as **gallium phosphide (GaP) or gallium arsenide phosphide (GaAsP)**, the number of photons of light energy emitted is enough to create a visible light source. Here, the charge carrier recombination takes place when electrons from the N – side cross the junction and recombine with the holes on the P – side.

Forward Bias:

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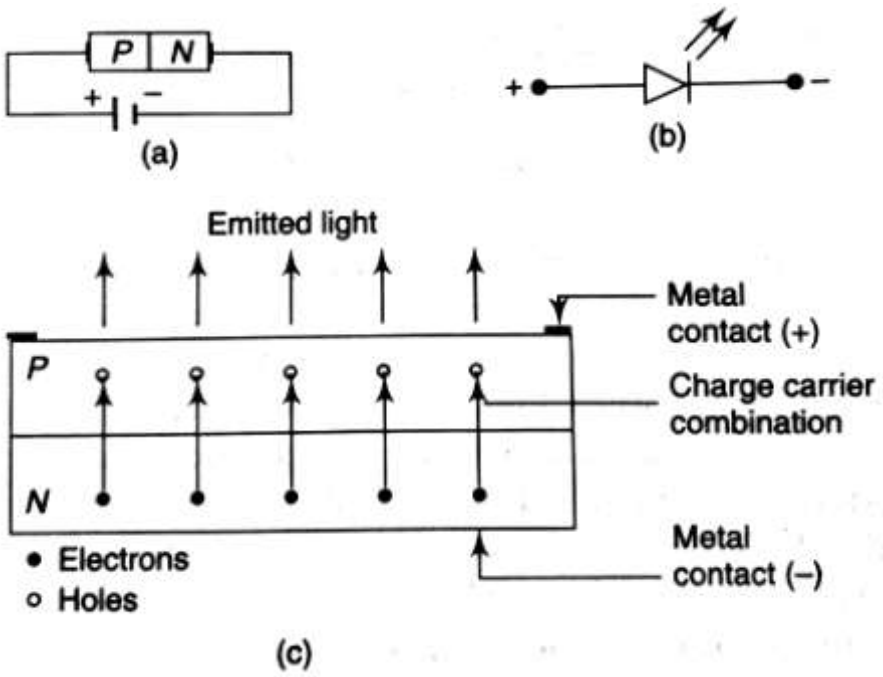
- Under Forward Bias
- Difference of energy

When an LED under is **under forward biased**, the electrons and holes move towards the junction and recombination takes place. As a result of recombination, the electrons lying in the conduction bands of N – region fall into the holes lying in the valence band of a P – region. The difference of energy between the conduction band and the valence band is radiated in the form of light energy. Each

recombination causes radiation of light energy. Light is generated by recombination of electrons and holes whereby their excess energy is transferred to an emitted photon.

Brightness of the emitted light is directly proportional to the forward bias current.



(a) LED under Forward Bias (b) Symbol (c) Recombination's and emission of Light

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- Carrier Recombination
- Domed Lenses
- Efficiency Generation

The above figure shows the basic structure of an LED showing recombination of carriers and emission of light. Here, an N – type layer is grown on a substrate and a P – type is deposited on it by diffusion. Since **carrier recombination takes place in the P – layer**, it is kept uppermost. The metal anode connections are made at the outer edges of the P – layer so as to allow more central surface area for the light to escape. **LEDs are manufactured with domed lenses** in order to reduce the reabsorption problem. A metal (gold) film is applied to the bottom of the substrate for reflecting as much light as possible to the surface of the device and also to provide cathode connection. LEDs are always encased to protect their delicate wires.

The **efficiency generation of light increases** with the increased in injected current and with a **decrease in temperature**. The light is concentrated near the junction as the carriers are available within a diffusion length of the junction.

LIQUID CRYSTAL DISPLAY (LCD)

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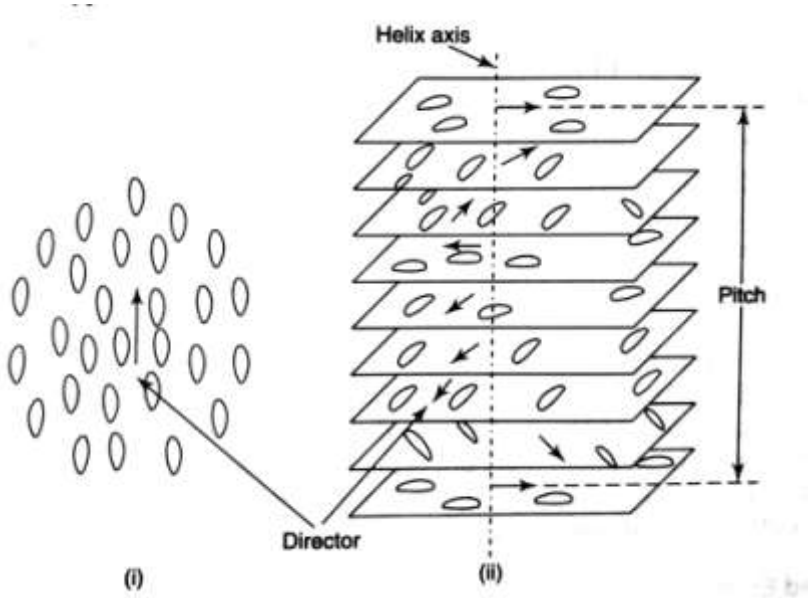
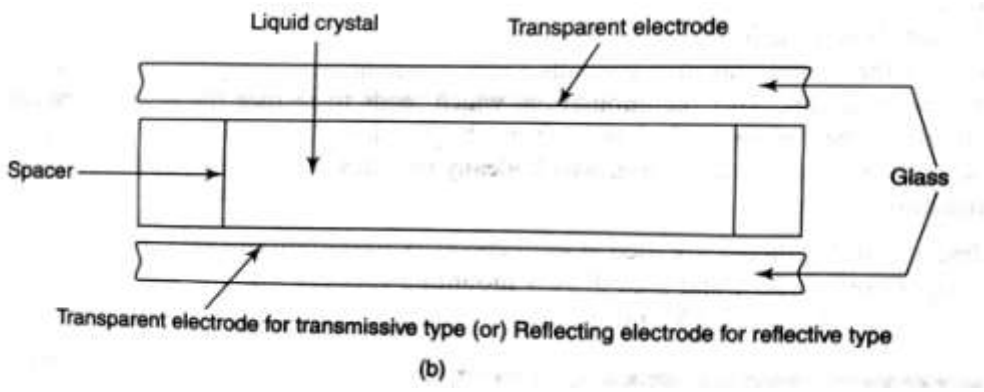
- Two liquid crystal materials
  - Nematic
  - Cholestric

Liquid Crystal Display (LCD's) is used for display of numeric and alphanumeric character in dot matrix and segmental displays. The **two liquid crystal materials** which are commonly used in display technology are **nematic** and **cholestric** whose schematic arrangement of molecules is as shown. The most popular liquid crystal structure is the **Nematic Liquid Crystal (NLC).** In this type, all the molecules align themselves approximately parallel to the unique axis (director), while retaining the complete translational freedom. The liquid is normally transparent, but of subjected to a strong electric field, disruption of the well-ordered crystal structure takes place causing the liquid to polarize and turn opaque. The removal of the applied electric field allows the crystal structure to regain its original form and the material becomes transparent.





(a) Schematic arrangement of molecules in liquid crystal (ii) Nematic and (ii) Cholesteric
(b) Construction of a dynamic scattering LCD

Based on the construction, LCDs are classified into two types. They are

(i) Dynamic scattering type
(ii) Field effect type

Dynamic Scattering Type:

The construction of dynamic scattering liquid crystal cell is shown. The display consists of two glass plates, each coated with tin oxide (SnO_2) on the inside with transparent electrodes separated by a liquid crystal layer, 5 to 50 μm thick.

Field Effect Type:

The construction of a field effect LCD display is similar to that of the dynamic scattering type, with the exception that two thin polarising optical filters are placed at the inside of each glass sheet. The LCD material is of twisted nematic type which twists the light passing through the cell when the later is not energised. This allows light to pass through the optical filters and the cell appears bright. When the cell is energised, no twisting of light takes place and the cell appears dull.

Liquid Crystal cells are of two types:

(i) Transmittive type – Both glass sheets are transparent so that light from a rear source is scattered in the forward direction when the cell is activated.
(ii) Reflective Type - Has a reflecting surface on one side of the glass sheet. The incident light on the front surface of the cell is dynamically scattered by an activated cell.

Advantages of LCD

- The voltage required are small
- They have low power consumption. A seven-segment display requires about 140 W, whereas LEDs require about 40 mW per numeral.
- They are economical

Disadvantages of LCD

- LCDs are very slow devices. The turn ON and OFF times are quite very large. The turn ON time is typically of the order of few ms, while the turn OFF time is 10ms.
- When used on DC, their life span is quite small. Therefore, they are used with AC supplies having a frequency less than 50 Hz.
- They occupy large area.

PHOTO TRANSISTOR

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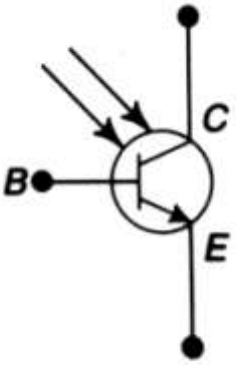
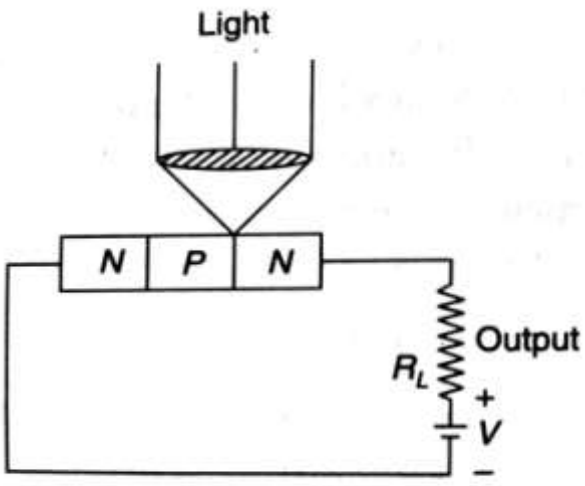
- Photo Diode + Transistor Amplifier
- CE configuration

Phototransistor or Photodiode is a much **more sensitive device semiconductor** photo device than the PN photodiode. The current produced by a photodiode is very low which cannot be directly used in control applications. Therefore, **this current should be amplified before applying to control circuits**. The phototransistor is a light detector which combines a photodiode and a transistor amplifier. When the phototransistor is illuminated, it permits a larger flow of current.



(a)



(b)

It is usually connected in **CE configuration** with the base open. A lens focuses the light on the base – collector junction. Although the photo transistor has three sections, only two leads, the emitter and collector leads, are generally used. In this device, base current is supplied by the current created by the light falling on the base – collector photodiode junction.

When there is no radiation excitation, the minority carriers are generated thermally, and the electrons crossing from the base to the collector and the holes crossing from the collector to the base constitute the reverse saturation collector I_{CO}. With $I_B = 0$, the collector current is given by

$$I_C = (\beta + 1)I_{CO}$$

When the light is turned ON, additional minority carriers are photo generated and the total collector current is

$$I_C = (\beta + 1)(I_{CO} + I_L)$$

The current in the transistor is dependent on the intensity of light entering the lens and is less affected by the voltage applied to the external circuit. Graph shows collector current I_C as a function of collector – emitter voltage V_{CE} and as a function of illumination H.

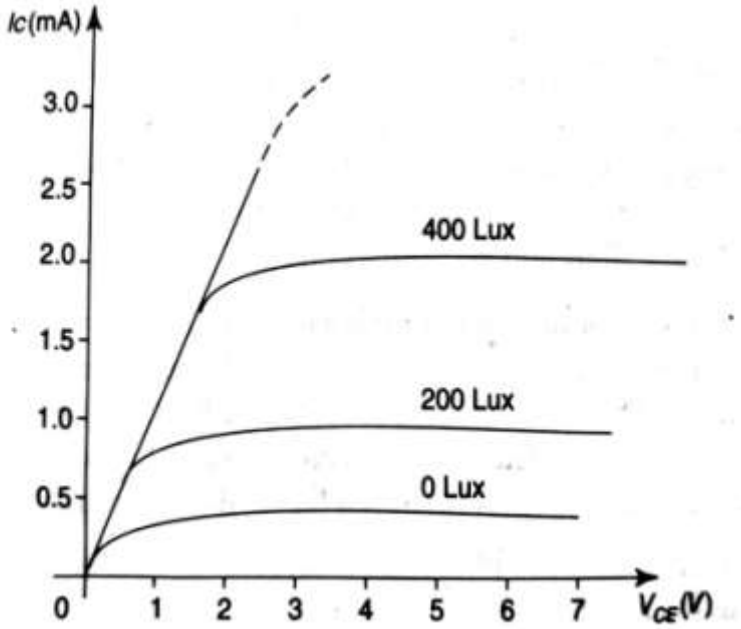


Fig: Characteristics of Phototransistor

OPTOCOUPLER

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- Light Emitter, Light Path & Light Detector
- Optoelectronic Coupler

An Optocoupler is a solid – state component in which the **light emitter, the light path and the light detector** are all enclosed within the component and cannot be charged externally. Optocoupler provides electrical isolations between circuits, it is also called optocoupler. An optoisolator allows signal transfer without coupling wires, capacitors or transformers. It can couple analog or digital (ON/OFF) signals.

Optoisolator, also referred to as an **optoelectronic coupler**, generally consists of an infrared LED and a photodetector such as PIN photodiode for fast switching, phototransistor Darlington pair, or photo – SCR combined in a single package. **Optoisolator transduce input voltage to proportional light intensity by using LEDs**. The light is transduced back to output voltage using light sensitive devices. GaAs LEDs are used to provide spectral matching with the silicon sensors.

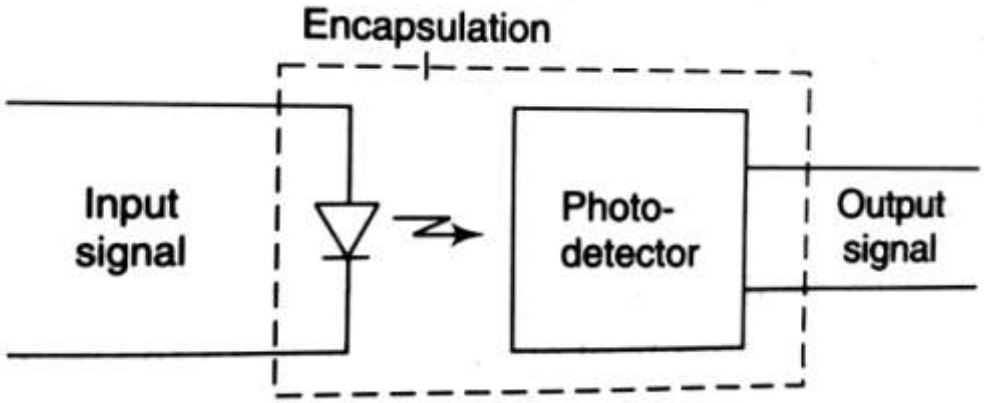

Fig: Schematic representation of an optocoupler

The wavelength response of each device is made to be as identical as possible to permit the highest measure of coupling possible. There is a transparent insulting cap between each set of elements embedded in the structure to permit the passage of light. They are designed with very small response times in such a way that they can be used to transmit data in the MHz range.

The rigid structure of this package permits one – way transfer of the electrical signals from the LED to the photodetector, without any electrical connection between the input and output circuitry. The extent of isolation between input and output depends on the kind of material in the light path and on the distance between the light emitter and the light detector.

The schematic diagrams for a **photodiode, photo – Darlington pair** and **photo SCR optoisolator** are illustrated.

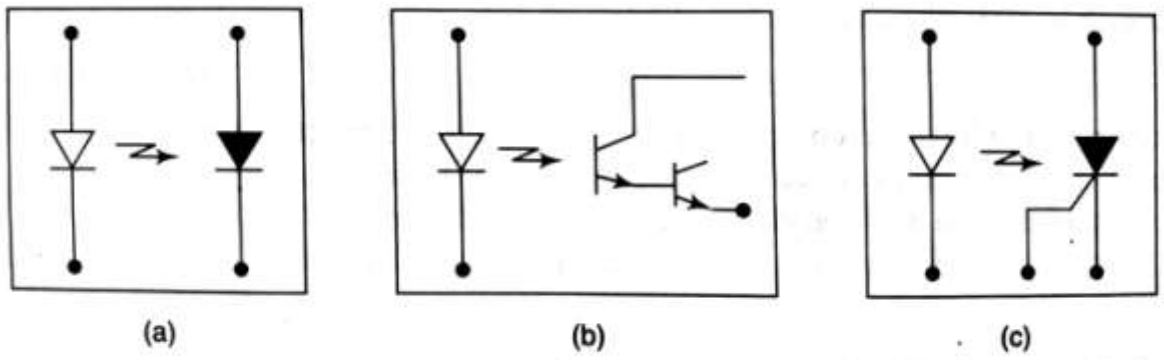

Fig. 5.35 *Optoisolators: (a) Photodiode (b) Photo-darlington (c) Photo-SCR*

PHOTOVOLTAIC CELL / SOLAR CELL

Photovoltaic Effect

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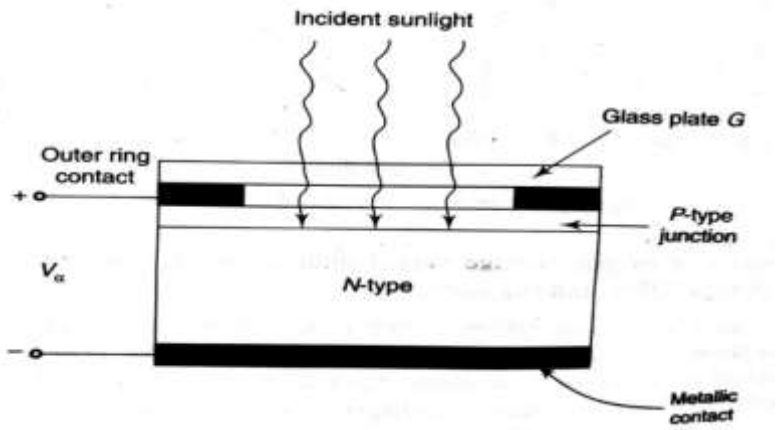
- PN junction is Open Circuited.
- Photovoltaic Cell – converted into electrical energy

If the PN junction is **open circuited**, the light energy is used to create a potential difference which is proportional to the frequency and intensity of the incident light. This phenomenon is called photovoltaic effect.

When light is incident on a **photovoltaic cell**, it is converted into electrical energy. Such an energy converter is called Solar Cell or Solar Cell and is used I satellites to provide the electrical power.



CHARGE COUPLED DEVICE (CCD)

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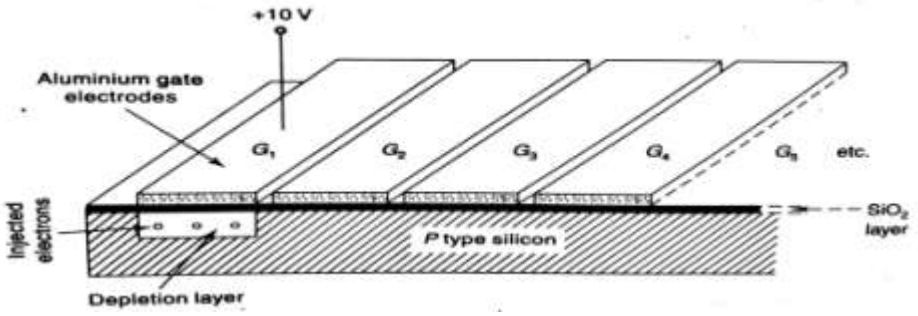
- Shift Register
- Store & Transfer
- Three – phase clocked voltage pulse.

A charge coupled device is a **shift register** formed by a string of closely spaced MOS capacitors. A CCD can store and transfer analog signals, either electrons or holes, which may be introduced electrically or optically. A cross – sectional view of a three phase charge – coupled device is illustrated. The structure consists of a series of metal gate electrodes, separated from a P – (or an – N) type semiconducting silicon substrate by a thin silicon dioxide layer. On top of the silicon dioxide layer is an array of metallised electrodes which are connected to signal voltages V_1, V_2, V_3.

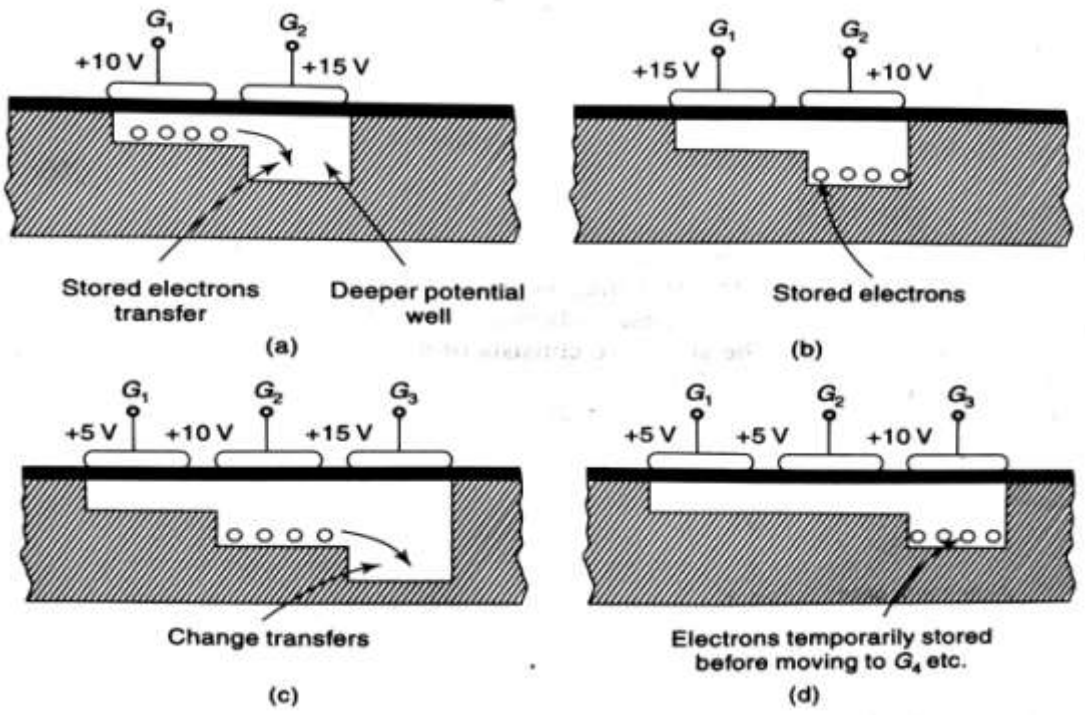


A **three – phase clocked voltage pulse system** is applied to the gates ensures that the charge is transferred serially between gates and its direction is controlled, as given below.

First Phase: A positive voltage V_1, say +10V to G_1, where $V_1$is greater than either V_2 or V_3, a depletion layer is formed, in typically less than 1μs. This produces the potential well into which information, in the form of minority electrons, is stored.

Second Phase: The adjacent gate G_2 is biased to a greater positive voltage V_2, say +15V, to produce a deeper well under it. The stored charge then transfers into the deeper potential well by diffusion down the potential gradient, which incidentally can be a relatively slow process. In order to ensure the charge transfer, the potential wells must physically overlap for which the spacing between neighbouring gates must be as small as possible. The charge is then completely stored in the well under G_2 and hence, the voltage on G_1 is reduced to a low value, say +5V and that on G_2 to a sustaining level of say +10V.

Third Phase: +15V voltage pulse to the next gate G_3 and the charge is transferred from G_2 to well under it. The voltages G_2 and G_3 can be relaxed as before to complete one cycle of the clock frequency. The charge has been transferred from under G_1 to under G_3 in one cycle of the clocked three phase pulse which causes a series of voltages in the sequences of +15, +10, +5, +15, etc., to be applied to each gate electrode.



Applications:

- CCD can be used as memories by storing charge corresponding to full and empty wells.
- In solid state imaging, the light may be shown in the CCD, either from top or the bottom through a tinned substrate.
- Dynamic Shift registers in computers
- Solid State imaging, such as video cameras.