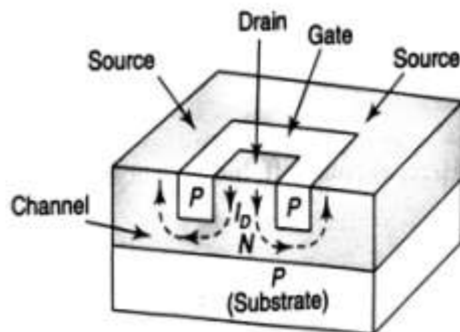
CHARACTERISTIC PARAMETERS OF JFET

In a JFET, the drain current I_D depends upon the drain voltage V_{DS} and the gate voltage V_{GS}. Any one of these variables may be fixed and the relation between the other two is determined. These relations are determined by the three parameters.

i. Mutual Conductance or Transconductance, g_m
ii. Drain Resistance, r_d
iii. Amplification Factor, μ
iv. Relationship among FET parameters
v. Power Dissipation, P_D
vi. Pinch – off Voltage, V_P

vi. Pinch – off Voltage, V_p

A single ended geometry junction FET is shown in the Fig. in which the diffusion is done from one side only. The substrate is of P – type material which is epitaxially grown on an N – type channel.



P – type gate material is then diffused into the N – type channel. The substrate functions as a second gate which is of relatively low resistivity material. The diffused gate is also of very low resistivity material.

A slab of N – type semiconductor is sandwiched between two layers of P – type material forming two PN junctions in this device.

P – type region – doped with N_A acceptor atoms

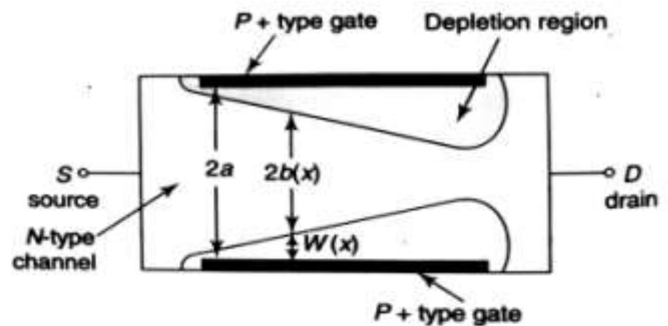
N – type region – doped with N_D donor atoms

Assumption: Acceptor impurity is much larger than the donor density, then the depletion region width will be much smaller than depletion region width of the N – region.

$$N_A \gg N_D, then\ W_P \ll W_N\ and\ W_P = W$$

The barrier potential is represents a reverse voltage, it is lowered by an applied forward voltage V(x) at x and it is expressed as $V_B = V_P - V(x)$. Now the space charge width, $W_n(x) = W(x)$ at a distance x along the channel.

$$W(x) = a - b(x) = \left\{\frac{2\varepsilon}{qN_D}[V_o - V(x)]\right\}$$



ε – Dielectric constant of channel material

q – Magnitude of electronic charge

V_0 – Junction contact potential

V(x) – applied potential across the space charge region at a distance x

a – metallurgical channel thickness between the substrate and P^+ gate region

W(x) – depletion region into the channel at a point x along channel.

If the drain current is zero, b(x) and V(x) are independent of x and hence b(x) =b.

The pinch off voltage V_P can be obtained as

$$|V_P| = \frac{qN_D}{2\varepsilon} a^2$$

Here at pinch – off, the depletion width $W_{PO} = (2\varepsilon/(qN_D)V_{GS})^{1/2}$

Therefore the gate - to – source voltage is

$$V_{GS} = (1 - \frac{b}{a})^2 V_P$$

EXPRESSION FOR SATURATION DRAIN CURRENT

For the transfer characteristics, V_{DS} is maintained constant at a suitable value greater than the pinch off voltage V_P. The gate voltage V_{GS} is decreased from zero till I_D is reduced to zero. The transfer characteristics I_D versus V_{GS} are shown. The shape of the transfer characteristics is very nearly a parabola,

$$I_D = I_{DSS}\left(1-\frac{V_{GS}}{V_p}\right) \longrightarrow (1)$$

$$I_{DS} - Satiration\ Drain\ Current$$

$$I_{DSS}\ is\ the\ value\ of\ I_{DS}\ when\ = 0, and\ V_P\ is\ the\ pinch-off\ voltage.$$

$$The\ expression\ for\ the\ drain\ current\ in\ saturation\ region\ is\ derived.$$

Differentiating the above equation w.r.t to V_{GS} we can obtain an expression for g_m

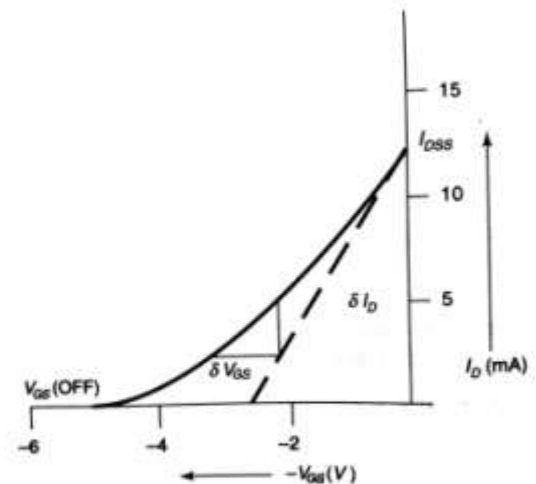
$$\frac{\delta I_{DS}}{\delta V_{GS}} = I_{DSS} * 2\left(1-\frac{V_{GS}}{V_P}\right)\left(-\frac{1}{V_P}\right) \longrightarrow (2)$$

We know that $g_m = \frac{\delta I_{DS}}{\delta V_{GS}}, V_{DS}\ is\ constant$

Therefore, $$g_m = -\frac{2I_{DSS}}{V_P}\left(1-\frac{V_{GS}}{V_P}\right) \longrightarrow (3)$$

Now from Eqn (1), we have

$$\left(1-\frac{V_{GS}}{V_P}\right) = \sqrt{\frac{I_{DS}}{I_{DSS}}}$$



Substituting this value in Eqn (3), we get

$$g_m = -\frac{-2\sqrt{I_{DS}I_{DSS}}}{V_P}$$

Suppose $g_m = g_{mo}, when\ V_{GS} = 0$, then from eqn (3)

$$g_{mo} = -\frac{2I_{DSS}}{V_P}$$

Therefore from Eqn (3) & (4) we get,

$$\boxed{g_m = g_{mo}\left(1-\frac{V_{GS}}{V_P}\right)}$$

APPLICATIONS OF JFET

FET is

- Used as a **buffer in measuring instruments**, receivers since it has high input impedance and low output admittance
- Used in **RF amplifiers** in FM tuners and in communication equipment for its low noise level.
- Used in **cascade amplifiers in measuring and test equipment's**, since the input capacitance is low
- Used as a **voltage variable resistor** in operational amplifier and tone controls
- Used in **mixer circuits in FM and TV receivers**, and in communication equipment because inter modulation distortion is low.

COMPARISON BETWEEN JFET AND BJT

JFET	BJT
Operation depends on the **flow of majority carriers - Holes for P – Channel & Electrons for N – Channel** - Unipolar Devices	Operation depends on **both minority and majority current carriers**
No Junctions. Less noisy	More Noisy
Higher Input impedance & Lower output impedance	Low input impedance
Voltage Controlled Device, i.e., voltage at the input terminal controls the output current.	**Current Controlled Device**, i.e., input current controls the output current.
Easier to fabricate and they occupy lesser in space	Fabrication is quite difficult and occupies a larger space area.
Tolerate much higher level of radiation since they do not rely on minority carriers for operation.	Degraded by neutron radiation because of reduction in minority carrier life times.
Costlier to Manufacture compared to BJT	Cheaper
Does not suffer from Minority carrier storage effects and therefore have higher switching speeds & cut – off frequencies.	**Suffers from Minority carrier storage effects** and therefore have lower switching speeds & cut – off frequencies
Negative temperature coefficient at high current levels, it prevents from thermal breakdown.	**Positive temperature coefficient** at high current levels, which leads to thermal breakdown.

EFFECT OF CHANNEL LENGTH MODULATION

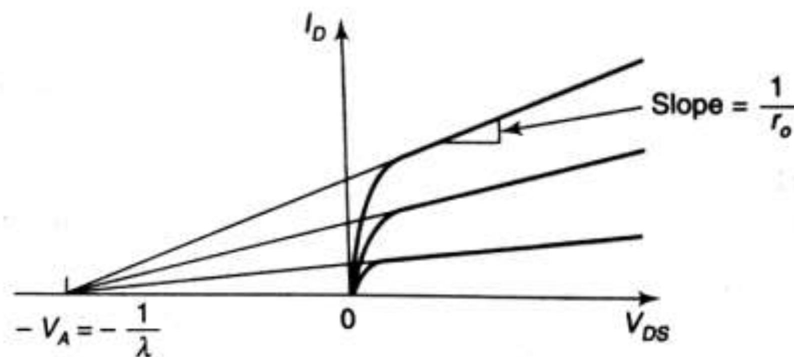
In MOSFET Characteristics a non – zero slope exists beyond the saturation point. For the saturation region, i.e., (V_{DS}>$V_{DS(sat)}$), the effective channel length decreases and this phenomenon is called channel length modulation. For an N – channel device the slope of the curve in the saturation region can be expressed by using the drain current I_D given by

$$\boldsymbol{I_D = K_N\ (V_{GS} - V_{TN})^2(1 + \lambda V_{DS})}$$

$$\lambda - Positive\ quantity\ called\ th\ channel\ Lenght\ Modulation$$

$$K_N - Conduction\ \ Parameter$$

$$V_{TN} - Threshold\ Voltage$$



Effect of Channel Length Modulation due to non – zero slope in the saturation region, resulting in a finite output resistance

The output resistance due to the channel length modulation is expressed by

$$r_o = \left(\frac{\partial I_D}{\partial V_{DS}}\right)\ V_{GS}\ is\ constant$$

The output resistance can be determined at the Q – point by

$$r_o = [\lambda K_N (V_{GSQ} - V_{TN})^2]^{-1}$$

$$= \left[\lambda I_{DSS}\left(1 - \frac{V_{GSQ}}{V_P}\right)^2\right]^{-1}$$

$$r_O \cong [\lambda I_{DQ}]^{-1} = \frac{1}{\lambda I_{DQ}} = \frac{V_E}{I_{DQ}}$$

The output resistance is an important factor in the analysis of small signal equivalent circuit of MOSFET.

THRESHOLD VOLTAGE IN MOSFET

Threshold voltage is the applied gate voltage **needed to achieve the threshold inversion point.** The **condition to achieve the threshold inversion point** is that the surface potential,

$$\Phi_s = 2\Phi_{fp} \text{ For P – type semiconductor}$$

$$\Phi_s = 2\Phi_{fn} \text{ For N – type semiconductor}$$

$$\Phi_{fp} - Difference\ in\ potential\ between\ the\ fermi\ energy\ levels\ for\ P - type$$

$$\Phi_{fn} - Difference\ in\ potential\ between\ the\ fermi\ energy\ levels\ for\ N - type$$

The potential Φ_{fp} for P – type semiconductor is given by

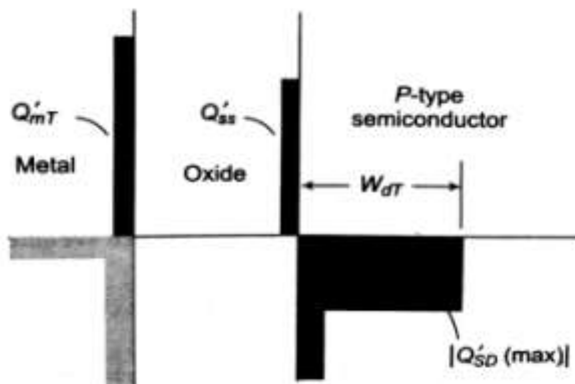
$$\Phi_{fp} = V_T ln\left(\frac{N_A}{n_i}\right)$$

$$V_T = \frac{kT}{q} = 26mV\ at\ room\ temperature.$$

$$N_A - acceptor\ doping\ concentration$$

$$n_i - intrinsic\ carrier\ concentration$$

Figure shows the charge distribution in the MOS capacitor at the threshold inversion point for a P – type semiconductor substrate. Consider the space charge width reaches its maximum value.



The space charge width is given by

$$W_d = \left\{\frac{2\varepsilon_s \Phi_s}{qN_A}\right\}^{1/2}$$

$$\varepsilon_s - permittivity\ of\ the\ semiconductor$$

$$q - chrage\ of\ an\ electron$$

Conservation of Charge can be written as

$$Q_{mT} + Q_{ss} = |Q_{SD}(\text{max})|$$

$|Q_{SD}(\text{max})|$
$- magnitude\ of\ the\ maximum\ space\ charge\ density\ per\ unit\ area\ of\ the\ depletion\ region$

$$|Q_{SD}(\text{max})| = qN_A W_{dT}$$

$$W_{dT} - maximum\ charge\ width$$

If the gate voltage is applied, the voltage across the oxide, V_{ox}, and the surface potential, Φ_s will change. Therefore

$$\boldsymbol{V_G = \Delta V_{OX} + \Delta\Phi_s = V_{OX} + \Phi_S + \Phi_{ms}}$$

$$\Phi_{ms} - metal - semicondcutor\ work\ function\ potential\ difference$$

MOSFET	**JFET**
In Enhancement and Depletion types of MOSFET, the **transverse electric field** induced across an insulating Layer deposited on the semiconductor material controls the conductivity of the channel.	The **transverse electric field** induced across the reverse biased PN junction controls the conductivity of the channel.

Gate leakage current is of the order of 10^{-12}A. Hence the input resistance of MOSFET is very high in the order of 10^{10} to 10^{15} Ω.	**Gate leakage current** of a JFET is of the order of 10^{-9}A and its input resistance is of the order of 10^{8}.
The depletion type MOSFET can be operated in both depletion and enhancement mode.	JFET's are operation only in the depletion mode.
MOSFET's are quite **easier to fabricate**, comparing to JFET	
MOSFET is very susceptible to overload voltage and needs special handling during installation. It gets damaged easily if it is not properly handled.	

DUAL - GATE MOSFETS

Construction

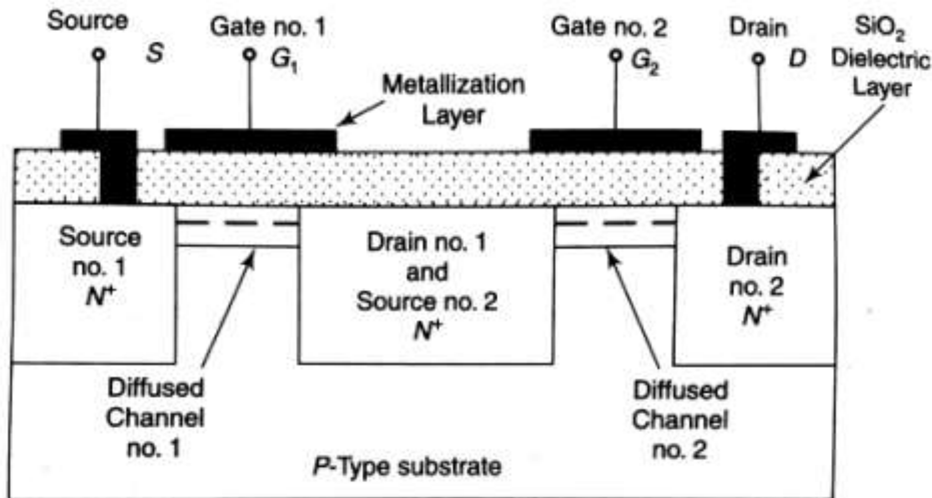
The operation of conventional MOSFET is limited at high frequencies by its high gate – to – channel capacitance. The metal plate used for the gate is a conductor. The silicon dioxide between the gate and channel is a dielectric layer. Since the channel itself is considered a conductor, the combination of the three forms a capacitor.

In dual – gate MOSFET, **two gate terminals** are provided as compared to a conventional single – gate MOSFET. A dual – gate MOSFET uses two gates **to reduce the overall high gate – to – channel capacitance at high frequencies**. The voltage at both the gate terminals controls the flow of current through the MOSFET. The dual – gate MOSFET can be considered the counterpart of a tetrode as the control is exerted by two gates similar to a tetrode.

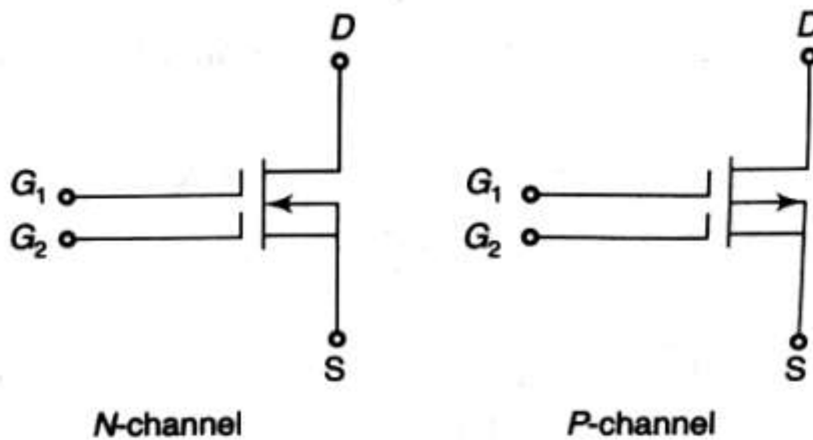
The physical construction of an N – channel dual – gate MOSFET is shown as below and the schematic symbols for both N – channel and P – channel are shown.

The device is normally wired so that the two gates are in series. Here, the **N^+ region in the middle acts as drain for MOSFET – 1 and source for MOSFET** – 2. When the dual – gate MOSFET is used as two series MOSFETs, the effect is similar to connecting two capacitor in

series. As the total capacitance in a series combination is less than either individual value, by connecting the two gates in series, the overall capacitance is reduced.



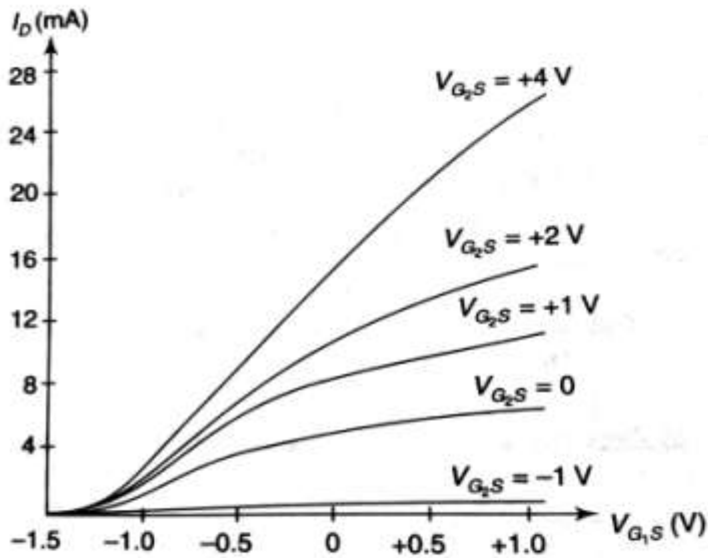
N – Channel dual gate MOSFET



Schematic symbols for N – channel and P – channel MOSFET

Operation

In the N – channel dual – gate MOSFET, the voltages at both the gate terminals control the flow of current. When the voltages applied to the gate terminals such as gate – 1 and gate – 2 are greater than threshold voltage, a channel is formed between the corresponding source and drain. When the gate voltage of either of the two terminals is made negative, the drain current decreases. The drain current gets enhanced when the gate voltage applied both gate terminals are made positive. The transfer characteristics of the dual – gate N – channel MOSFET are shown.



Applications

At high frequencies, the conventional MOSFET has high gate – to – channel capacitance. This capacitance is a result of metal – oxide – semiconductor layers.

Dual – gate MOSFET reduces the overall gate – to – channel capacitance because the total series capacitance is lower than either individual capacitance.

- Due to simultaneous control of two gate voltages, the dual – gate MOSFET has wide applications in mixers, demodulators, cascade amplifier, RF amplifier and AGC amplifiers.