JEPPIAAR INSTITUTE OF TECHNOLOGY

"Self-Belief | Self Discipline | Self Respect"

DEPARTMENT

OF

ELECTRONICS AND COMMUNICATION ENGINEERING

LECTURE NOTES

EC8453 – LINEAR INTEGRATED CIRCUITS

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UNIT V WAVEFORM GENERATORS AND SPECIAL FUNCTION ICS 9

Sine-wave generators, Multivibrators and Triangular wave generator, Saw-tooth wave generator, ICL8038 function generator, Timer IC 555, IC Voltage regulators – Three terminal fixed and adjustable voltage regulators - IC 723 general purpose regulator - Monolithic switching regulator, Low Drop – Out(LDO) Regulators - Switched capacitor filter IC MF10, Frequency to Voltage and Voltage to Frequency converters, Audio Power amplifier, Video Amplifier, Isolation Amplifier, Opto-couplers and fibre optic IC.

Basics Of Oscillators: Criteria for oscillation:

The canonical form of a feedback system is shown in Figure 5 . 1, and Equation 1 describes the performance of any feedback system (an amplifier with passive feedback Components constitute a feedback system).

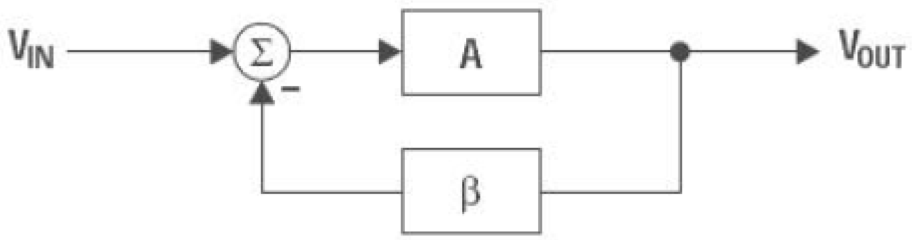


Fig. 5.1 Canonical form of feedback circuit

$$\frac{V_{OUT}}{V_{IN}} = \frac{A}{1 + A\beta} \qquad \textbf{(1)}$$

Oscillation results from an unstable state; i.e., the feedback system can't find a stable state because its transfer function can't be satisfied. Equation 1 becomes unstable when (1+Aβ) = 0 because A/0 is an undefined state. Thus, the key to designing an oscillator is to insure that Aβ = –1 (called the Barkhausen criterion), or using complex math the equivalent expression is Aβ = 1 –180°. The 180° phase shift criterion applies to negative feedback systems, and 0° phase shift applies to
positive feedback systems.

The output voltage of a feedback system heads for infinite voltage when Aβ = –1. When the output voltage approaches either power rail, the active devices in the amplifiers change gain, causing the value of A to change so the value of Aβ ≠1; thus, the charge to infinite voltage slows down and eventually halts. At this point one of three things can occur.

First, nonlinearity in saturation or cutoff can cause the system to become stable and lock up. Second, the initial charge can cause the system to saturate (or cut off) and stay that way for a long time before it becomes linear and heads for the opposite power rail.

Third, the system stays linear and reverses direction, heading for the opposite power rail. Alternative two produces highly distorted oscillations (usually quasi square waves), and the resulting oscillators are called relaxation oscillators. Alternative three produces sine wave oscillators.

✓ **Phase Shift in Oscillators:**

The 180° phase shift in the equation Aβ = 1 –180° is introduced by active and passive components. The phase shift contributed by active components is minimized because it varies with temperature, has a wide initial tolerance, and is device dependent.
Amplifiers are selected such that they contribute little or no phase shift at the oscillation frequency. A single pole RL or RC circuit contributes up to 90° phase shift per pole, and because 180° is required for oscillation, at least two poles must be used in oscillator design. An LC circuit has two poles; thus, it contributes up to 180° phase shift per pole pair, but LC and LR oscillators are not considered here because low frequency inductors are expensive, heavy, bulky, and non-ideal. LC oscillators are designed in high frequency applications beyond the frequency range of voltage feedback op amps, where the inductor size, weight, and cost are less significant.
Multiple RC sections are used in low-frequency oscillator design in lieu of inductors.
Phase shift determines the oscillation frequency because the circuit oscillates at the frequency that accumulates –180° phase shift. The rate of change of phase with frequency, dS/dt, determines frequency stability.
When buffered RC sections (an op amp buffer provides high input and low output impedance) are cascaded, the phase shift multiplies by the number of sections, n (see Figure 2).
Although two cascaded RC sections provide 180° phase shift, dS/dt at the oscillator frequency is low, thus oscillators made with two cascaded RC sections have poor frequency stability. Three equal cascaded RC filter sections have a higher dS/dt, and the resulting oscillator has improved frequency stability.
Adding a fourth RC section produces an oscillator with an excellent dS/dt, thus this is the most stable oscillator configuration. Four sections are the maximum number used

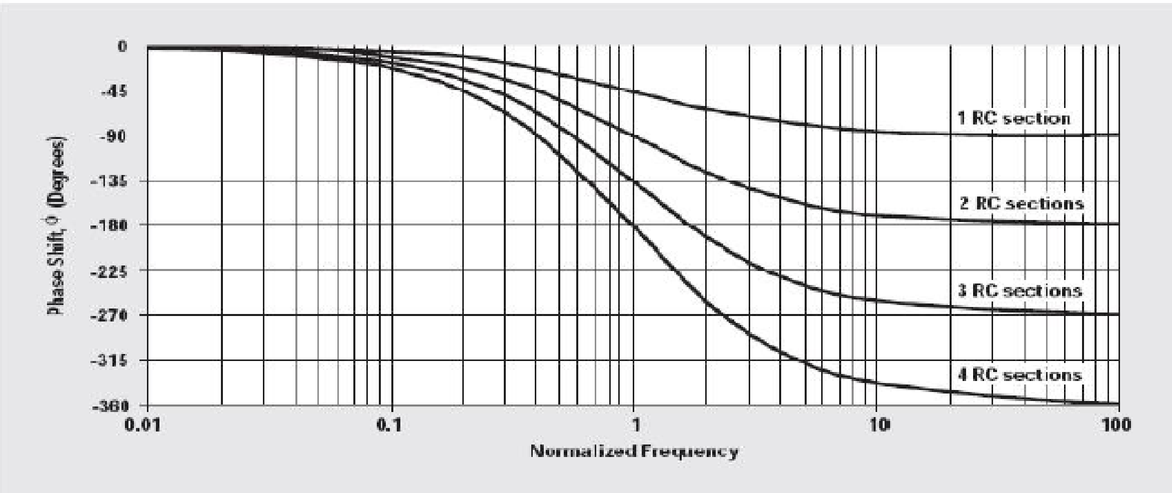


Figure 5.2 Phase plot of RC sections

because op amps come in quad packages, and the four-section oscillator yields four sine waves that are 45° phase shifted relative to each other, so this oscillator can be used to obtain sine/cosine or quadrature sine waves.

Applications

Crystal or ceramic resonators make the most stable oscillators because resonators have an extremely high dS/dt resulting from their non-linear properties.

Resonators are used for high- frequency oscillators, but low-frequency oscillators do not use resonators because of size, weight, and cost restrictions.
Op amps are not used with crystal or ceramic resonator oscillators because op amps have low bandwidth. It is more cost-effective to build a high- frequency crystal oscillator and count down the output to obtain a low frequency than it is to use a low-frequency resonator.

Gain in Oscillators:

The oscillator gain must equal one (Aβ = 1–180°) at the oscillation frequency. The circuit becomes stable when the gain exceeds one and oscillations cease. When the gain exceeds one with a phase shift of –180°, the active device non-linearity reduces the gain to one.
The non-linearity happens when the amplifier swings close to either power rail because cutoff or saturation reduces the active device (transistor) gain. The paradox is that worst-case design practice requires nominal gains exceeding one for manufacturability, but excess gain causes more distortion of the output sine wave.
When the gain is too low, oscillations cease under worst-case conditions, and when the gain is too high, the output wave form looks more like a square wave than a sine wave. Distortion is a direct result of excess gain overdriving the amplifier; thus, gain must be carefully controlled in low distortion oscillators.
Phase-shift oscillators have distortion, but they achieve low-distortion output voltages because cascaded RC sections act as distortion filters. Also, buffered phase-shift oscillators have low distortion because the gain is controlled and distributed among the buffers.

5.1 Sine Wave Generators (Oscillators)

Sine wave oscillator circuits use phase shifting techniques that usually employ
- Two RC tuning networks, and
- Complex amplitude limiting circuitry

5.1.1 RC Phase Shift Oscillator

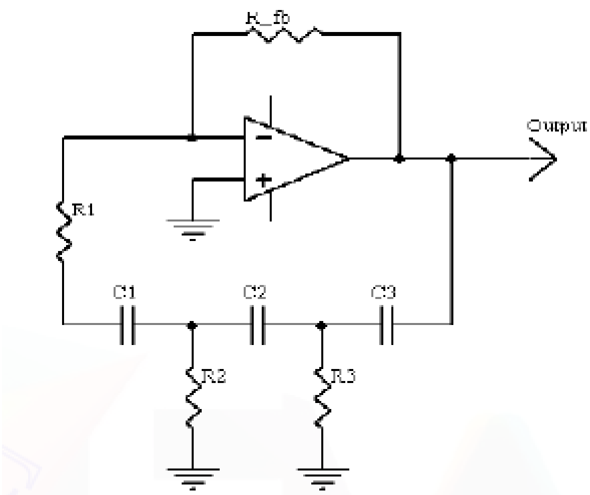


Fig.5.3 RC Phase shift oscillator

RC phase shift oscillator using op-amp in inverting amplifier introduces the phase shift of 180 between input and output. The feedback network consists of 3 RC sections each producing 60 phase shift. Such a RC phase shift oscillator using op-amp is shown in the figure.

The output of amplifier is given to feedback network. The output of feedback network drives the amplifier. The total phase shift around a loop is 1800 of amplifier and 180 due to 3 RC sections, thus 360 . This satisfies the required condition for positive feedback and circuit works as an oscillator.

$$f_{oscillation} = \frac{1}{2\pi\sqrt{R_2R_3(C_1C_2+C_1C_3+C_2C_3)+R_1R_3(C_1C_2+C_1C_3)+R_1R_2C_1C_2}}$$

Oscillation criterion:

$$R_{feedback} = 2(R_1+R_2+R_3)+\frac{2R_1R_3}{R_2}+\frac{C_2R_2+C_2R_3+C_3R_3}{C_1}$$

$$+\frac{2C_1R_1+C_1R_2+C_3R_3}{C_2}+\frac{2C_1R_1+2C_2R_1+C_1R_2+C_2R_2+C_2R_3}{C_3}$$

$$+\frac{C_1R_1^2+C_3R_1R_3}{C_2R_2}+\frac{C_2R_1R_3+C_1R_1^2}{C_3R_2}+\frac{C_1R_1^2+C_1R_1R_2+C_2R_1R_2}{C_3R_3}$$

$$A\beta - A\left(\frac{1}{RCs+1}\right)^3 \qquad (3)$$

The loop phase shift is –180° when the phase shift of each section is –60°, and this occurs when ω = 2πf = 1.732/RC because the tangent 60° = 1.73. The magnitude of β at this point is (1/2)3, so the gain, A, must be equal to 8 for the system gain to be equal to 1.

5.1.2 Wien Bridge Oscillator:

Figure 5. 3 give the Wien-bridge circuit configuration. The loop is broken at the positive input, and the return signal is calculated in Equation 2 below.

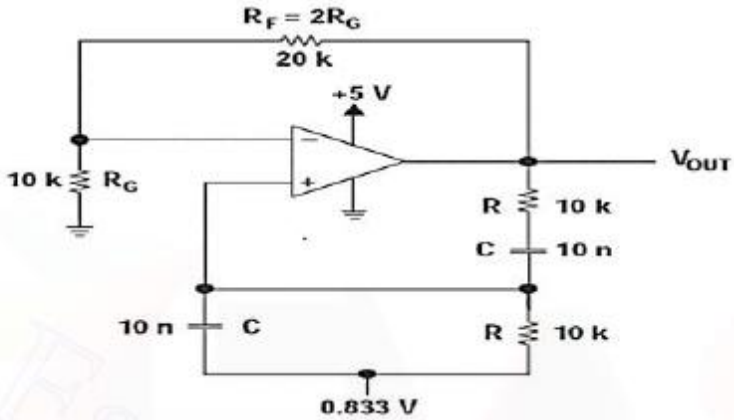


Fig.5.4 Wien Bridge Oscillator

$$\frac{V_{RETURN}}{V_{OUT}} = \frac{\frac{R}{RCs+1}}{\frac{R}{RCs+1} + R + \frac{1}{Cs}} = \frac{1}{3 + RCs + \frac{1}{RCs}} = \frac{1}{3 + j\left(RC\omega - \frac{1}{RC\omega}\right)}, \qquad (2)$$

where $s = j\omega$ and $j = \sqrt{-1}$.

When $\omega = 2\pi f = 1/RC$, the feedback is in phase (this is positive feedback), and the gain is 1/3, so oscillation requires an amplifier with a gain of 3. When RF = 2RG, the amplifier gain is 3 and oscillation occurs at $f = 1/2\pi RC$. The circuit oscillated at 1.65 kHz rather than 1.59 kHz with the component values shown in Figure 3, but the distortion is noticeable.

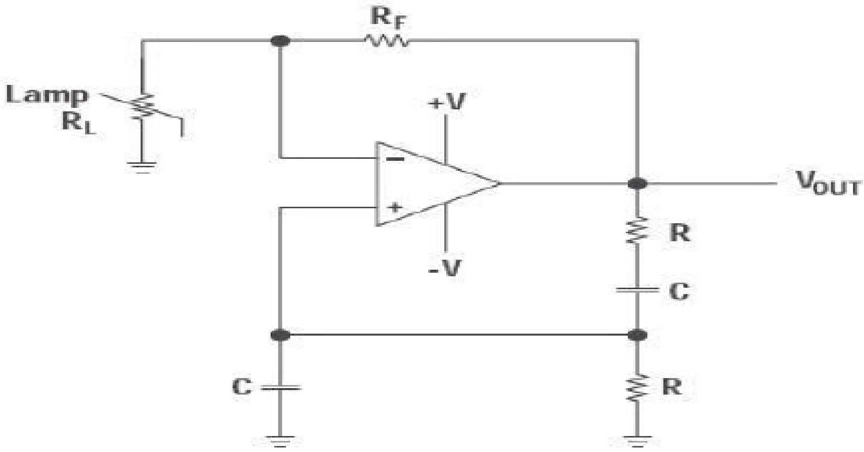


Fig.5.5 Wien Bridge Circuit Schematic with non-linear feedback

Figure 4 shows a Wien-bridge circuit with non-linear feedback. The lamp resistance, RL, is nominally selected as half the feedback resistance, RF, at the lamp current established by RF and RL. The non-linear relationship between the lamp current and resistance keeps output voltage changes small.

If a voltage source is applied directly to the input of an **ideal** amplifier with feedback, the input current will be:

$$i_{in} = \frac{v_{in} - v_{out}}{Z_f}$$

Where *vin* is the input voltage, *vout* is the output voltage, and *Zf* is the feedback impedance. If the voltage gain of the amplifier is defined as:

$$A_v = \frac{v_{out}}{v_{in}}$$

And the input admittance is defined as:

$$Y_i = \frac{i_{in}}{v_{in}}$$

Input admittance can be rewritten as:

$$Y_i \; \frac{1 - A_v}{Z_f}$$

For the Wien Bridge, *Zf* is given by:

$$Z_f = R + \frac{1}{j\omega C}$$

$$Y_i = \frac{(1 - A_v)(\omega^2 C^2 R + j\omega C)}{1 + (\omega C R)^2}$$

If *Av* is greater than 1, the input admittance is a negative resistance in parallel with an inductance The inductance is:

$$L_{in} = \frac{\omega^2 C^2 R^2 + 1}{\omega^2 C (A_v - 1)}$$

If a capacitor with the same value of *C* is placed in parallel with the input, the circuit has a natural resonance at:

$$\omega = \frac{1}{\sqrt{L_{in} C}}$$

Substituting and solving for inductance yields:

$$L_{in} - \frac{R^2 C}{A_v - 2}$$

If *Av* is chosen to be 3: $Lin = R^2 C$

Substituting this value yields:

$$\omega = \frac{1}{RC} \quad \text{Or} \quad f = \frac{1}{2\pi RC}$$

Similarly, the input resistance at the frequency above is: $R_{in} = \dfrac{-2R}{A_v - 1}$

For *Av* = 3: $Rin = -R$

If a resistor is placed in parallel with the amplifier input, it will cancel some of the negative resistance. If the net resistance is negative, amplitude will grow until clipping occurs. Similarly, if the net resistance is positive, oscillation amplitude will decay. If a resistance is added in parallel with exactly the value of *R*, the net resistance will be infinite and the circuit can sustain stable oscillation at any amplitude allowed by the amplifier. Increasing the gain makes the net resistance more negative, which increases amplitude. If gain is reduced to exactly 3 when suitable amplitude is reached, stable, low distortion oscillations will result. Amplitude stabilization circuits typically increase gain until suitable output amplitude is reached. As long as *R*, *C*, and the amplifier are linear, distortion will be minimal.

5.2 Multivibrators

5.2.1 Astable Multivibrator

The two states of circuit are only stable for a limited time and the circuit switches between them with the output alternating between positive and negative saturation values.

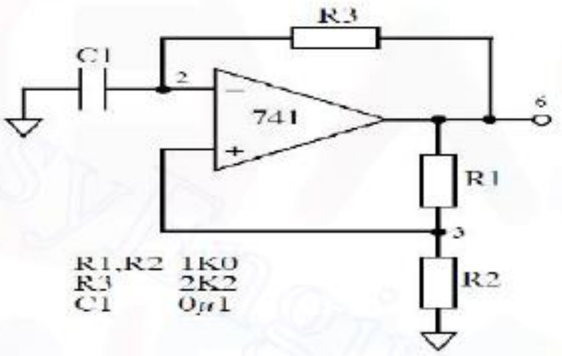


Fig. 5.6 Astable multivibrator circuit

Analysis of this circuit starts with the assumption that at time *t*=0 the output has just switched to state 1, and the transition would have occurred. An op-amp Astable multivibrator is also called as free running oscillator. The basic principle of generation of square wave is to force an op-amp to operate in the saturation
region (±Vsat).

A fraction β =R2/(R1+R2) of the output is feedback to the positive input terminal of op-amp. The charge in the capacitor increases & decreases upto a threshold value called ±βVsat.

The charge in the capacitor triggers the op-amp to stay either at +Vsat or –Vsat.

Asymmetrical square wave can also be generated with the help of Zener diodes. Astable multi vibrator do not require a external trigger pulse for its operation & output toggles from one state to another and does not contain a stable state. Astable multi vibrator is mainly used in timing applications & waveforms generators.

Design

1. The expression of fo is obtained from the charging period t1 & t2 of capacitor as

$$T=2RC\ln (R_1+2R_2)/R_1$$

2. To simplify the above expression, the value of R1 & R2 should be taken as

R2 = 1.16R

Such that fo simplifies to fo =1/2RC.

3. Assume the value of R1 and find R2.
4. Assume the value of C & Determine R from fo =1/2*R C*
5. Calculate the threshold point from βVSATl = *R*1lVTl/ *R*1-*R*2

l/βVSATl w h e r e β is the feedback ratio.

5.2.2 Monostable Multivibrator using Op-amp: circuit diagram:

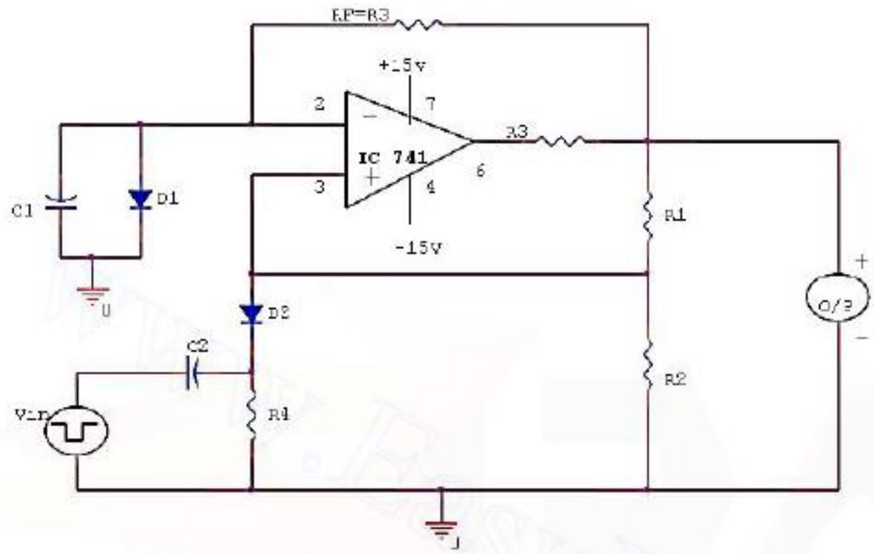


Fig.5.7 Mono stable Multi vibrator using Op-amp

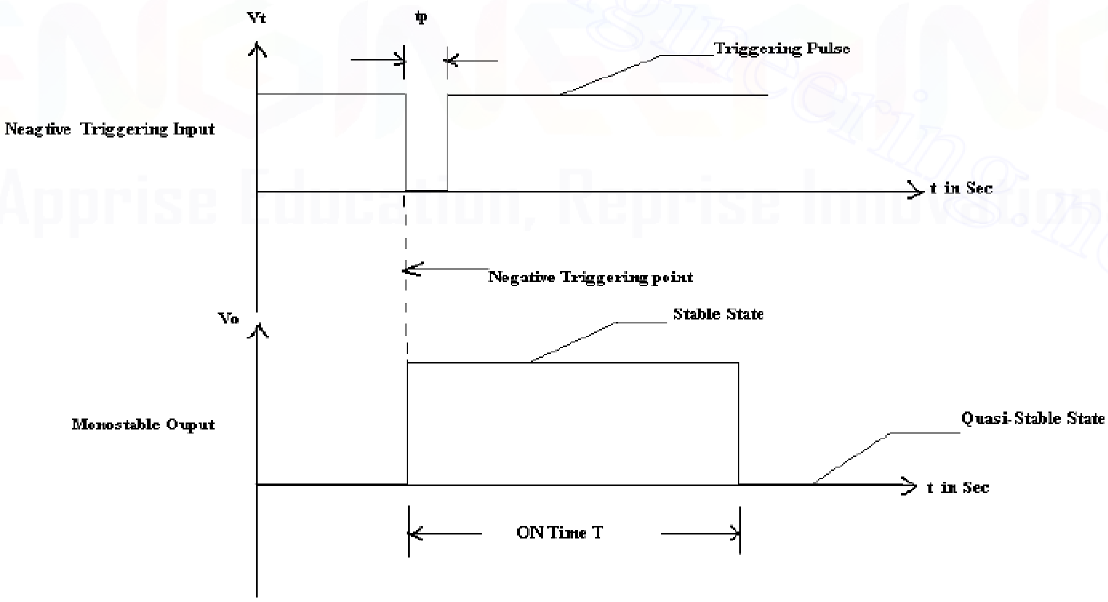


Fig.5.8 Input Output Waveform:

A multivibrator which has only one stable and the other is quasi stable state is called as Monostable multivibrator or one-short multivibrator. This circuit is useful for generating signal output pulse of adjustable time duration in response to a triggering signal. The width of the output pulse depends only on the external components connected to the opamp. Usually a negative trigger pulse is given to make the output switch to other state. But, it then return to its stable state after a time interval determining by circuit components. The pulse width T can be given as T = 0.69RC. For Monostable operation the triggering pulse width Tp should be less then T, the pulse width of Monostable multivibrator. This circuit is also called as time delay circuit or gating circuit.

Design:

1. Calculating β from expression

$$\beta = \frac{R1}{R1 + R2}$$

2. The value of R & C from the pulse width time expression.

$$T = RC \ln \frac{(1 + V_D / V_{sat})}{1 - \beta}$$

$$T = RC \ln \frac{(1 + V_D / V_{sat})}{0.5}$$

$$T = 0.69RC.$$

3. Triggering pulse width T_p must be much smaller then T. $T_p < T$.

5.2.3 Triangular Wave Generator Circuit:

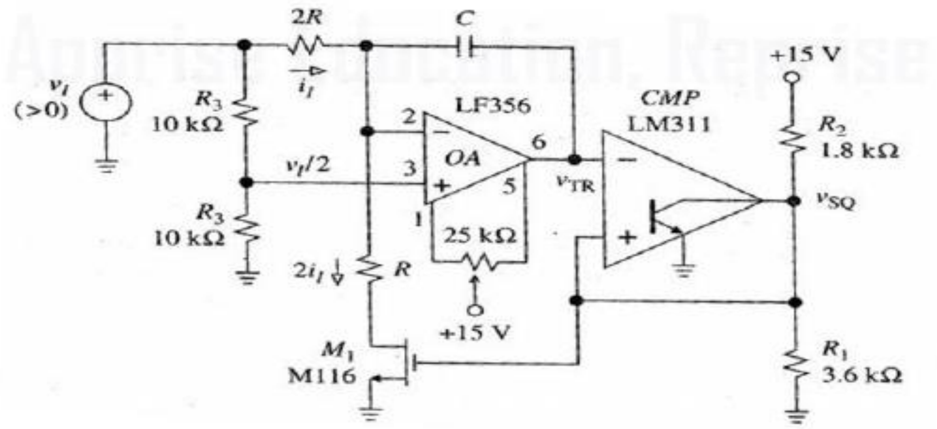


Fig. 5.9 Circuit diagram of Triangular waveform generator

This signal generator gives two waveforms: a triangle-wave and a square- wave. The central component of this circuit is the integrator capacitor CI. Basically we are interested in performing two functions on CI: *charge it, discharge it - repeat indefinitely*. The output waveforms are shown here and it is apparent that a square wave generator followed by an integrator acts as a triangular wave generator.

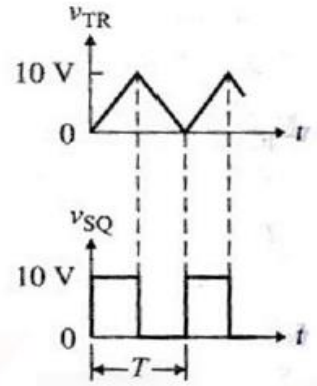


Fig.5.10 Output waveforms from generator

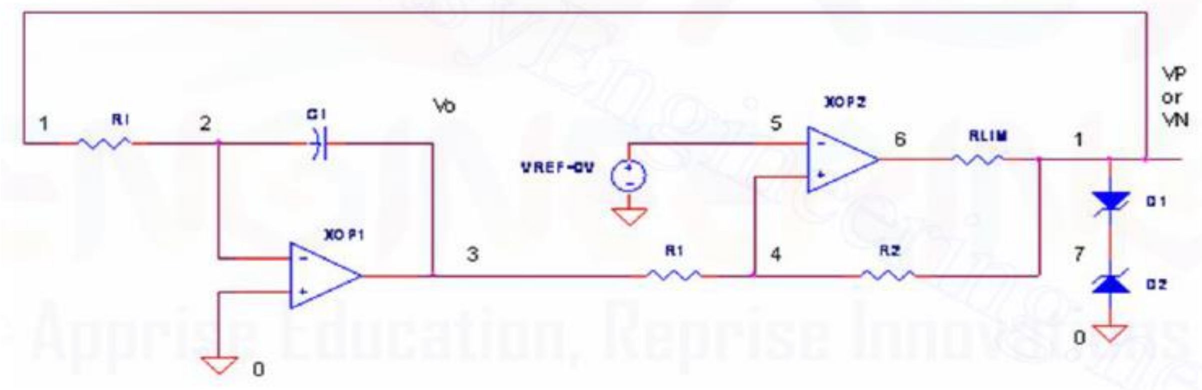


Fig. 5.11 Basic triangular waveform generator

The triangle peaks and period may not accurately meet +/-10V swing at 100 us. The main reason is that current source and thresholds are derived from Zener diodes - not exactly the most accurate reference.

5.2.4 Linear Ramp Generator

A triangle wave implies that the circuit generates a linear voltage ramp. One way to achieve this goal is by charging discharging CI with a constant current. The Op Amp Integrator provides f o r this.

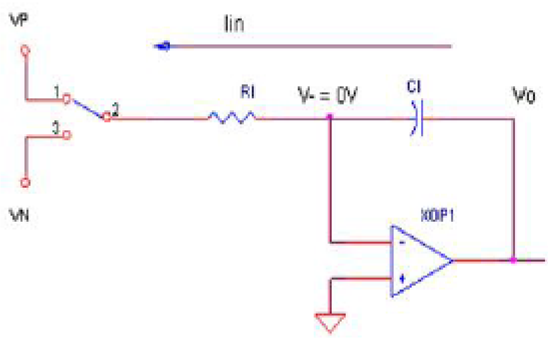


Fig. 5.12 Linear Ramp Generator

Ramp Up

Connect R_I to V_N and With V- held at the virtual ground (0V), a constant current flows from V- to V_N.

$I_{in} = V_N / R_I$.
CI integrates Iin creating a positive linear ramp at Vo. The ramp is linear because Vo changes proportionally to the time elapsed ΔT.
$\Delta V_o = - V_N / (C_I \cdot R_I) \cdot \Delta T$
Ramp Down Connect RI to V_P and constant current flows from V_P to V-,
$Iin = - V_P / R_I$.
Now Vo ramps down linearly $\Delta Vo = - V_P / (C_I \cdot R_I) \cdot \Delta T$
Ramp Up:$\Delta V_o/\Delta T= -V_N/(C_I R_I)$
Ramp Down:$\Delta Vo /\Delta T = - V_P / (C_I \cdot R_I)$
These equations show the parameters available to control the ramp up / down speeds.
Asymmetrical voltage swings are got by including a reference voltage VREF to the comparator's negative input.
$V_{th}+ =V_{REF}\cdot(R_1+R_2)/R_2-V_N\cdot R_1/R_2$
$V_{th}- = V_{REF} \cdot (R_1+R_2)/R_2 -V_P \cdot R_1 / R_2$

Upper and Lower Bounds

When do we switch from charging to discharging CI? Basically, there is a need to pick two levels - *an upper and a lower threshold* - to define the bounds of the triangle wave. The circuit ramps up or down, reversing at the upper and lower thresholds.

- With one leg of RI at VN, the output **ramps up** until the **Upper Threshold (Vth+)** is reached. Then RI is switched from VN to VP.
- With one leg of RI at VP, the output **ramps down** until the **Lower Threshold (Vth-)** is reached. Then RI is switched from VP to VN.

Comparator:

An Op Amp Comparator with two thresholds. Produce circuit changes in output state from VN to VP (or vice-versa) depending on the upper Vth+ and lower Vth- thresholds.
$Vth+=-V_N\cdot R_1/R_2$
$Vth- = -V_P \cdot R_1 / R_2$

Comparator Working:

- When Vin > Vth+, the output switches to VP, the POSITIVE output state.
- When Vin < Vth-, the output switches to VN, the NEGATIVE output state.

Zener diodes D1 and D2 set the positive and negative output levels:
$V_P=V_{fD1}+V_{ZD2}$ $V_N = V_{fD2} + V_{ZD1}$.
These output levels do double duty - they set the comparator thresholds, and set the voltage levels for the next stage - the integrator.

5.3 Saw-Tooth Wave Generator

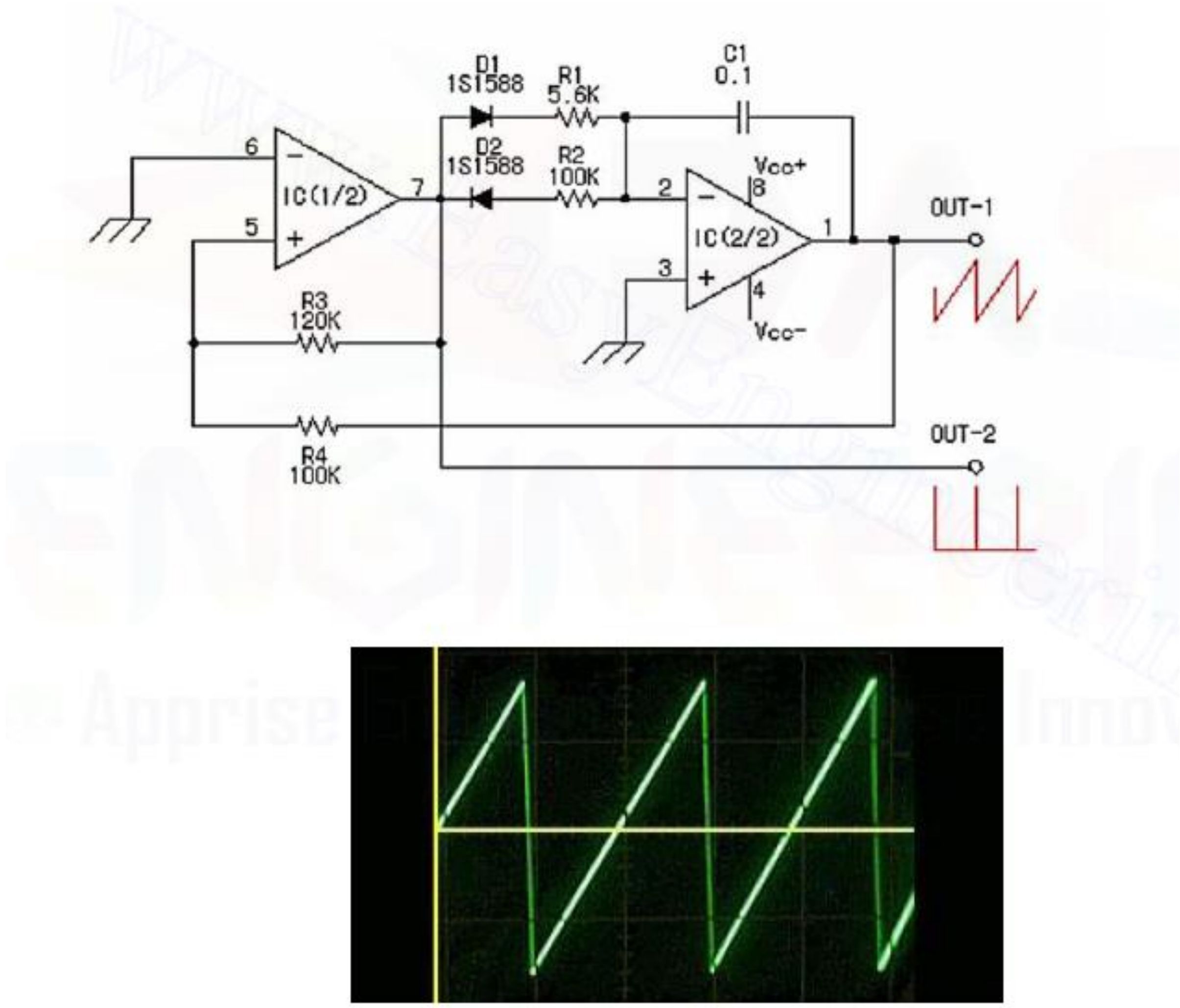


Fig. 5.13 Saw-Tooth Wave Generator Circuit Diagram and output waveform

The saw tooth wave oscillator which used the operational amplifier. The composition of this circuit is the same as the triangular wave oscillator basically and is using two operational amplifiers.

At the circuit diagram above, IC(1/2) is the Schmitt circuit and IC(2/2) is the Integration circuit. The difference with the triangular wave oscillator is to be changing the time of the charging and the discharging of the capacitor. When the output of IC (1/2) is positive voltage, it charges rapidly by the small resistance (R1) value.

(When the integration output voltage falls) When the output of IC(1/2) is negative voltage, it is made to charge gradually at the big resistance(R2) value. The output waveform of the integration circuit becomes a form like the tooth of the saw. Such voltage is used for the control of the electron beam (the scanning line) of the television,

When picturing a picture at the cathode-ray tube, an electron beam is moved comparative slow. (When the electron beam moves from the left to the right on the screen). When turning back, it is rapidly moved.(When moving from the right to the left).

Like the triangular wave oscillator, the line voltage needs both of the positive power supply and the negative power supply. Also, to work in the oscillation, the condition of R3>R4 is

necessary. However, when making the value of R4 small compared with R3, the output voltage becomes small. The near value is good for R3 and R4
The oscillation frequency can be calculated by the following formula.

$$f = \frac{1}{2C\,(R_1+R_2)}\left(\frac{R_3}{R_4}\right)$$

With the circuit diagram,the oscillation frequency is as follows.
f = (1/2C (R1+R2))*(R3/R4)
= (1/(2x0.1x10-6x(5.6x103+100x103))x(120x103/100x103)
= (1/(21.12x10-3))x1.2
= 56.8 Hz

5.4 Function Generator IC 8038:

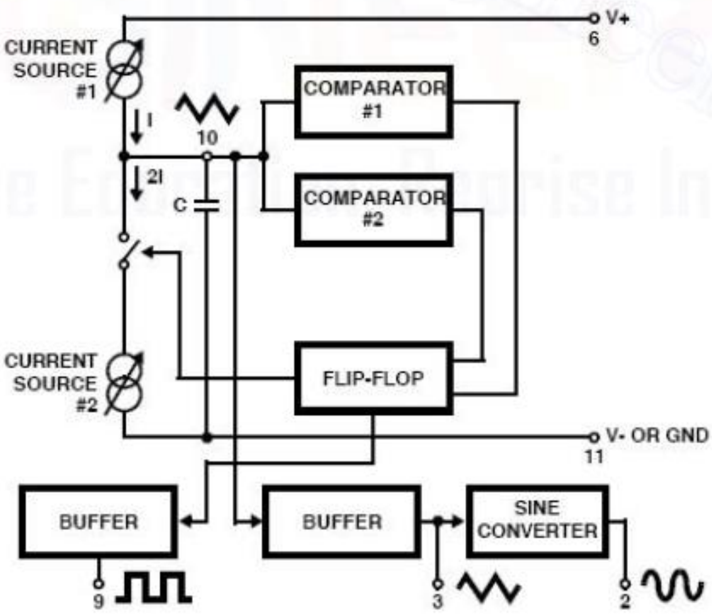


Fig.5.14 Functional block diagram of Function generator

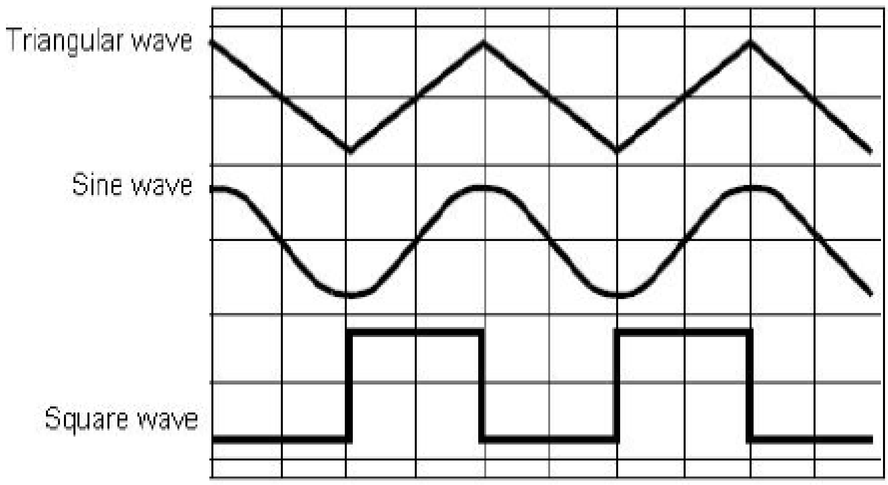


Fig. 5.15 Output Waveforms from Function Generator IC 8038

It consists of two current sources, two comparators, two buffers, one FF and a sine wave converter.

Pin description:

• Pin 1 & Pin 12: Sine wave adjusts:
The distortion in the sine wave output can be reduced by adjusting the 100KΩ pots connected between pin12 & pin11 and between pin 1 & 6.

• Pin 2 Sine Wave Output:
Sine wave output is available at this pin. The amplitude of this sine wave is 0.22 Vcc. Where ± 5V ≤ Vcc ≤ ± 15 V.

• Pin 3 Triangular Wave output:
Triangular wave is available at this pin. The amplitude of the triangular wave is 0.33Vcc. Where ± 5V ≤ Vcc ≤ ± 15 V.

• Pin 4 & Pin 5 Duty cycle / Frequency adjust:
The symmetry of all the output wave forms & 50% duty cycle for the square wave output is adjusted by the external resistors connected from Vcc to pin 4. These external resistors & capacitors at pin 10 will decide the frequency of the output wave forms.

• Pin 6 + Vcc:
Positive supply voltage the value of which is between 10 & 30V is applied to this pin.

• Pin 7 : FM Bias:
This pin along with pin no8 is used to TEST the IC 8038.

• Pin9 : Square Wave Output:
A square wave output is available at this pin. It is an open collector output so that this pin can be connected through the load to different power supply voltages. This arrangement is very useful in making the square wave output.

• Pin 10 : Timing Capacitors:
The external capacitor C connected to this pin will decide the output frequency along with the resistors connected to pin 4 & 5.

• Pin 11 : -VEE or Ground:
If a single polarity supply is to be used then this pin is connected to supply ground & if (±) supply voltages are to be used then (-) supply is connected to this pin.

• Pin 13 & Pin 14: NC (No Connection)

Important features of IC 8038:

1. All the outputs are simultaneously available.
2. Frequency range : 0.001Hz to 500kHz
3. Low distortion in the output wave forms.
4. Low frequency drifts due to change in temperature.
5. Easy to use.

Parameters:

(i) Frequency of the output wave form:
The output frequency dependent on the values of resistors R1 & R2 along with the external capacitor C connected at pin 10.
If RA= RB = R & if RC is adjusted for 50% duty cycle then f_0= 0.3/RC; RA = R1, RB = R3, RC= R2.

(ii) Duty cycle / Frequency Adjust : (Pin 4 & 5):
Duty cycle as well as the frequency of the output wave form can be adjusted by external resistors at pin 4 & 5. The values of resistors RA & RB connected between Vcc pin 4 & 5

respectively along with the capacitor connected at pin 10 decide the frequency of the wave form. The values of RA & RB should be in the range of 1kΩ to 1MΩ.

(iii)FM Bias:

- The FM Bias input (pin7) corresponds to the junction of resistors R1 & R2.
- The voltage Vin is the voltage between Vcc & pin8 and it decides the output frequency.
- The output frequency is proportional to Vin as given by the following expression.

For RA = RB (50% duty cycle).

- f_0= 5 V_{in}/CRAV_{cc} ; where C is the timing capacitor.
- With pin 7 & 8 connected to each other the output frequency is given by f_0= 0.3/RC where R = RA = RB for 50% duty cycle.
- This is because M Sweep input (pin 8):
- Vin=R1Vcc/R1+R2
- This input should be connected to pin 7, if we want a constant output frequency.
- But if the output frequency is supposed to vary, then a variable dc voltage should be applied to this pin.
- The voltage between Vcc & pin 8 is called Vin and it decides the output frequency as,

f_0=1.5 V_{in}/C$R_A$$V_{CC}$

A potentiometer can be connected to this pin to obtain the required variable voltage required to change the output frequency.

5.5 The 555 Timer IC

The 555 is a monolithic timing circuit that can produce accurate & highly stable time delays or oscillation. The timer basically operates in one of two modes: either

(i) Monostable (one - shot) multivibrator or

(ii) Astable (free running) multivibrator

The important features of the 555 timer are these:

(i) It operates on +5v to +18 v supply voltages

(ii) It has an adjustable duty cycle

(iii) Timing is from microseconds to hours

(iv) It has a current o/p

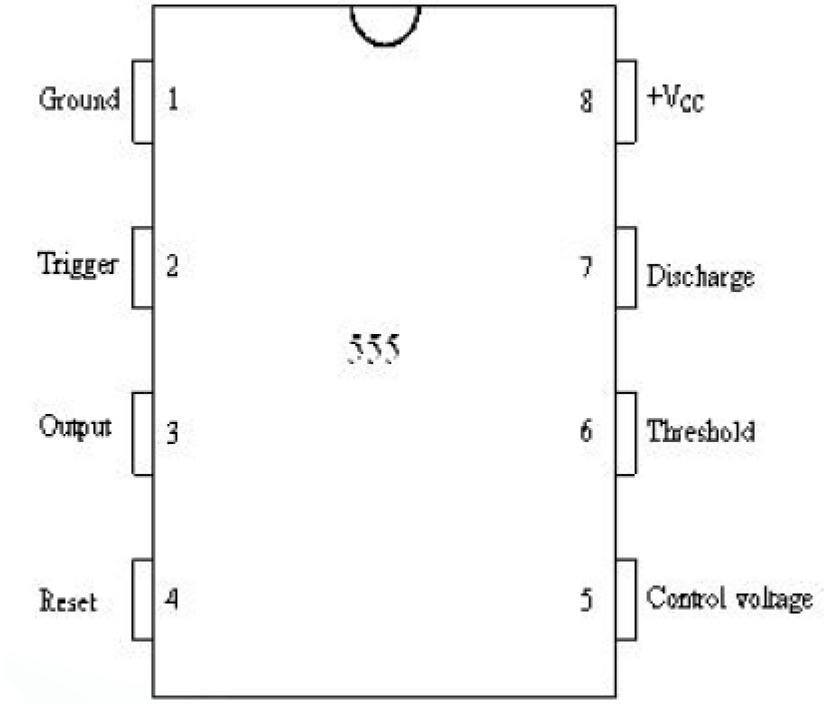


Fig. 5.16 Pin configuration of 555 timer

Pin description:

Pin 1: Ground**:**
All voltages are measured with respect to this terminal.
Pin 2: Trigger:
The o/p of the timer depends on the amplitude of the external trigger pulse applied to this pin.
Pin 3: Output:
There are 2 ways a load can be connected to the o/p terminal either between pin3 & ground or between pin 3 & supply voltage (Between Pin 3 & Ground ON load) (Between Pin 3 & + Vcc OFF load)
(i) When the input is low:
The load current flows through the load connected between Pin 3 & +Vcc in to the output terminal & is called the sink current.
(ii) When the output is high:
The current through the load connected between Pin 3 & +Vcc (i.e. ON load) is zero. However the output terminal supplies current to the normally OFF load. This current is called the source current.
Pin 4: Reset:
The 555 timer can be reset (disabled) by applying a negative pulse to this pin. When the reset function is not in use, the reset terminal should be connected to +Vcc to avoid any false triggering.
Pin 5: Control voltage:
An external voltage applied to this terminal changes the threshold as well as trigger voltage. In other words by connecting a potentiometer between this pin & GND, the pulse width of

the output waveform can be varied. When not used, the control pin should be bypassed to ground with 0.01 capacitor to prevent any noise problems.
Pin 6: Threshold:
This is the non inverting input terminal of upper comparator which monitors the voltage across the external capacitor.
Pin 7: Discharge:
This pin is connected internally to the collector of transistor Q1.
When the output is high Q1 is OFF.
When the output is low Q is (saturated) ON.
Pin 8: +Vcc:
The supply voltage of +5V to +18V is applied to this pin with respect to ground.

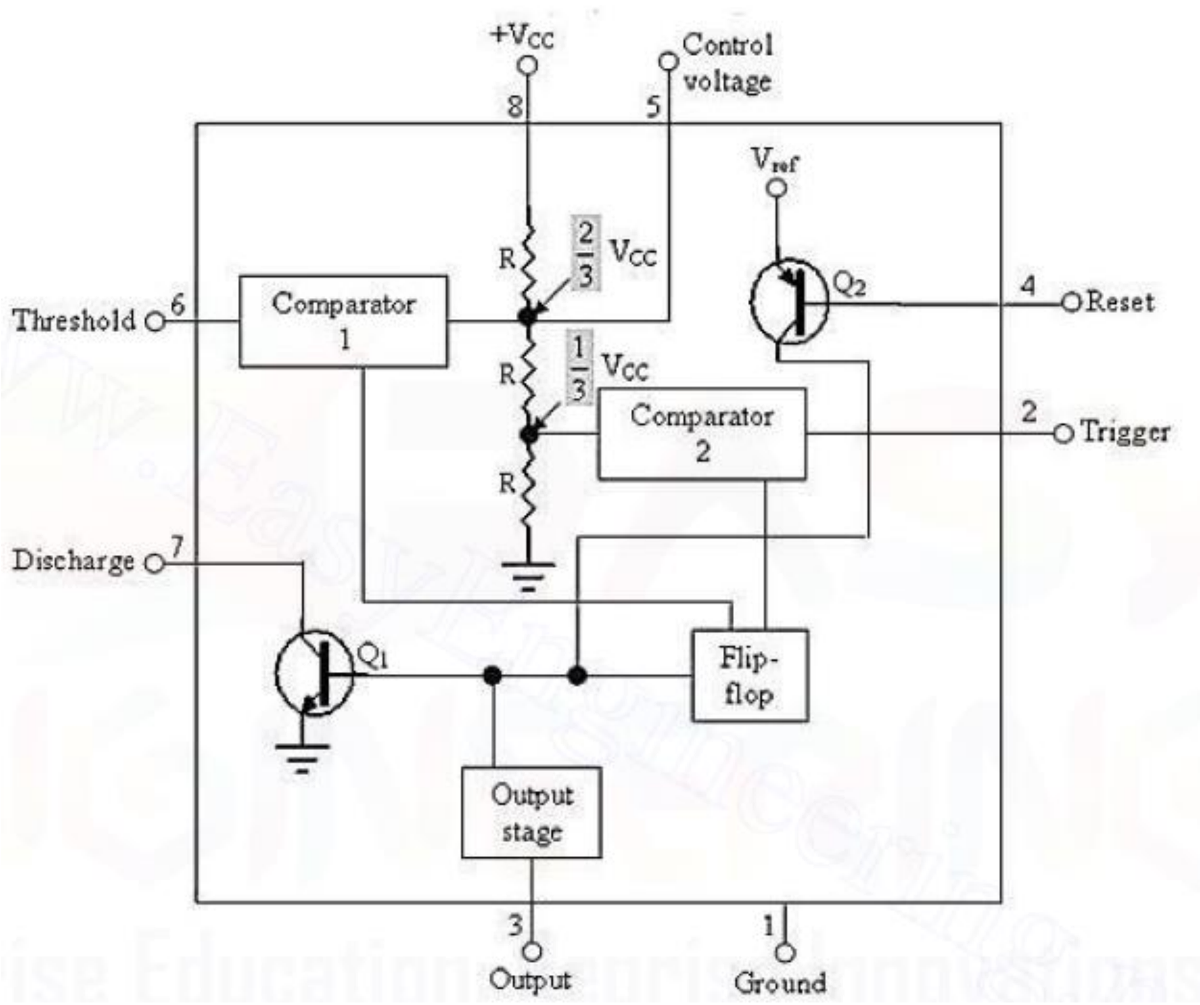


Fig.5.17 Block **Diagram of 555 Timer IC**

From the above figure, three 5k internal resistors act as voltage divider providing bias voltage of 2/3 Vcc to the upper comparator & 1/3 Vcc to the lower comparator. It is possible to vary time electronically by applying a modulation voltage to the control voltage input terminal (5).
(i) In the Stable state:
The output of the control FF is high. This means that the output is low because of power amplifier which is basically an inverter. Q = 1; Output = 0

(ii) At the Negative going trigger pulse:
The trigger passes through (Vcc/3) the output of the lower comparator goes high & sets the FF. Q = 1; Q = 0
(iii) At the Positive going trigger pulse: It passes through 2/3Vcc, the output of the upper comparator goes high and resets the FF. Q = 0; Q = 1
The reset input (pin 4) provides a mechanism to reset the FF in a manner which overrides the effect of any instruction coming to FF from lower comparator.

• **Monostable Operation:**

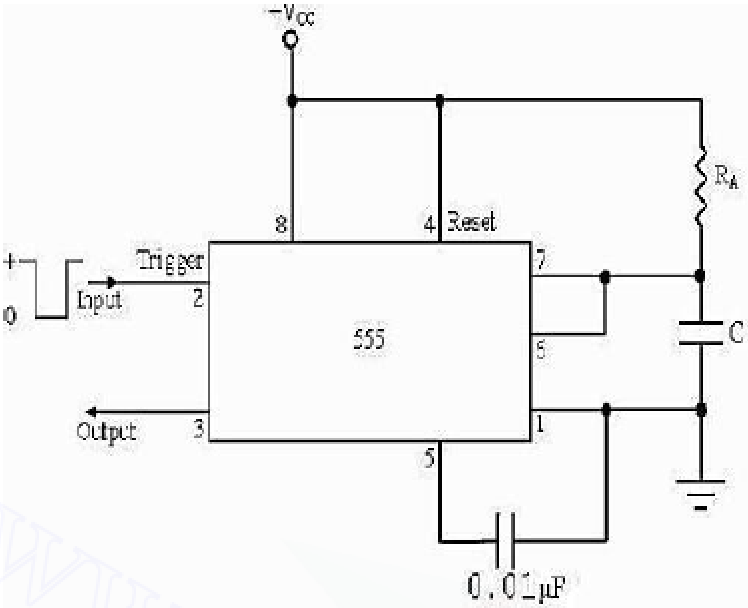


Fig. 5.18 555 connected as a Monostable Multivibrator

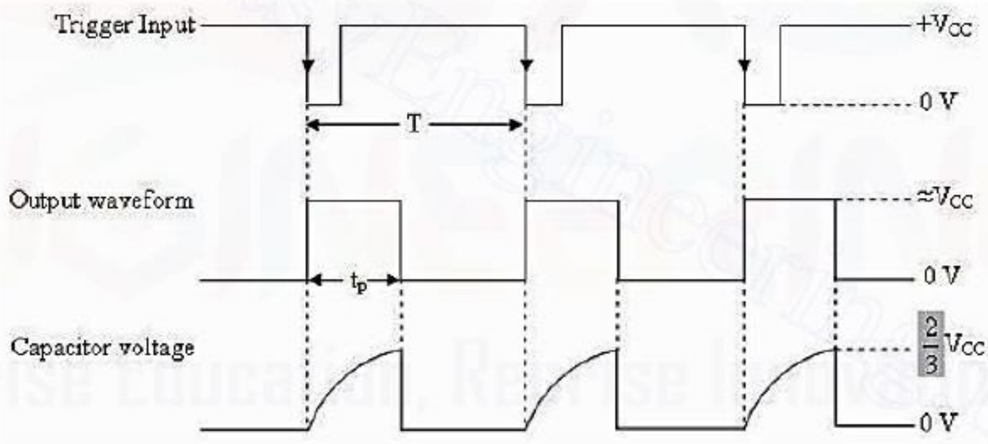


Fig. 5.19 Waveforms of monostable multivibrators

Initially when the output is low, i.e. the circuit is in a stable state, transistor Q1 is ON & capacitor C is shorted to ground. The output remains low. During negative going trigger pulse, transistor Q1 is OFF, which releases the short circuit across the external capacitor C & drives the output high. Now the capacitor C starts charging toward Vcc through RA. When

the voltage across the capacitor equals 2/3 Vcc, upper comparator switches from low to high. i.e. Q = 0, the transistor Q1 = OFF ; the output is high.
Since C is unclamped, voltage across it rises exponentially through R towards Vcc with a time constant RC (fig b) as shown in below. After the time period, the upper comparator resets the FF, i.e. Q = 1, Q1 = ON; the output is low.[i.e discharging the capacitor C to ground potential (fig c)]. The voltage across the capacitor as in fig (b) is given by

Vc = Vcc (1-e-t/RC)……. (1)

Therefore At t = T, Vc = 2/3 Vcc

2/3 Vcc = Vcc(1-e-T/RC)

or

T = RC ln (1/3)

Or

T = 1.1RC seconds ……………. (2)

If the reset is applied Q2 = OFF, Q1 = ON, timing capacitor C immediately discharged. The output now will be as in figure (d & e). If the reset is released output will still remain low until a negative going trigger pulse is again applied at pin 2.

Applications of Monostable Mode of Operation:

(a) Frequency Divider:

The 555 timer as a monostable mode. It can be used as a frequency divider by adjusting the length of the timing cycle tp with respect to the time period T of the trigger input. To use the monostable multivibrator as a divide by 2 circuit, the timing interval tp must be a larger than the time period of the trigger input. [Divide by 2, tp > T of the trigger]
By the same concept, to use the monostable multivibrator as a divide by 3 circuit, tp must be slightly larger than twice the period of the input trigger signal & so on,
[divide by 3tp > 2T of trigger]

(b) Pulse width modulation:

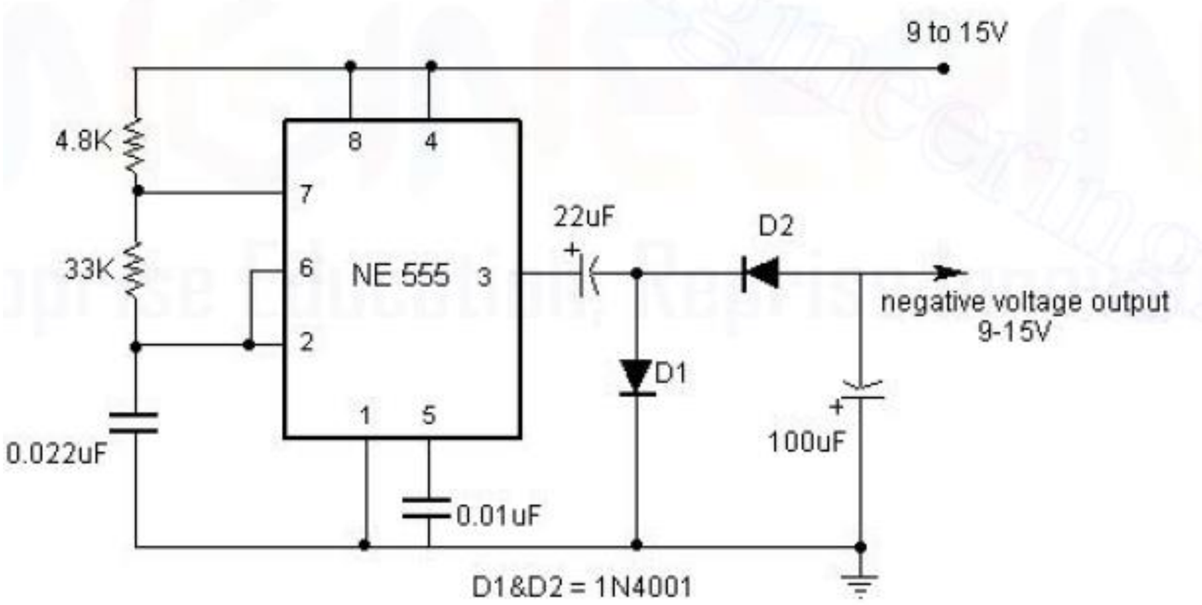


Fig.5.20 Pulse Width Modulation

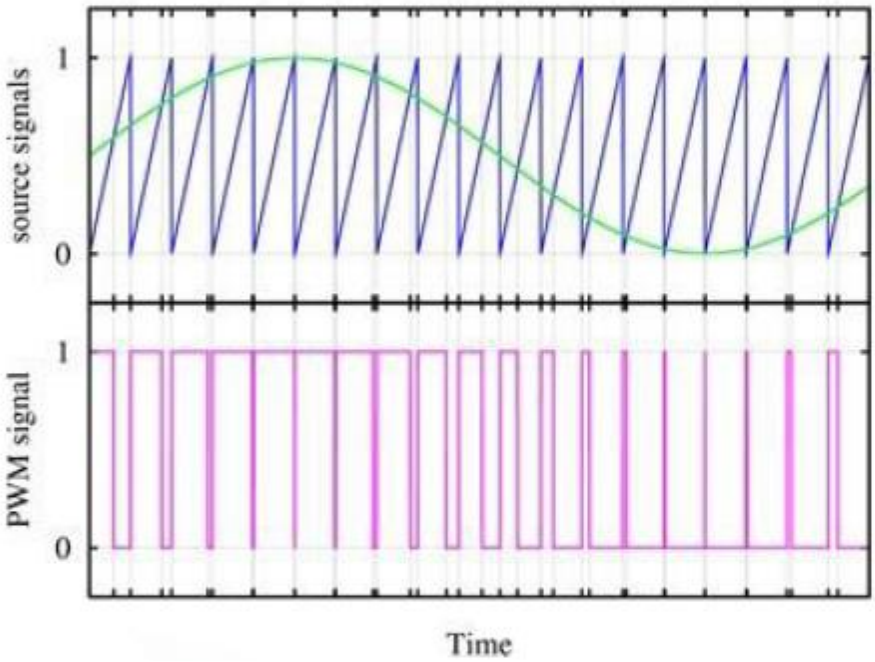


Fig. 5.21 Output Waveform

Pulse width of a carrier wave changes in accordance with the value of a incoming (modulating signal) is known as PWM. It is basically monostable multivibrator. A modulating signal is fed in to the control voltage (pin 5). Internally, the control voltage is adjusted to 2/3 Vcc externally applied modulating signal changes the control voltage level of upper comparator. As a result, the required to change the capacitor up to threshold voltage level changes, giving PWM output.

(c) Pulse Stretcher:

This application makes use of the fact that the output pulse width (timing interval) of the monostable multivibrator is of longer duration than the negative pulse width of the input trigger. As such, the output pulse width of the monostable multivibrator can be viewed as a stretched version of the narrow input pulse, hence the name "Pulse stretcher".

Often, narrow –pulse width signals are not suitable for driving an LED display, mainly because of their very narrow pulse widths. In other words, the LED may be flashing but not be visible to the eye because its on time is infinitesimally small compared to its off time. The 55 pulse stretcher can be used to remedy this problem. The LED will be ON during the timing interval tp = 1.1RAC which can be varied by changing the value of RA & C.

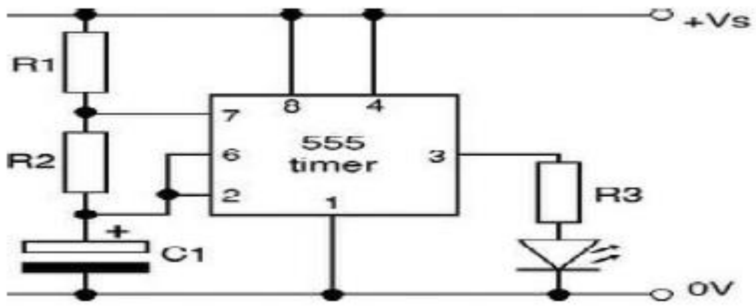


Fig.5.23 Pulse Stretcher

The 555 timer as an Astable Multivibrator:

An Astable multivibrator, often called a free running multivibrator, is a rectangular wave generating circuit. Unlike the monostable multivibrator, this circuit does not require an external trigger to change the state of the output, hence the name free running. However, the time during which the output is either high or low is determined by 2 resistors and capacitors, which are externally connected to the 555 timer.

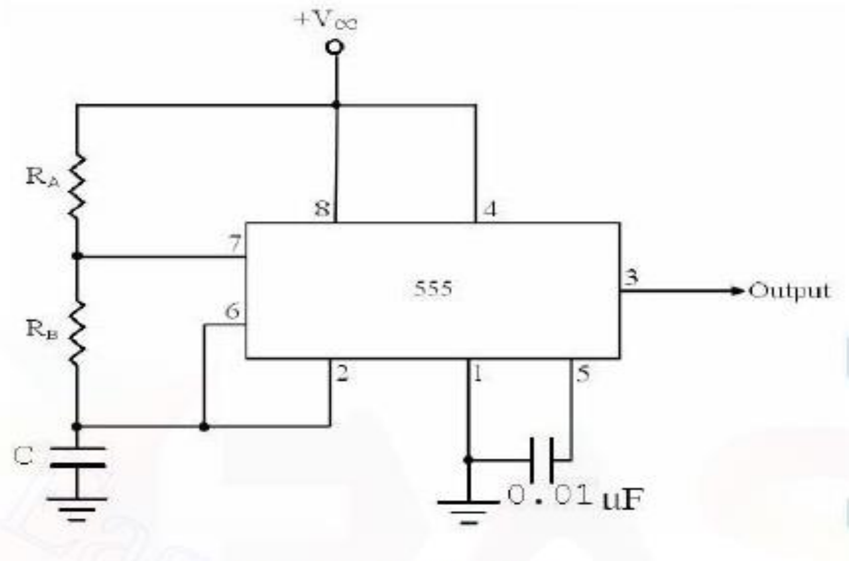


Fig.5.24 Astable Multivibrator

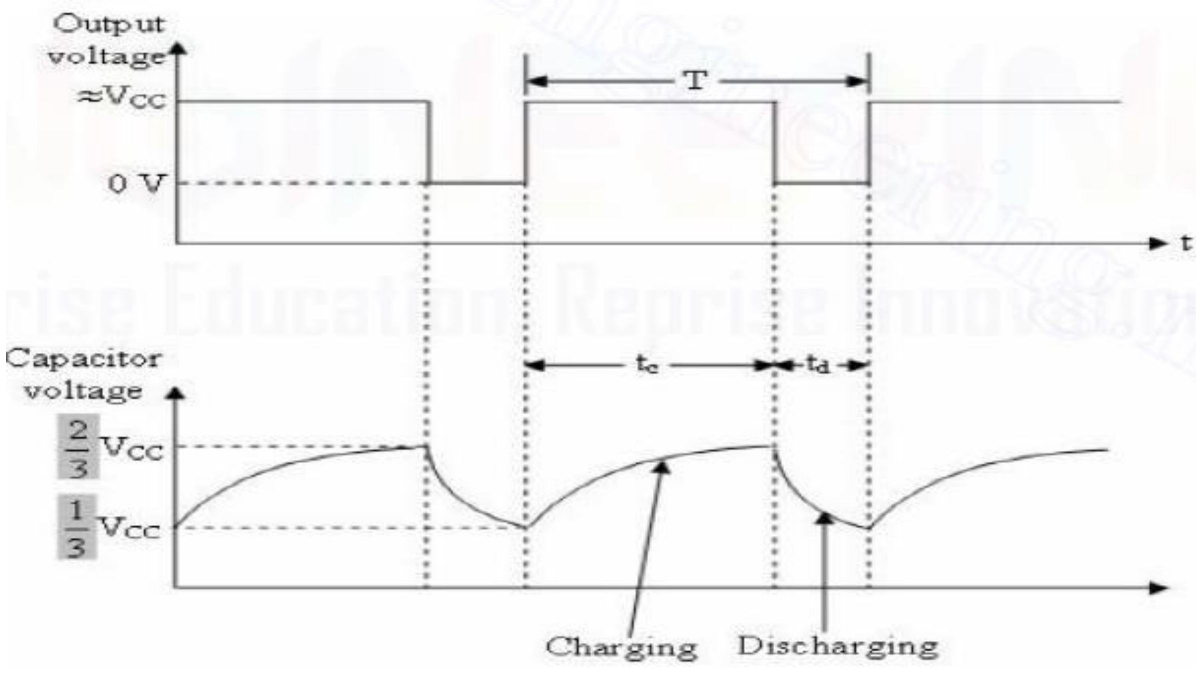


Fig. 5.25 Waveforms of Astable multivibrator

The above figures show the 555 timer connected as an astable multivibrator and its model graph

Initially, when the output is high :

Capacitor C starts charging toward Vcc through RA & RB. However, as soon as voltage across the capacitor equals 2/3 Vcc. Upper comparator triggers the FF & output switches low.

When the output becomes Low:

Capacitor C starts discharging through RB and transistor Q1, when the voltage across C equals 1/3 Vcc, lower comparator output triggers the FF & the output goes high. Then cycle repeats. The capacitor is periodically charged & discharged between 2/3 Vcc & 1/3 Vcc respectively. The time during which the capacitor charges from 1/3 Vcc to 2/3 Vcc equal to the time the output is high & is given by

tc = (RA+RB)C ln 2……………(1) Where [ln 2 = 0.69]

= 0.69 (RA+RB) C

Where RA & RB are in ohms. And C is in farads.
Similarly, the time during which the capacitors discharges from 2/3 Vcc to 1/3 Vcc is equal to the time, the output is low and is given by,

tc = RB C ln 2

td = 0.69 RB C …………………..(2)

where RB is in ohms and C is in farads.
Thus the total period of the output waveform is

T = tc + td = 0.69 (RA+2RB) C …………….(3)

This, in turn, gives the frequency of oscillation as,

f 0 = 1/T = 1.45/(RA+2RB)C ………(4)

Equation 4 indicates that the frequency f 0 is independent of the supply voltage Vcc.
Often the term duty cycle is used in conjunction with the astable multivibrator. The duty cycle is the ratio of the time tc during which the output is high to the total time period T. It is generally expressed as a percentage.

% duty cycle = (tc / T)* 100

% DC = [(RA+RB)/ /(RA+2RB)] * 100

Astable Multivibrator Applications:

(a) Square wave oscillator:

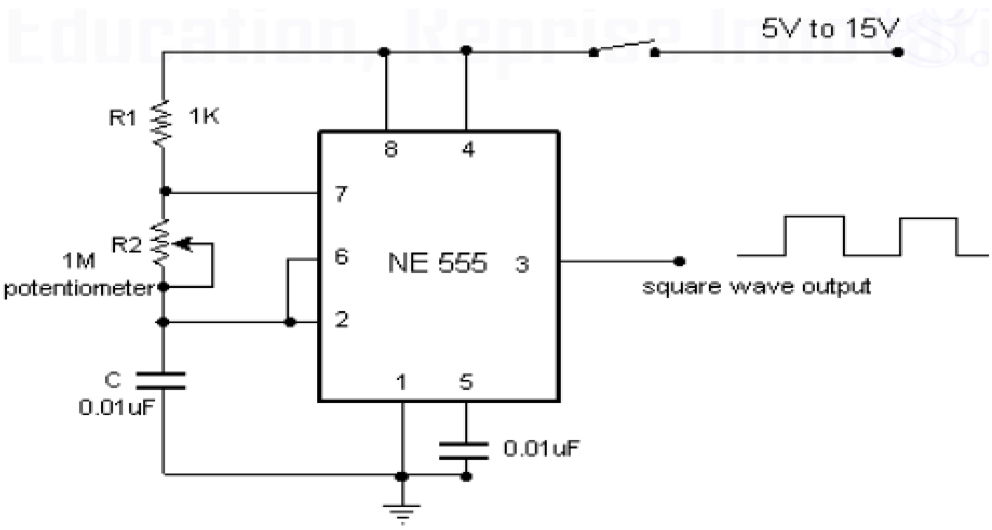
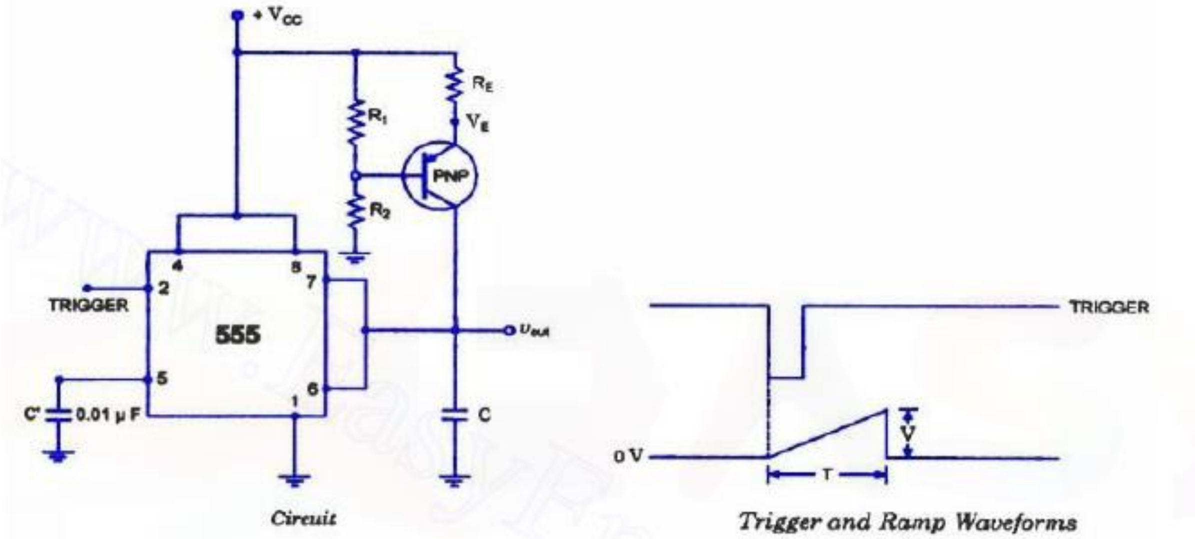


Fig.5.26 Square Wave Oscillator

Without reducing RA = 0 ohm, the astable multivibrator can be used to produce square wave output. Simply by connecting diode D across Resistor RB. The capacitor C charges through RA & diode D to approximately 2/3Vcc & discharges through RB & Q1 until the capacitor voltage equals approximately 1/3Vcc, then the cycle repeats.

To obtain a square wave output, RA must be a combination of a fixed resistor & potentiometer so that the potentiometer can be adjusted for the exact square wave.

(b) Free – running Ramp generator:



Ramp Generator Using The Timer 555

• The astable multivibrator can be used as a free – running ramp generator when resistor RA & RB is replaced by a current mirror.
• The current mirror starts charging capacitor C toward Vcc at a constant rate.
• When voltage across **C equals to 2/3 Vcc**, upper comparator turns transistor Q1 ON & C rapidly discharges through transistor Q1.
• When voltage across **C equals to 1/3 Vcc**, lower comparator switches transistor OFF & then capacitor C starts charging up again.
• Thus the charge – discharge cycle keeps repeating.
• The discharging time of the capacitor is relatively negligible compared to its charging time.
• The time period of the ramp waveform is equal to the charging time & is approximately is given by,

$$T = VccC/3IC$$

$$(1)\ IC = (Vcc - VBE)/R = \text{constant current}$$

Therefore the free – running frequency of ramp generator is

$$f0 = 3IC/ Vcc\ C$$

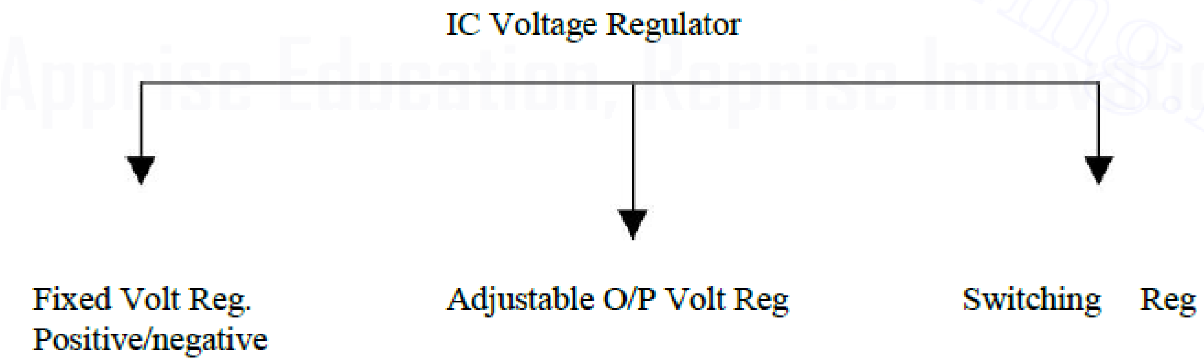
5.6 Linear Regulators

• All electronic circuits need a dc power supply for their operation. To obtain this dc voltage from 230 V ac mains supply, we need to use rectifier.
• Therefore the filters are used to obtain a “steady” dc voltage from the pulsating one.
• The filtered dc voltage is then applied to a regulator which will try to keep the dc output voltage constant in the event of voltage fluctuations or load variation.
The combination of rectifier & filter can produce a dc voltage. But the problem with this type of dc power supply is that its output voltage will not remain constant in the event of fluctuations in an AC input or changes in the load current(IL).

• The output of unregulated power supply is connected at the input of voltage regulator circuit.
• The voltage regulator is a specially designed circuit to keep the output voltage constant. It does not remain exactly constant. It changes slightly due to changes in certain parameters.
Factors affecting the output voltage:
i) IL (Load Current)
ii) VIN (Input Voltage)
iii) T (Temperature)

IC Voltage Regulators:

They are basically series regulators.
✓ Important features of IC Regulators:
1. Programmable output
2. Facility to boost the voltage/current
3. Internally provided short circuit current limiting
4. Thermal shutdown
5. Floating operation to facilitate higher voltage output



• Fixed & Adjustable output Voltage Regulators are known as Linear Regulator.
• A series pass transistor is used and it operates always in its active region.

Switching Regulator:

1. Series Pass Transistor acts as a switch.
2. The amount of power dissipation in it decreases considerably.
3. Power saving result is higher efficiency compared to that of linear

Adjustable Voltage Regulator:

Advantages of Adjustable Voltage Regulator over fixed voltage regulator are,
1. Adjustable output voltage from 1.2v to 57 v
2. Output current 0.10 to 1.5 A
3. Better load & line regulation
4. Improved overload protection
5. Improved reliability under the 100% thermal overloading

Adjustable Positive Voltage Regulator (LM317):

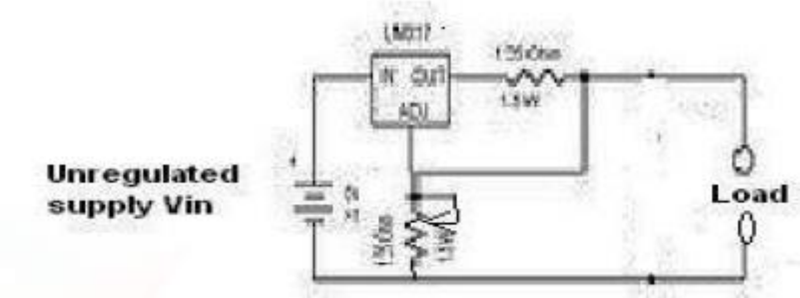


Fig. 5.27 Circuit diagram of LM317 regulator

- LM317 series adjustable 3 terminal positive voltage regulator, the three terminals are Vin, Vout & adjustment (ADJ).
- LM317 requires only 2 external resistors to set the output voltage.
- LM317 produces a voltage of 1.25v between its output & adjustment terminals. This voltage is called as Vref.
- Vref (Reference Voltage) is a constant, hence current I1 flows through R1 will also be constant. Because resistor R1 sets current I1. It is called "current set" or "program resistor".
- Resistor R2 is called as "Output set" resistors, hence current through this resistor is the sum of I1 & Iadj
- LM317 is designed in such as that Iadj is very small & constant with changes in line voltage & load current.
- The output voltage Vo is, $V_o=R_1I_1+(I_1+I_{adj})R_2$ ------------- (1)

Where $I_1= V_{ref}/R_1$

$$V_o = (V_{ref}/R_1) R_1 + V_{ref}/R_1 + I_{adj} R_2$$
$$= V_{ref} + (V_{ref}/R_1) R_2 + I_{adj} R_2$$
$$V_o = V_{ref} [1 + R_2/R_1] + I_{adj} R_2 \text{ ------------- (2)}$$

R_1 = Current (I_1) set resistor

R_2 = output (V_o) set resistor.

Vref = 1.25v which is a constant voltage between output and ADJ terminals.

- Current Iadj is very small. Therefore the second term in (2) can be neglected.
- Thus the final expression for the output voltage is given by

$$V_o= 1.25v[1 + R2/R1] \text{ -------------- (3)}$$

Eqn (3) indicates that we can vary the output voltage by varying the resistance R2. The value of R1 is normally kept constant at 240 ohms for all practical applications.

Practical Regulator using LM317:

- If LM317 is far away from the input power supply, then 0.1μf disc type or 1μf tantalum capacitor should be used at the input of LM317.
- The output capacitor Co is optional. Co should be in the range of 1 to 1000μf.
- The adjustment terminal is bypassed with a capacitor C2 this will improve the ripple rejection ratio as high as 80 dB is obtainable at any output level.
- When the filter capacitor is used, it is necessary to use the protective diodes.
- These diodes do not allow the capacitor C2 to discharge through the low current point of the regulator.
- These diodes are required only for high output voltages (above 25v) & for higher

values of output capacitance 25µf and above.

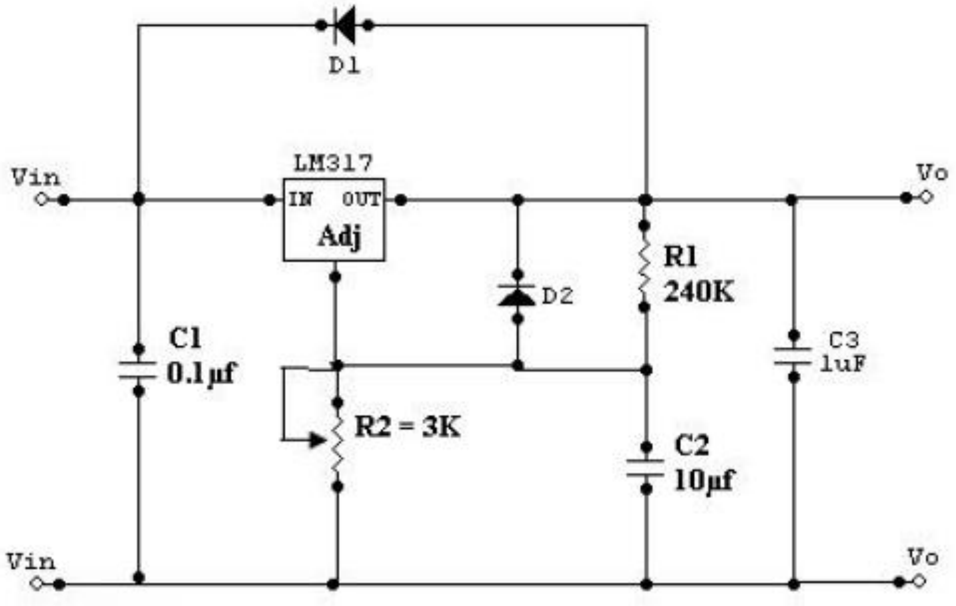


Fig. 5.28 Practical regulator

5.7 IC 723 – General Purpose Regulator

✓ Disadvantages of fixed voltage regulator:
1. Do not have the shot circuit
2. Output voltage is not adjustable
These limitations can be overcomes in IC723.
✓ Features of IC723:
1. Unregulated dc supply voltage at the input between 9.5V & 40V
2. Adjustable regulated output voltage between 2 to 3V.
3. Maximum load current of 150 mA (ILmax = 150mA).
4. With the additional transistor used, ILmax upto 10A is obtainable.
5. Positive or Negative supply operation
6. Internal Power dissipation of 800mW.
7. Built in short circuit protection.
8. Very low temperature drift.
9. High ripple rejection.

✓ The simplified functional block diagram can be divided in to 4 blocks.
1. Reference Generating block:
The temperature compensated Zener diode, constant current source & voltage reference amplifier together from the reference generating block. The Zener diode is used to generate a fixed reference voltage internally. Constant current source will make the Zener diode to operate at affixed point & it is applied to the Non – inverting terminal of error amplifier. The Unregulated input voltage ±Vcc is applied to the voltage reference amplifier as well as error amplifier.
2. Error Amplifier:

Error amplifier is a high gain differential amplifier with 2 input (inverting & Noninverting).The Non-inverting terminal is connected to the internally generated reference voltage. The Inverting terminal is connected to the full regulated output voltage.

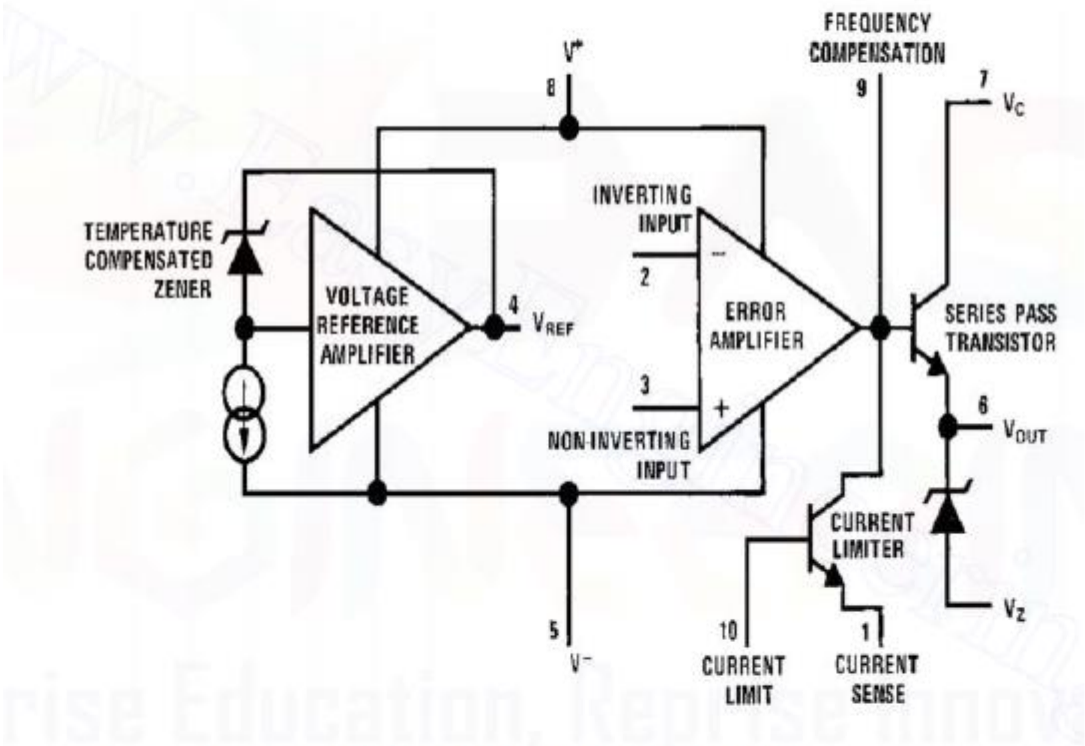


Fig. 5.29 Functional block diagram of IC723

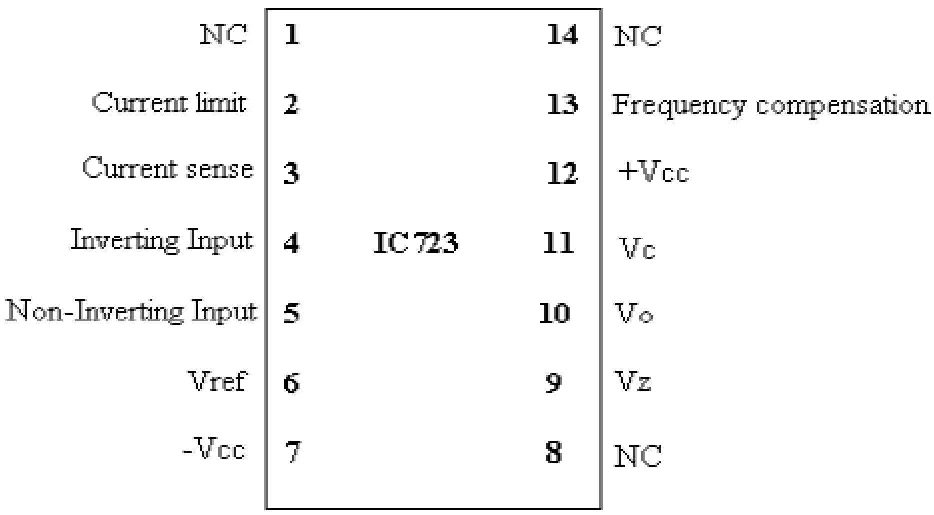


Fig.5.30 Pin diagram of IC723

3. Series Pass Transistor:

Q1 is the internal series pass transistor which is driven by the error amplifier. This transistor actually acts as a variable resistor & regulates the output voltage. The collector of transistor Q1 is connected to the Un-regulated power supply. The maximum collector voltage of Q1 is limited to 36Volts. The maximum current which can be supplied by Q1 is 150mA.

4. Circuitry to limit the current:

The internal transistor Q2 is used for current sensing & limiting. Q2 is normally OFF transistor. It turns ON when the IL exceeds a predetermined limit. Low voltage, Low current is capable of supplying load voltage which is equal to or between 2 to 7Volts.

Vload = 2 to 7V and Iload= 50Ma

5.7.1 IC723 as a LOW voltage LOW current:

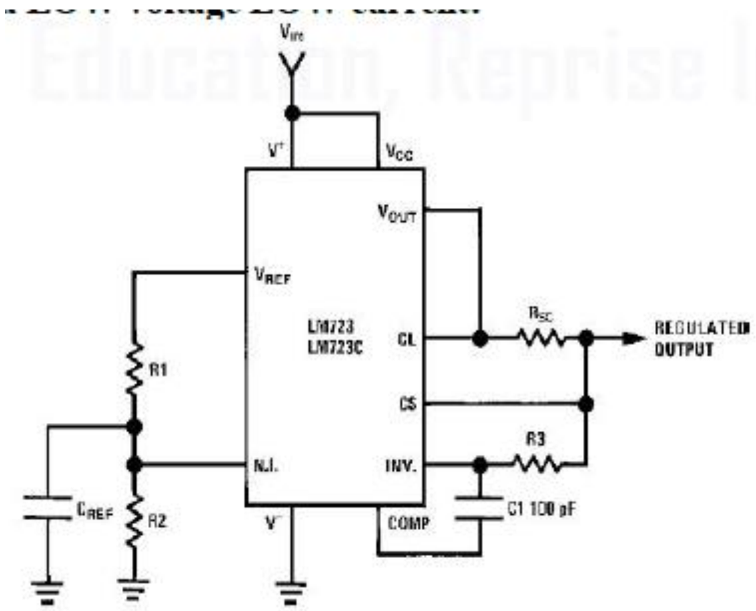


Fig.5.31 Typical circuit connection diagram

- R_1 & R_2 from a potential divider between Vref & Gnd.
- The Voltage across R2 is connected to the Non – inverting terminal of the regulator IC

$$V_{non\text{-}inv} = R_2/(R_1+R_2)\ V_{ref}$$

- Gain of the internal error amplifier is large

$V_{non\text{-}inv} = V_{in}$

- Therefore the Vo is connected to the Inverting terminal through R3 & RSC must also be equal to Vnon-inv

$$V_o = V_{non\text{-}inv} = R_2/(R_1+R_2)\ V_{ref}$$

R1 & R2 can be in the range of 1 KΩ to 10KΩ & value of R3 is given by

$$R_3 = R_1 \| R_2 = R_1R_2/(R_1+R_2)$$

Rsc (current sensing resistor) is connected between Cs & CL. The voltage drop across R_{sc} is proportional to the IL.

- This resistor supplies the output voltage in the range of 2 to 7 volts, but the load current can be higher than 150mA.
- The current sourcing capacity is increased by including a transistor Q in the circuit.
- The output voltage , $V_o = R_2/(R_1+R_2)\ V_{ref}$

5.7.2 IC723 as a HIGH voltage LOW Current:

• This circuit is capable of supplying a regulated output voltage between the ranges of 7 to 37 volts with a maximum load current of 150 mA.
• The Non – inverting terminal is now connected to Vref through resistance R3.
• The value of R1 & R2 is adjusted in order to get a voltage of Vref at the inverting terminal at the desired output.

$$V_{in} = V_{ref} = R_2/(R_1+R_2)\ V_0$$
$$V_o = [1+R_1/R_2]\ V_{in}$$

• Rsc is connected between CL & Cs terminals as before & it provides the short Circuit current limiting $Rsc = 0.6/I_{limit}$
• The value of resistors R3 is given by ,

$$R3 = R_1 \| R_2 = R_1R_2/(R_1+R_2)$$

5.7.3 IC723 as a HIGH voltage HIGH Current:

• An external transistor Q is added in the circuit for high voltage low current regulator to improve its current sourcing capacity.

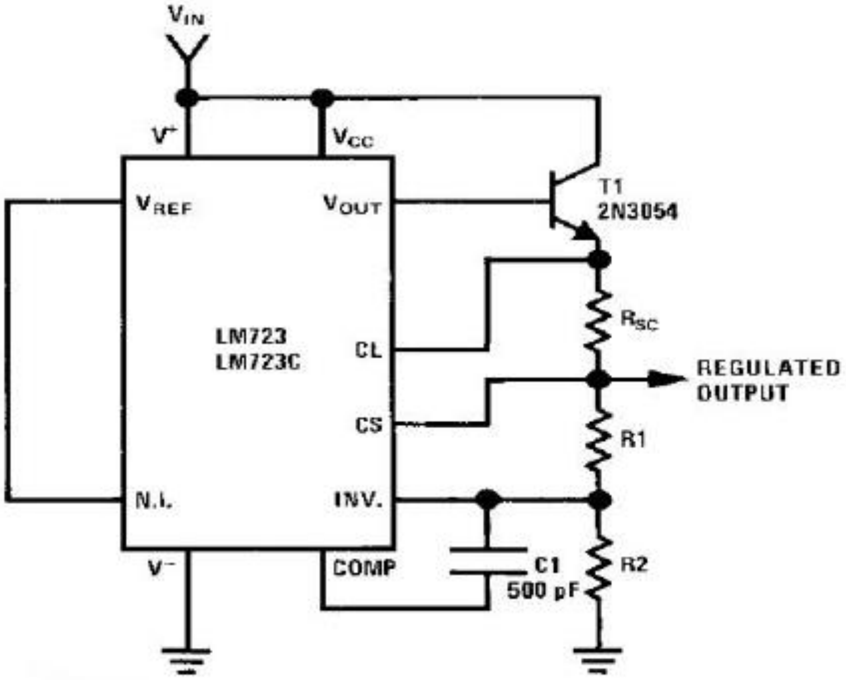


Fig.5.32 Typical circuit connection diagram

• For this circuit the output voltage varies between 7 & 37V.
• Transistor Q increase the current sourcing capacity thus IL (MAX) is greater than 150mA.
• The output voltage Vo is given by ,

$$V0 = V_o = [1+R_1/R_2]\ V_{in}$$
$$Rsc = 0.6/I_{limit}$$

5.8 Switching Regulators

Introduction

The switching regulator offers the advantages

- higher power conversion efficiency
- Increased design flexibility (multiple output voltages of different polarities can be generated from a single input voltage).
- a lot less heat and
- Smaller size.

The primary filter capacitor is placed on the input to the regulator to help filter out the 60 cycle ripple. If the output voltage is 12 volts and the input voltage is 24 volts then we must drop 12 volts across the regulator. At output currents of 10 amps this translates into 120 watts (12 volts times 10 amps) of heat energy that the regulator must dissipate into heat.

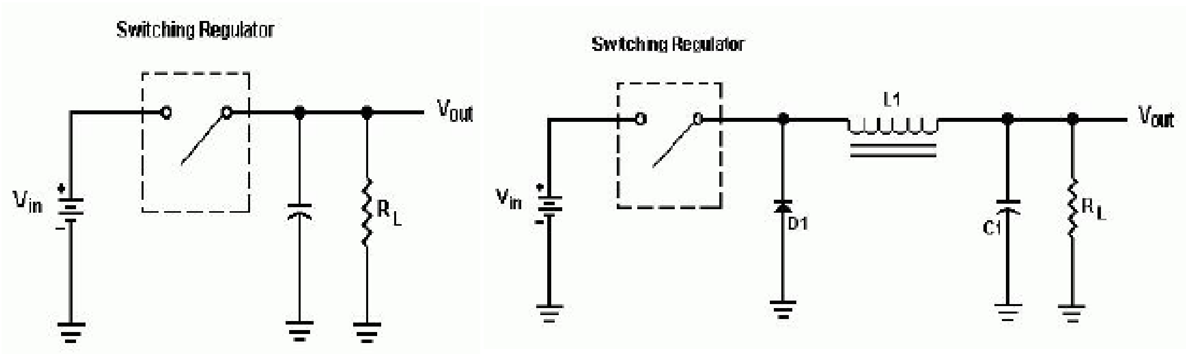


Fig.5.33 switching regulator principle

The switching regulator is much more efficient than the linear regulator achieving efficiencies as high as 80% to 95% in some circuits. The obvious result is smaller heat sinks, less heat and smaller overall size of the power supply. The switching regulator is really nothing more than just a simple switch. This switch goes on and off at a fixed rate usually between 50 Khz to 100Khz as set by the circuit.

Operation:

Diode D1 has to be a Schottky or other very fast switching diode. Inductor L1must be a type of core that does not saturate under high currents. Capacitor C1 is normally a low ESR (Equivalent Series Resistance) type.

To understand the action of D1 and L1, let’s look at what happens when S1 is closed as indicated below:

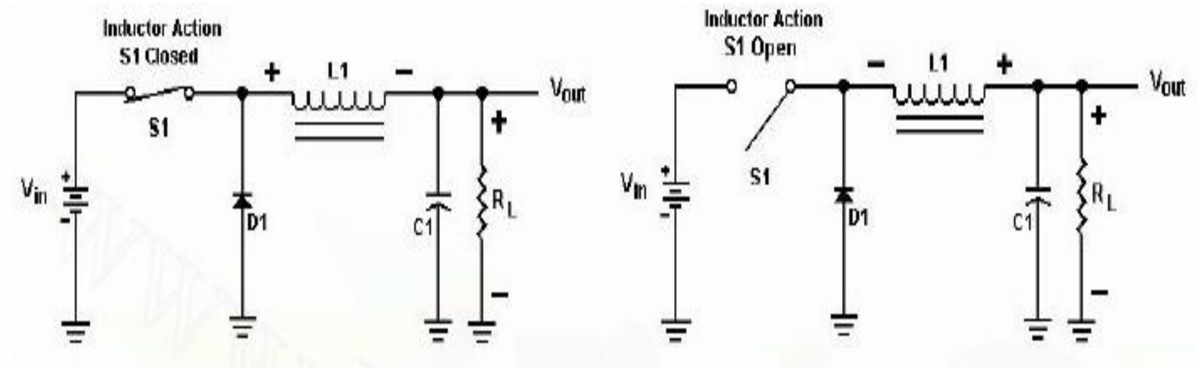


Fig.5.34 switching operation of regulator

L1, which tends to oppose the rising current, begins to generate an electromagnetic field in its core. Diode D1 is reversed biased and is essentially an open circuit at this point. When S1 opens, the electromagnetic field that was built up in L1 is now discharging and generating a current in the reverse polarity. As a result, D1 is now conducting and will continue until the field in L1 is diminished. This action is similar to the charging and discharging of capacitor C1. The use of this inductor/diode combination gives us even more efficiency and augments the filtering of C1.
Because the switching system operates in the 50 to 100 kHz region and has an almost square waveform, it is rich in harmonics way up into the HF and even the VHF/UHF region
Four most commonly used switching converter types:
Buck: used the reduce a DC voltage to a lower DC voltage.
Boost: provides an output voltage that is higher than the input.
Buck-Boost (invert): an output voltage is generated opposite in polarity to the input.
Fly back: an output voltage that is less than or greater than the input can be generated, as well as multiple outputs.
Converters:
Push-Pull: A two-transistor converter that is especially efficient at low input voltages.
Half-Bridge: A two-transistor converter used in many off-line applications.
Full-Bridge: A four-transistor converter (usually used in off-line designs) that can generate the highest output power of all the types listed.

Switching Regulator:

An example of general purpose regulator is Motorola's MC1723. It can be used in many different ways, for example, as a fixed positive or negative output voltage regulator, variable regulator or switching regulator because of its flexibility.
To minimize the power dissipation during switching, the external transistor used must be a switching power transistor. To improve the efficiency of a regulator, the series pass transistor is used as a switch rather than as a variable resistor as in the linear mode.
• A regulator constructed to operate in this manner is called a series switching regulator. In such regulators the series pass transistor is switched between cut off & saturation at a high frequency which produces a pulse width modulated (PWM) square wave output.
• This output is filtered through a low pass LC filter to produce an average dc output voltage.
• Thus the output voltage is proportional to the pulse width and frequency.
• The efficiency of a series switching regulator is independent of the input & output differential & can approach 95%

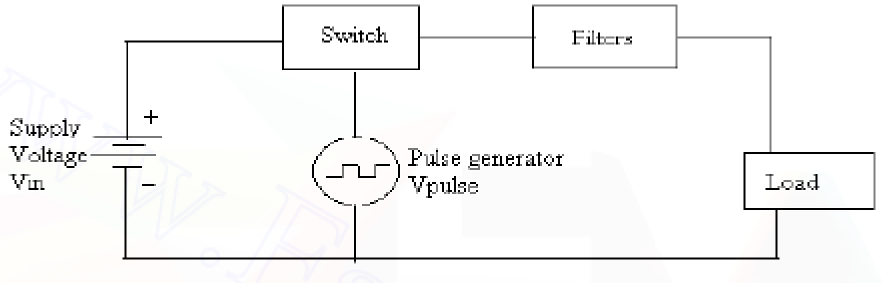


Fig.5.35 Basic Switching regulator

A basic switching regulator consists of 4 major components,
1. Voltage source Vin
2. Switch S1
3. Pulse generator Vpulse
4. Filter F1

1. Voltage Source Vin:

It may be any dc supply – a battery or an unregulated or a regulated voltage. The voltage source must satisfy the following requirements.

- It must supply the required output power & the losses associated with the switching regulator.
- It must be large enough to supply sufficient dynamic range for line & load regulations.
- It must be sufficiently high to meet the minimum requirement of the regulator system to be designed.
- It may be required to store energy for a specified amount of time during power failures.

2. Switch S1:

It is typically a transistor or thyristor connected as a power switch & is operated in the saturated mode. The pulse generator output alternately turns the switch ON & OFF

3. Pulse generator Vpulse:

It provides an asymmetrical square wave varying in either frequency or pulse width called frequency modulation or pulse width modulation respectively. The most effective frequency range for the pulse generator for optimum efficiency 20 KHz. This frequency is inaudible to the human ear & also well within the switching speeds of most inexpensive transistors & diodes.

- The duty cycle of the pulse wave form determines the relationship between the input & output voltages. The duty cycle is the ratio of the on time ton, to the period T of the pulse waveform.

$$\text{Duty cycle} = t_{on}/(t_{on}+t_{off}) = t_{on}/T = t_{on}.f$$

Where ton = On-time of the pulse waveform toff=off-time of the pulse wave form

$$T = \text{time period} = t_{on} + t_{off}$$
$$= 1/\text{frequency or } T = 1/f$$

- Typical operating frequencies of switching regulator range from 10 to 50 kHz.
- Lower operating frequency improve efficiency & reduce electrical noise, but require large filter components (inductors & capacitors).

4. Filter F1:

It converts the pulse waveform from the output of the switch into a dc voltage.
Since this switching mechanism allows a conversion similar to transformers, the switching regulator is often referred to as a dc transformer.
The output voltage Vo of the switching regulator is a function of duty cycle & the input voltage Vin.
Vo is expressed as follows,

$$V_o = t_{on} V_{in}/T$$

- This equation indicates that, if time period T is constant, Vo is directly proportional to the ON-time, ton for a given value of Vin. This method of changing the output

voltage by varying ton is referred to as a pulse width modulation.
• Similarly, if ton is held constant, the output voltage Vo is inversely proportional to the period T or directly proportional to the frequency of the pulse waveform. This method of varying the output voltage is referred to as frequency modulation (FM).
• Switching regulator can operate in any of 3 modes
i) Step – Down
ii) Step – Up
iii) Polarity inverting

5.8 Monolithic Switching Regulator [µa78s40]:

The µA78S40 consists of a temperature compensated voltage reference, duty cycle controllable oscillator with an active current limit circuit, a high gain comparator, a high-current, high voltage output switch, a power switching diode & an uncommitted op-amp. Important features of the µA78S40 switching regulators are:
• Step up, down & Inverting operation
• Operation from 2.5 to 40V input
• 80dB line & load regulations
• Output adjustable from 1.3 to 40V
• Peak current to 1.5A without external resistors
• Variable frequency, variable duty cycle device
The internal switching frequency is set by the timing capacitor CT, connected between pin12 & ground pin 11. The initial duty cycle is 6:1. The switching frequency & duty cycle can be modified by the current limit circuitry, IPK sense, pin14, 7 the comparator, pin9 & 10.

Comparator:

The comparator modifies the OFF time of the output switch transistor Q1 & Q2. In the step – up & step down modes, the non-inverting input(pin9) of the comparator is connected to the voltage reference of 1.3V (pin8) & the inverting input (pin10) is connected to the output terminal via the voltage divider network.

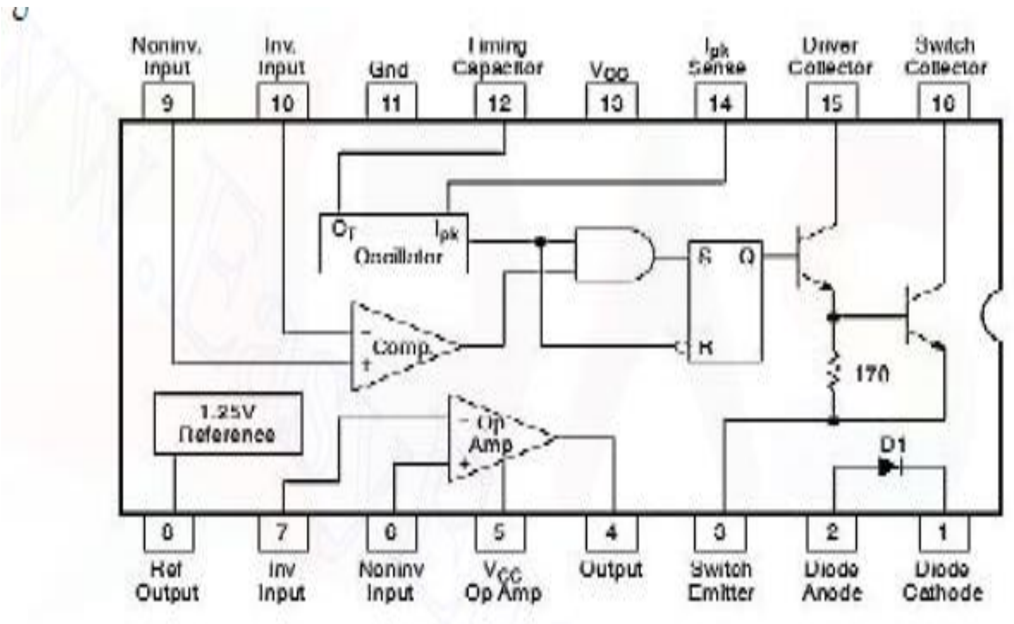


Fig.5.36 Functional block diagram of µA78S40

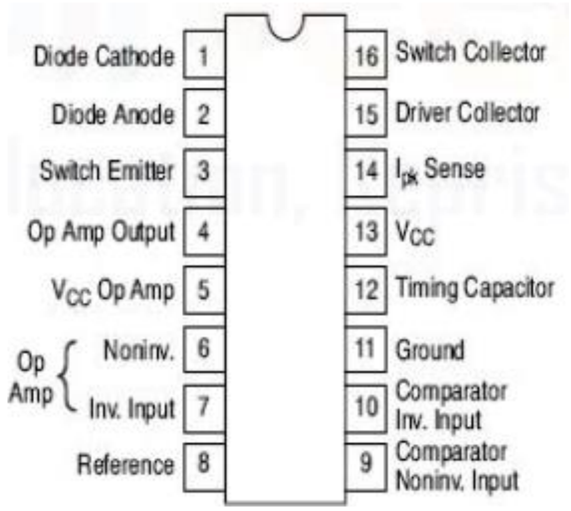


Fig.5.37 Pin diagram of Monolithic Switching Regulator [µa78s40]:

- In the Inverting mode the non – inverting input is connected to both the voltage reference & the output terminal through 2 resistors & the inverting terminal is connected to ground.
- When the output voltage is correct, the comparator output is in high state & has no effect on the circuit operation
- However, if the output is too high & the voltage at the inverting terminal is higher than that at the non-inverting terminal, then the comparator output goes low.
- In the LOW state the comparator inhibits the turn on of the output switching transistors. This means that, as long as the comparator output is low, the system is in off time.
- As the output current rises or the output voltage falls, the off time of the system decreases.

• Consequently, as the output current nears its maximum IoMAX, the off time approaches its minimum value.
In all 3 modes (Step down, step up, Inverting), the current limit circuit is completed by connecting a sense resistor Rsc, between IPK sense & Vcc.
• The current limit circuit is activated when a 330mV potential appears across Rsc.
• Rsc is selected such that 330mV appears across it when the desired peak current IPK, flows through it.
• When the peak current is reached, the current limit circuit is turned on.
The forward voltage drop, VD, across the internal power diode is used to determine the value of inductor L off time & efficiency of the switching regulator. Another important quantity used in the design of a switching regulator is the saturation voltage Vs:
In the step down mode an "output saturation volt" is 1.1V typical, 1.3VMAX.
In the step up mode an "Output saturation volt" is 0.45V typical, 0.7 maximum.
The desired peak current value is reached; the current limiting circuit turns ON & immediately terminates the ON time & starts OFF time.
• As we increase IL (load current), Vout will decrease, to compensate for this, the ON time of the output is increased automatically. If the I_L decreased then Vout increased, to compensate for this, the OFF time of the output is increased automatically.

(i) Step – Down Switching Regulator:

• CT is the timing capacitor which decides the switching frequency.
• Rsc is the current sensing resistance. Its value is given by
• The Non-inverting terminal of the internal op-amp (pin9) is connected to the 1.3V reference (pin8).
• Resistances R1 & R2 from a potential divider, across the output voltage Vo. Their value should be such that the potential at the inverting input of the op-amp should be equal to 1.3V ref when Vo is at its desired level. The output capacitance Co is used for reducing the ripple contents in the output voltage. It acts as a filter along with the inductor L.
• The inductor L is a part of filter connected on the output side, to reduce the ripple percentage.
• The 0.1μF capacitor connected between pin8 & ground bypasses any noise voltage coupled to the reference (pin8).

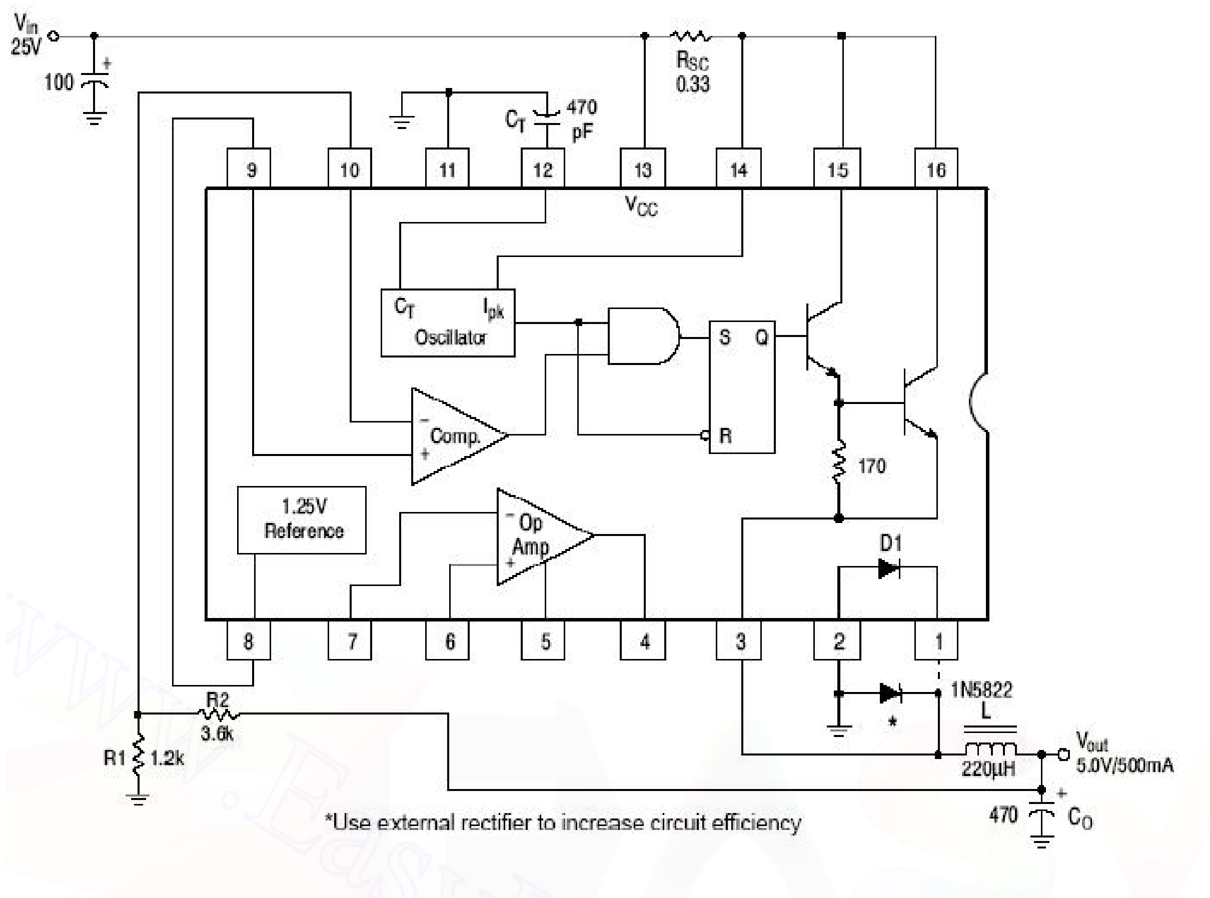


Fig. 5.38 Step down convertor

(ii) Step – Up Switching Regulator:

- Inductor is connected between the collectors of Q1 & Q2.
- When Q1 is ON, the output is shorted & the collector current of Q1 flows through L.
- The diode D1 is reverse biased & Co supplies the load current.
- The inductor stores the energy. When the Q1 is turned OFF, there is a self induced emf that appears across the inductor with polarities.
- The output voltage is given by,

$$V_o = V_{in} + V_L$$

- Hence it will be always higher than Vin & step up operation is achieved.

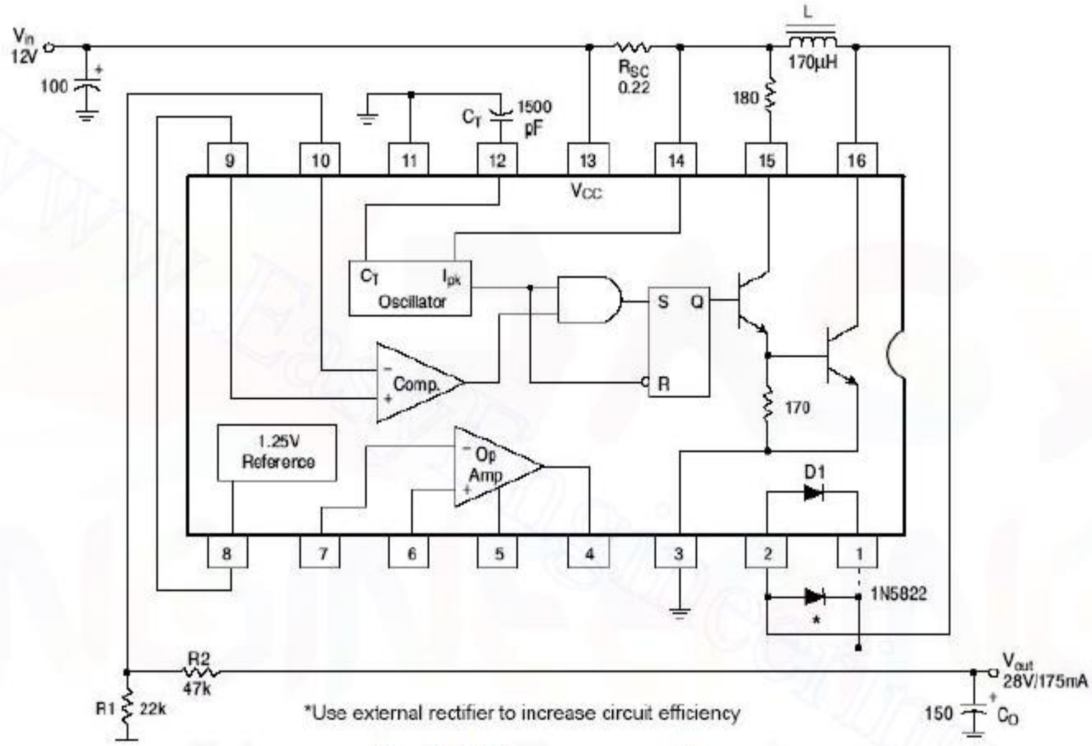
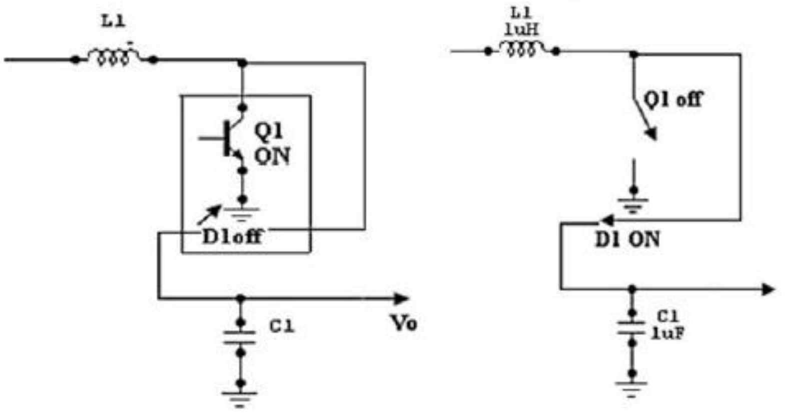


Fig.5.39 Step up convertor



With Q1 ON with Q1 oFF

(iii) Inverting Switching Regulator:

Inverting switching regulator converts a positive input voltage into a negative output voltage which is higher in magnitude.

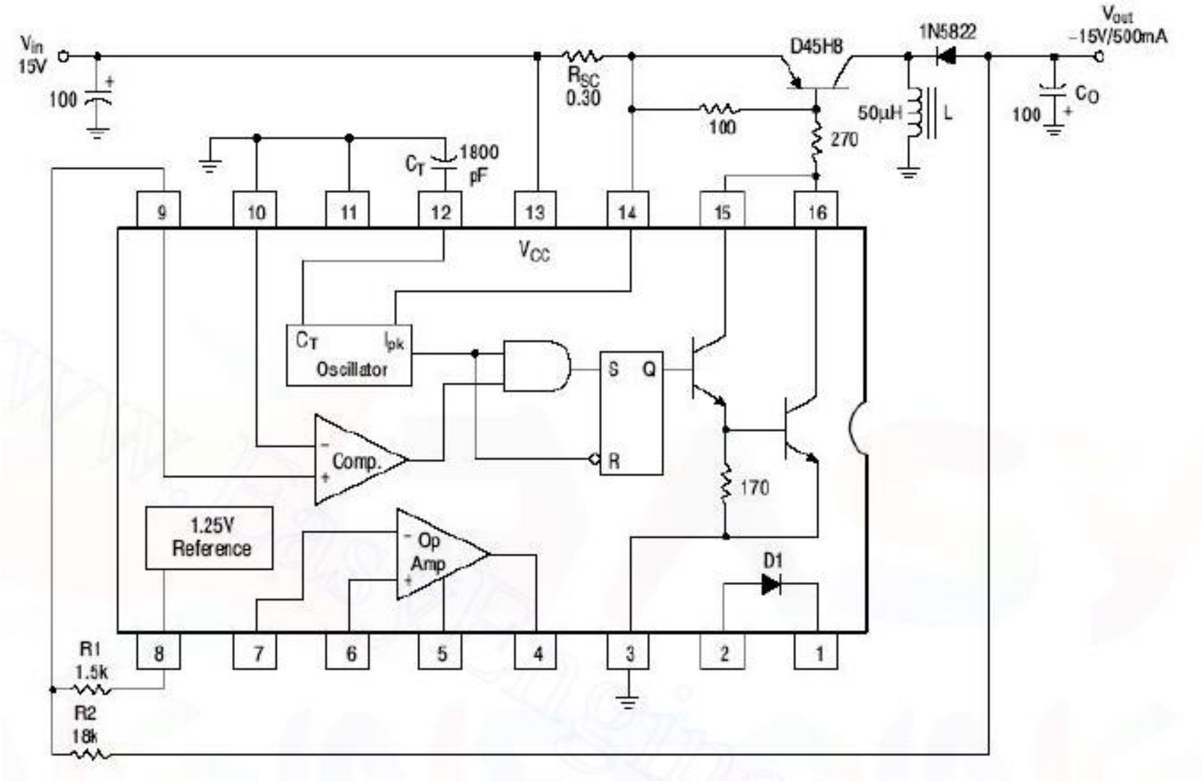


Fig.5.40 Circuit diagram of inverting switching regulator

5.9 The Switched Capacitor Filter

Basic Representation:

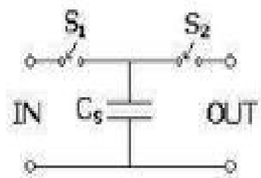


Fig 5.41 Switched-capacitor resistor

The simplest switched capacitor (SC) circuit is the switched capacitor resistor, made of one capacitor C and two switches S1 and S2 which connect the capacitor with a given frequency alternately to the input and output of the SC. Each switching cycle transfers a charge *q* from the input to the output at the switching frequency *f*. Recall that the charge *q* on a capacitor *C* with a voltage *V* between the plates is given by:

$$q = CV$$

where *V* is the voltage across the capacitor. Therefore, when S1 is closed while S2 is open, the charge transferred from the source to CS is:

$$q_{IN} = C_S V_{IN}$$

And when S2 is closed while S1 is open, the charge transferred from CS to the load is:

$$q_{OUT} = C_S V_{OUT}$$

Thus, the charge transferred in each cycle is:

$$q = q_{OUT} - q_{IN} = C_S (V_{OUT} - V_{IN})$$

Since a charge *q* is transferred at a rate *f*, the rate of transfer of charge per unit time is:

$$I = qf$$

Note that we use *I*, the symbol for electric current, for this quantity. This is to demonstrate that a continuous transfer of charge from one node to another is equivalent to a current. Substituting for *q* in the above, we have:

$$I = C_S (V_{OUT} - V_{IN}) f$$

Let us define V, the voltage across the SC from input to output, thus:

$$V = V_{OUT} - V_{IN}$$

We now have a relationship between I and V, which we can rearrange to give an equivalent resistance *R*:

$$R = \frac{V}{I} = \frac{1}{C_S f}$$

Thus, the SC behaves like a resistor whose value depends on *CS* and *f*.
The SC resistor is used as a replacement for simple resistors in integrated circuits because it is easier to fabricate reliably with a wide range of values. It also has the benefit that its value can be adjusted by changing the switching frequency. See also: operational amplifier applications.
This same circuit can be used in discrete time systems (such as analog to digital converters) as a track and hold circuit. During the appropriate clock phase, the capacitor samples the analog voltage through switch one and in the second phase presents this held sampled value to an electronic circuit for processing.

Switched Capacitor Circuits:

The switched capacitor filter allows for very sophisticated, accurate, and tuneable analog circuits to be manufactured without using resistors.

Advantages: resistors are hard to build on integrated circuits (they take up a lot of room), and the circuits can be made to depend on ratios of capacitor values (which can be set accurately), and not absolute values (which vary between manufacturing runs).

The Switched Capacitor Resistor:

Consider the circuit shown with a capacitor connected to two switches and two different voltages.

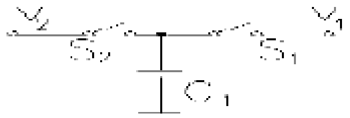


Fig.5.42 Example circuit

If S2 closes with S1 open, then S1 closes with switch S2 open, a charge (q is transferred from v2 to v1 with

$$\Delta q = C_1(v_2 \quad v_1)$$

If this switching process is repeated N times in a time (t, the amount of charge transferred per unit time is given by

$$\frac{\Delta q}{\Delta t} - C_1(v_2 - v_1)\frac{N}{\Delta t}$$

the number of cycles per unit time is the switching frequency (or clock frequency, fCLK)

$$i = C_1(v_2 - v_1)f_{CLK}$$

Rearranging we get

$$\frac{(v_2 \quad v_1)}{i} - \frac{1}{C_1 f_{CLK}} - R$$

Which states that the switched capacitor is equivalent to a resistor? The value of this resistor decreases with increasing switching frequency or increasing capacitance, as either will increase the amount of charge transferred from v2 to v1 in a given time.

The Switched Capacitor Integrator:

Now consider the integrator circuit. You have shown (in a previous lab) that the input-output relationship for this circuit is given by (neglecting initial conditions):

$$v_o(t) = -\frac{1}{RC_2}\int v_i(t)dt = -\omega'\int v_i(t)dt$$

We can also write this with the "s" notation (assuming a sinusoidal input, Aest, s=jω)

$$V_o(s) = -\frac{\omega'}{s}$$

If you replaced the input resistor with a switched capacitor resistor, you would get

$$\omega' = \frac{1}{RC_2} = f_{CLK}\frac{C_1}{C_2}$$

Thus, you can change the equivalent ω' of the circuit by changing the clock frequency. The value of ω' can be set very precisely because it depends only on the ratio of C1 and C2, and not their absolute value.

- ✓ **Switched Capacitor Filter ICs**:

Some of the Switched capacitor filter ICs is MF 5, MF10 and MF100

- ✓ **MF10:**

The MF10 contains two of the second-order universal filter sections found in the MF5. Therefore with MF10, two second order filters or one fourth-order filter can be built. As the MF5 and MF10 have similar filter sections, the design procedure for them is same.

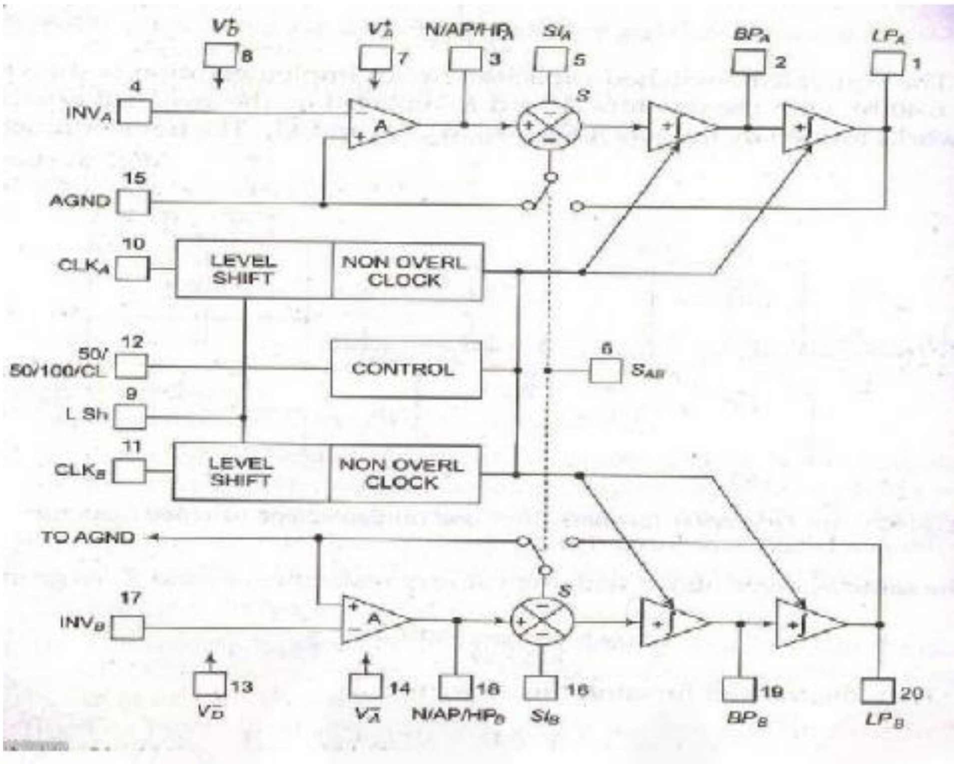


Fig.5.43 circuit connections of MF10

5.10 Frequency to Voltage (F-V) and voltage to frequency convertors (V-F)

• F-V convertors applications: Tachometer in motor speed control
Rotational speed measurement.
• Two types of it: Pulse integrating
Phase locked loop

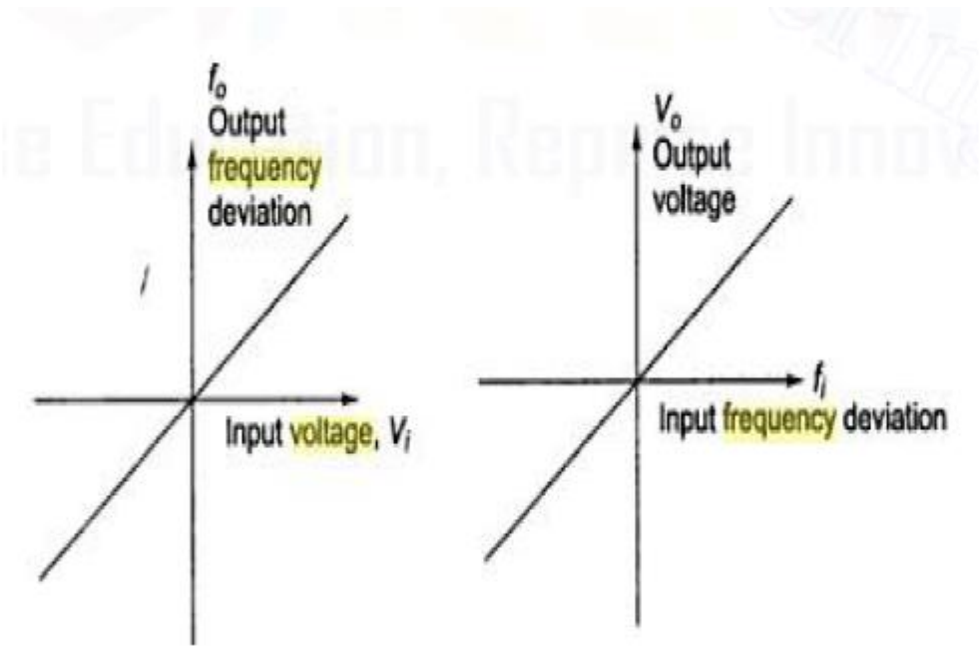
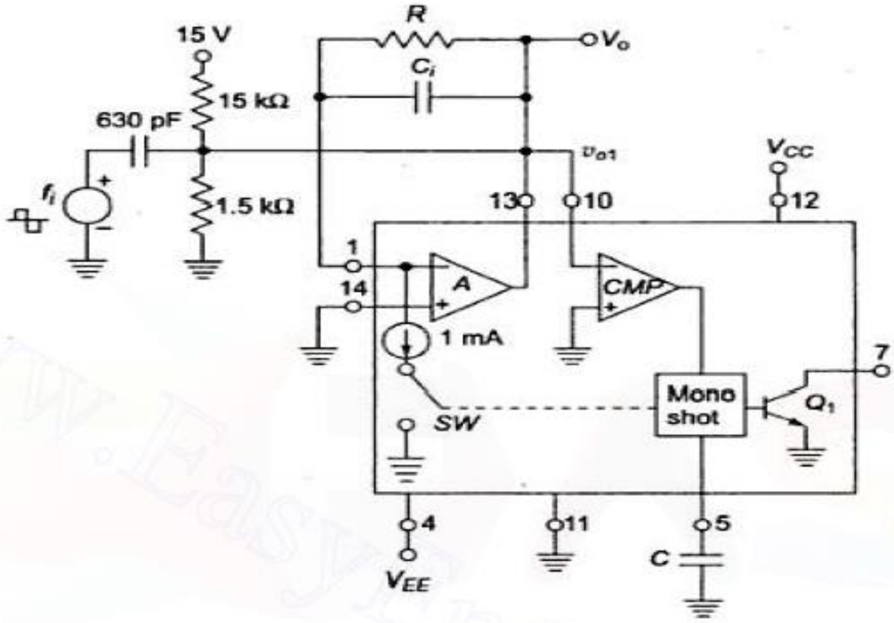


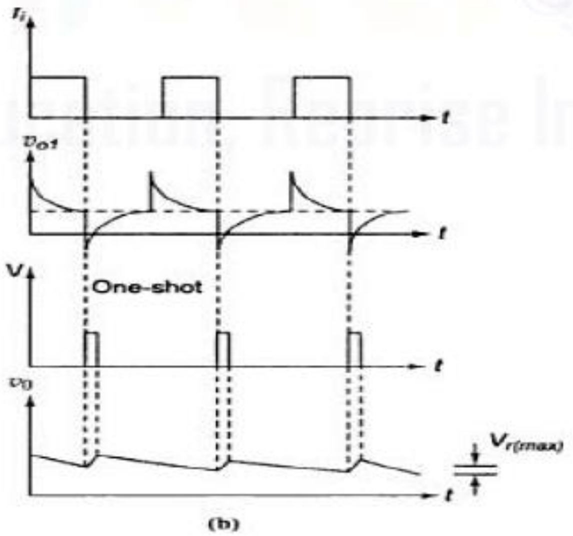
Fig. 5.44 Ideal characteristics of V-F convertor and F-V convertor

- F-V convertor produces an output voltage whose amplitude is a function of input signal frequency.
- $V0=k_f f_i$ kf is sensitivity of F-V convertor
- It is basically a FM discriminator.



(a)

Fig.5.45 Frequency To Voltage Convertor using VFC32 (V-F)



(b)

Fig.5.46 F-V Convertor using VF32 and input and output characteristics

Input frequency is applied to comparator A.
Resistor R acts as feedback element.
Capacitor Ci enables charge-balancing,
High pass network conditions input signal
For negative spike of V_{01}, comparator COMP triggers one shot multivibrator with threshold 7.5V The output of multivibrator closes the switch SW, for a time T_H, this causes voltage Vo

to build up and inject thru R and this continues until current out of summing input of opamp is equal to that injected by Vo through R continuously.

$V_o = 10^{-3} * T_H * R * f_i$ as $T_H = 7.5\ C / 1X10^{-3}$

Ripple Voltage, $V_r(max) = 7.5\ C / C_i$

5.10.2 Voltage to frequency convertor

Principle: Charge balancing technique-the process of charging and discharging results in frequency proportional to input signal $F_0 = k\ V_i$

Operation: Op-amp A converts input V_i to current $I_i = V_i/R$ into summing junction.
When switch SW is open the current flows into capacitor Ci and charges it, and node voltage Vo1 produce ramp down.
When $V_{01} = 0$ CMP triggers and sends a triggering signal to one shot multivibrator that closes the switch SW and turns transistor Q ON for time T_H.
The threshold of mono shot = 7.5 V and $T_H = 7.5\ C/10^{-3}$
During T_H, V_{01} ramps upward by amount $\Delta 01 = (1mA - I_i)\ T_H / Ci$
Time duration TL for vo1 to return to 0 is $TL = C\Delta 01 / I_i$

$$T_L + T_H = 1mA\ T_H / I_i = T$$

$$F_0 = V_i / 7.5\ RC$$

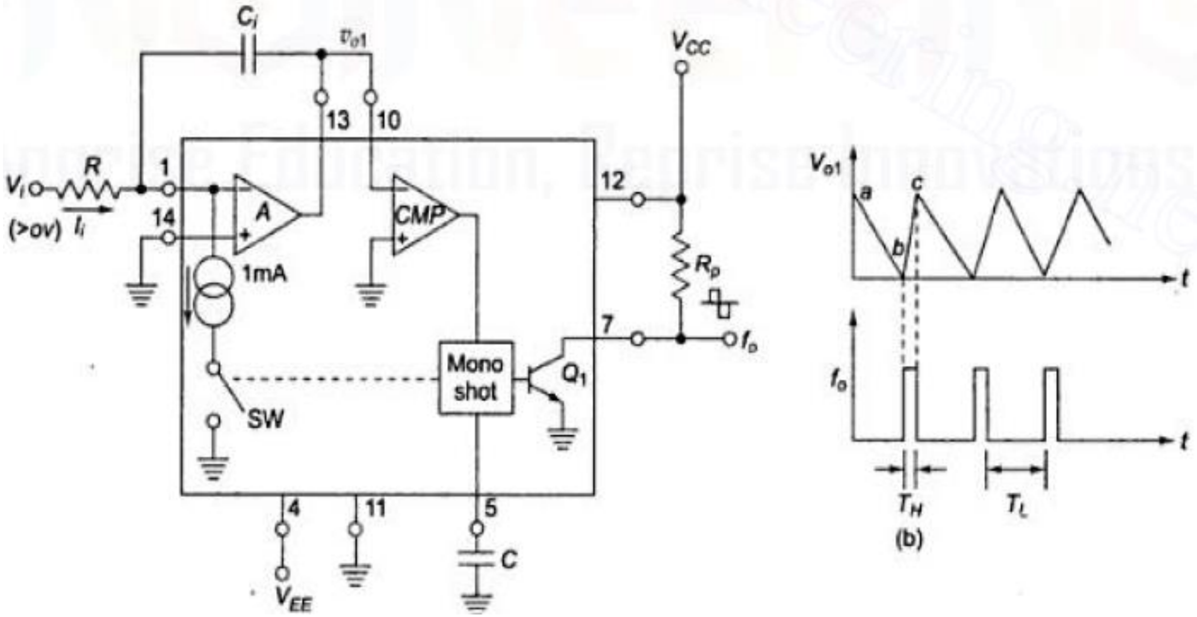


Fig.5.47 Voltage-Frequency convertor using VF32 and its input output characteristics

5.11 Power Audio Amplifier IC LM 380:

Introduction:

Small signal amplifiers are essentially voltage amplifier that supplies their loads with larger amplifier signal voltage. On the other hand, large signal or power amplifier supply a large signal current to current operated loads such as speakers & motors.

In audio applications, however, the amplifier called upon to deliver much higher current than that supplied by general purpose op-amps. This means that loads such as speakers & motors requiring substantial currents cannot be driven directly by the output of general purpose op-amps.

To handle it following is done

• To use discrete or monolithic power transistors called power boosters at the output of the op-amp

• To use specialized ICs designed as power amplifiers like LM 380.

✓ Features of LM380:

1. Internally fixed gain of 50 (34dB)
2. Output is automatically self centering to one half of the supply voltage.
3. Output is short circuit proof with internal thermal limiting.
4. Input stage allows the input to be ground referenced or ac
5. Wide supply voltage range (5 to 22V).
6. High peak current capability.
7. High impedance.

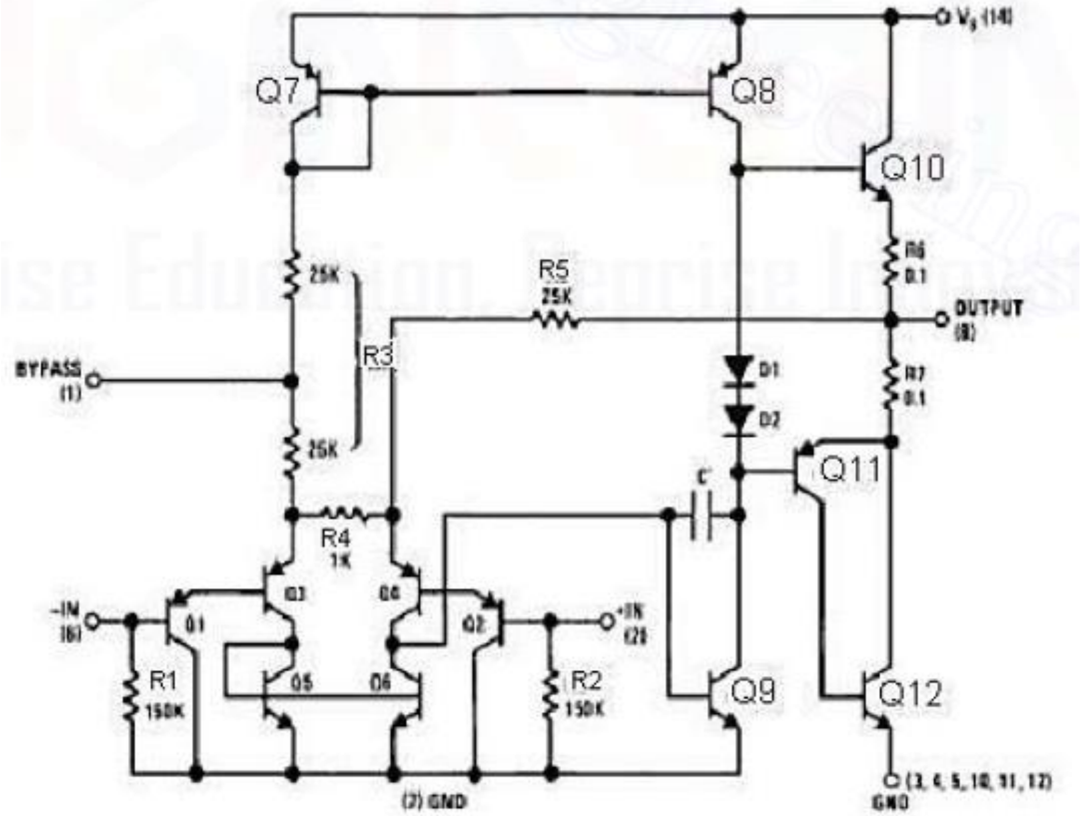


Fig.5.48 Functional block diagram of Audio Power Amplifier

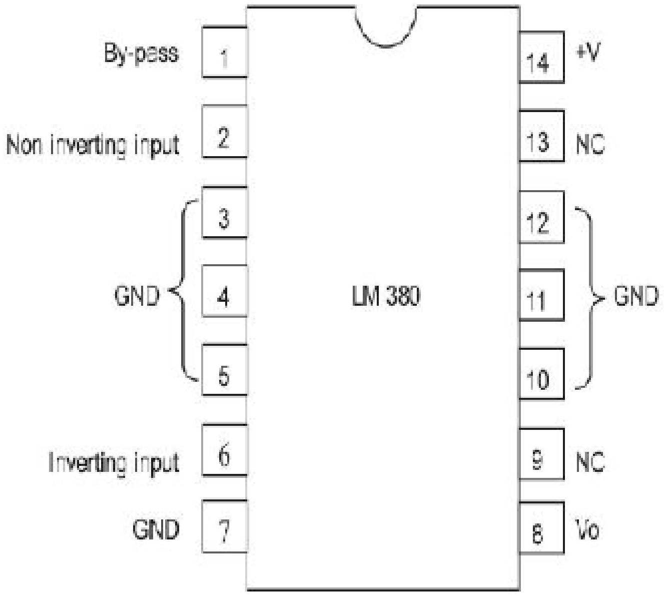


Fig.5.49 Pin diagram Of Power amplifier LM380

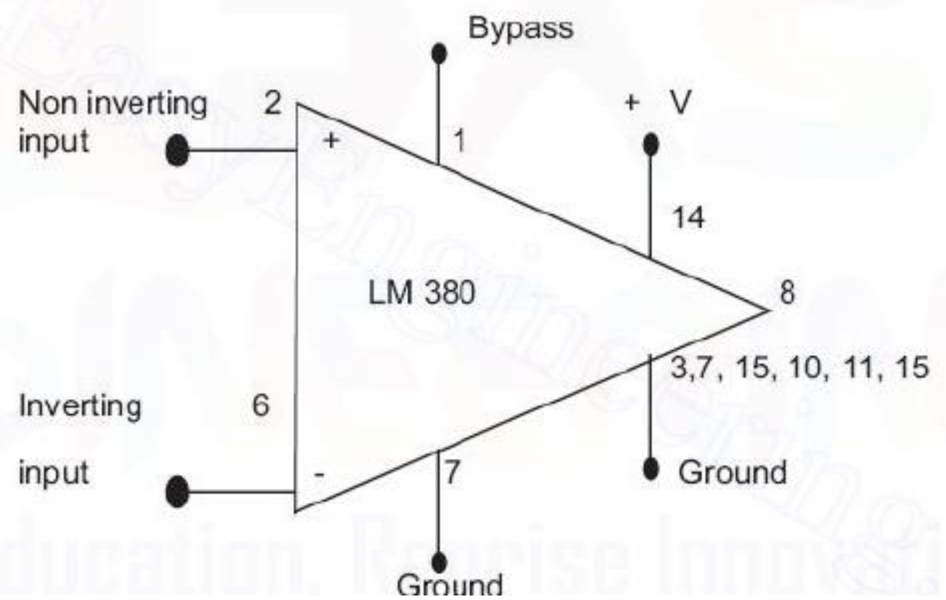


Fig.5.50 Block diagram of LM380

LM380 circuit description:
It is connected of 4 stages,
(i) PNP emitter follower
(ii) Different amplifier
(iii) Common emitter
(iv) Emitter follower
(i) PNP Emitter follower:
• The input stage is emitter follower composed of PNP transistors Q1 & Q2 which drives the PNP Q3-Q4 differential pair.

• The choice of PNP input transistors Q1 & Q2 allows the input to be referenced to ground i.e., the input can be direct coupled to either the inverting & non-inverting terminals of the amplifier.

(ii) Differential Amplifier:
• The current in the PNP differential pair Q3-Q4 is established by Q7, R3 & +V.
• The current mirror formed by transistor Q7, Q8 & associated resistors then establishes the collector current of Q9.
• Transistor Q5 & Q6 constitute of collector loads for the PNP differential pair.
• The output of the differential amplifier is taken at the junction of Q4 & Q6 transistors & is applied as an input to the common emitter voltage gain.
(iii) Common Emitter amplifier stage:
• Common Emitter amplifier stage is formed by transistor Q9 with D1, D2 & Q8 as a current source load.
• The capacitor C between the base & collector of Q9 provides internal compensation & helps to establish the upper cutoff frequency of 100 KHz.
• Since Q7 & Q8 form a current mirror, the current through D1 & D2 is approximately the same as the current through R3.
• D1 & D2 are temperature compensating diodes for transistors Q10 & Q11 in that D1 & D2 have the same characteristics as the base-emitter junctions of Q11. Therefore the current through Q10 & (Q11-Q12) is approximately equal to the current through diodes D1 & D2.
(iv) (Output stage) - Emitter follower:
• Emitter follower formed by NPN transistor Q10 & Q11. The combination of PNP transistor Q11 & NPN transistor Q12 has the power capability of NPN transistors but the characteristics of a PNP transistor.
• The negative dc feedback applied through R5 balances the differential amplifier so that the dc output voltage is stabilized at +V/2;
• To decouple the input stage from the supply voltage +V, by pass capacitor in order of micro farad should be connected between the bypass terminal (pin 1) & ground (pin 7).
• The overall internal gain of the amplifier is fixed at 50. However gain can be increased by using positive feedback.

✓ **Applications:**

(i) Audio Power Amplifier:

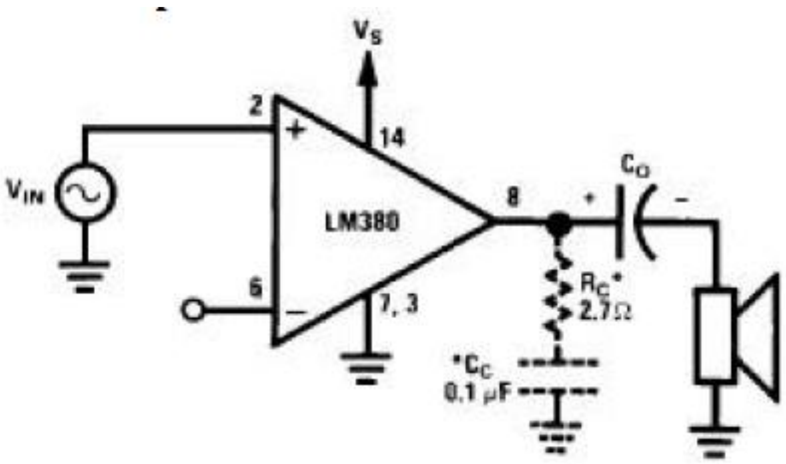


Fig. 5.51 Connections of audio power amplifier

- Amplifier requires very few external components because of the internal biasing, compensation & fixed gain.
- When the power amplifier is used in the non inverting configuration, the inverting terminal may be either shorted to ground, connected to ground through resistors & capacitors.
- Similarly when the power amplifier is used in the inverting mode, the non inverting terminal may be either shorted to ground or returned to ground through resistor or capacitor.
- Usually a capacitor is connected between the inverting terminal & ground if the input has a high internal impedance.
- As a precautionary measure, an RC combination should be used at the output terminal (pin 8) to eliminate 5-to-10 MHz oscillation.
- C1 is coupling capacitor which couples the output of the amplifier to the 8 ohms loud speaker which acts as a load. The amplifier will amplify the Vin applied at the non-inverting terminal.

(ii) LM 380 as a High gain amplifier:

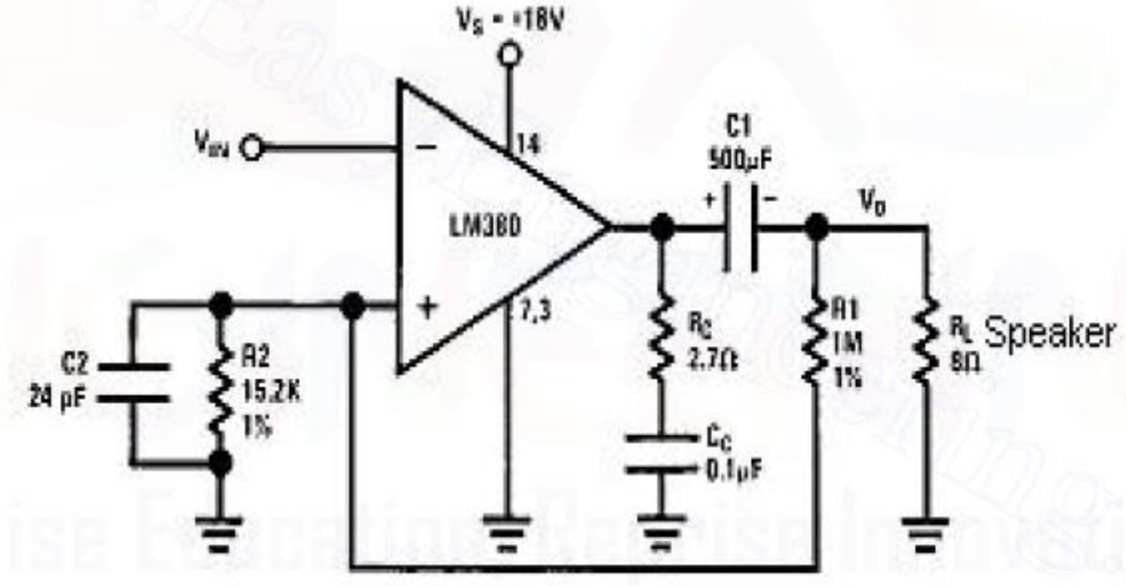


Fig.5.52 Circuit connections

- The gain of LM380 is internally fixed at 50. But it can be increased by using the external components.
- The increase in gain is possible due to the use of positive feedback, this setup to obtain a gain 200.

(iii) LM 380 as a variable Gain:

- Instead of getting a fixed gain of 50, it is possible to obtain a variable gain up to 50 by connecting a potentiometer between the input terminals.

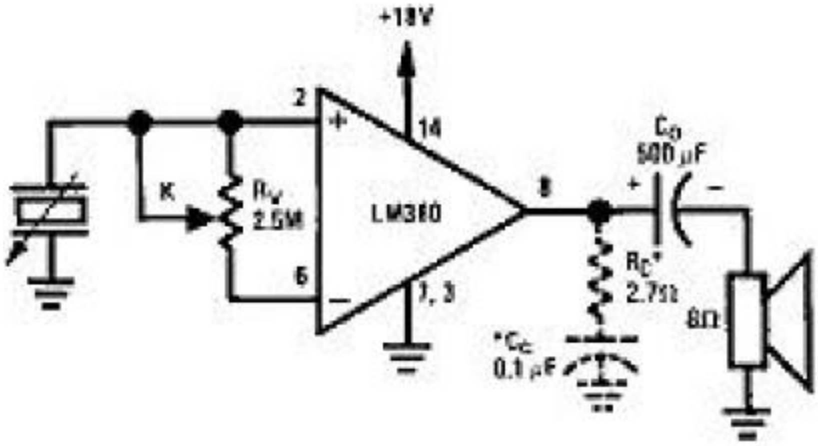


Fig. 5.53 Circuit connections

(iv) LM 380 as a Bridge Audio Power Amplifier:

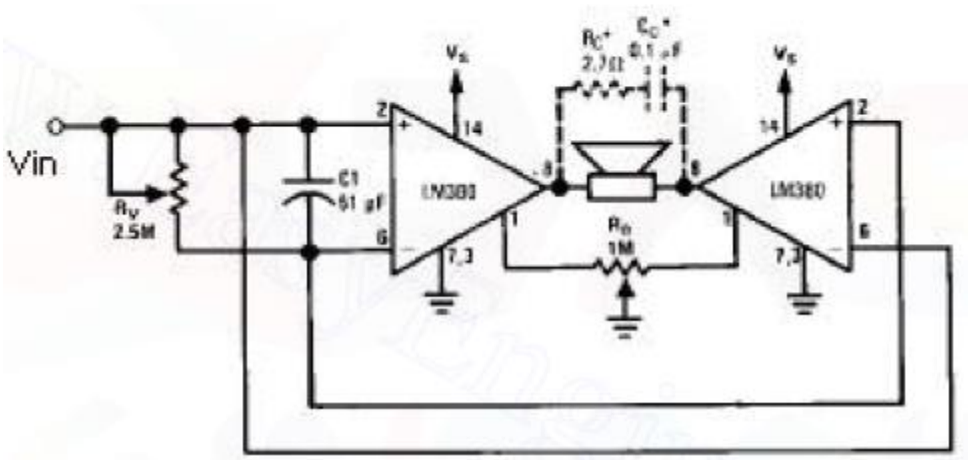


Fig. 5.54 Circuit connections

- If a certain application requires more power than what is provided by a single LM380 amplifier, then 2 LM380 chips can be used in the bridge configuration.
- With this arrangement we get an output voltage swing which is twice that of a single LM380 amplifier.
- As the voltage is doubled, power output will increase by four times that of a single LM380 amplifier. The pot R4 is used to balance the output offset voltages of the two chips.

(v) Intercom system using LM 380:

- When the switch is in Talk mode position, the master speaker acts as a microphone.
- When the switch is in Listen position, the remote speaker acts as a microphone.
- In either phone the overall gain of the circuit is the same depends on the turns of transformer T.

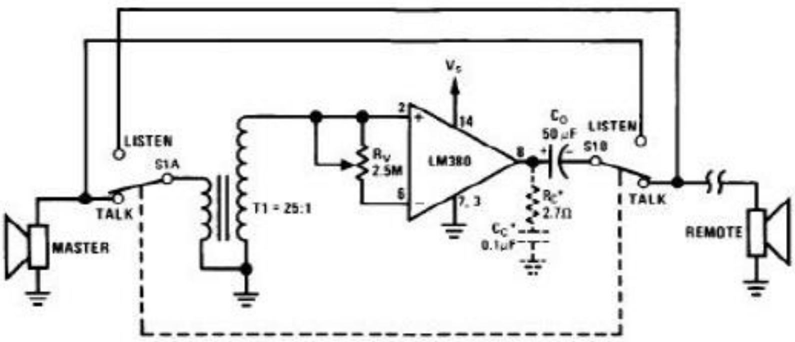


Fig. 5.55 Talk mode

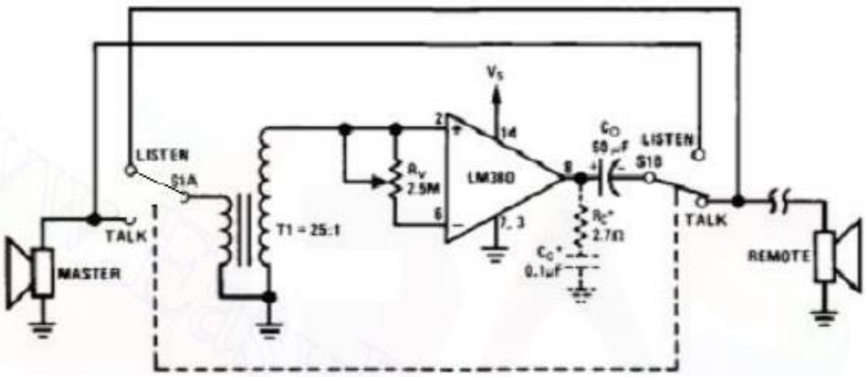


Fig.5.56 Listen mode

5.12 Monolithic video amplifier

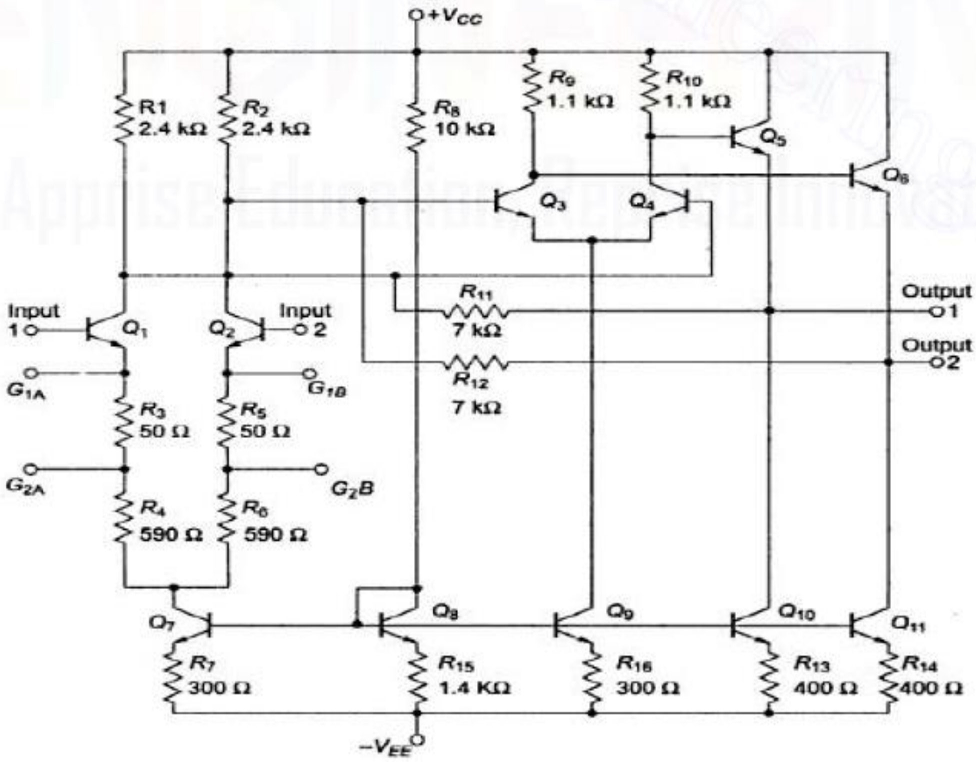


Fig.5.57 Monolithic video amplifier

5.13 Opto couplers/Opto Isolators and fibre optic IC

• Opto couplers or Opt isolators is a combination of light source & light detector in the same package.

• They are used to couple signal from one point to other optically, by providing a complete electric isolation between them. This kind of isolation is provided between a low power control circuit & high power output circuit, to protect the control circuit.

• Characteristics of opto coupler:

(i) Current Transfer Ratio:

It is defined as the ratio of output collector current (Ic) to the input forward current (If)

CTR = Ic/If * 100%. Its value depends on the devices used as source & detector.

(ii) Isolation voltage between input & output:

It is the maximum voltage which can exist differentially between the input & output without affecting the electrical isolation voltage is specified in K Vrms with a relative humidity of 40 to 60%.

(iii) Response Time:

Response time indicates how fast an opto coupler can change its output state. Response time largely depends on the detector transistor, input current & load resistance.

(iv) Common mode Rejection:

Even though the opto couplers are electrically isolated for dc & low frequency signals, an impulsive input signal (the signal which changes suddenly) can give rise to a displacement current Ic= Cf*dv/dt. This current can flow between input & output due to the capacitance Cf existing between input & output. This allows the noise to appear in the output. Depending on the type of light source & detector used we can get a variety of opto couplers.

They are as follows,

(i) LED – Photodiode opto coupler:

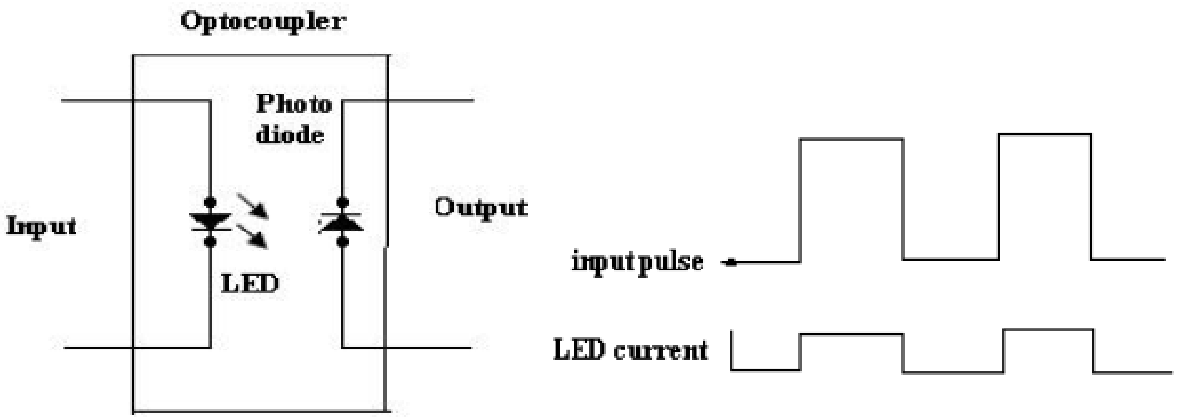


Fig.5.58 Schematic symbol and waveforms

• LED photodiode shown in figure, here the infrared LED acts as a light source & photodiode is used as a detector.

• The advantage of using the photodiode is its high linearity. When the pulse at the input goes high, the LED turns ON. It emits light. This light is focused on the photodiode.

• In response to this light the photocurrent will start flowing though the photodiode. As soon as the input pulse reduces to zero, the LED turns OFF & the photocurrent through the photodiode reduces to zero. Thus the pulse at the input is coupled to the output side.

(ii) LED – Phototransistor Opto coupler:

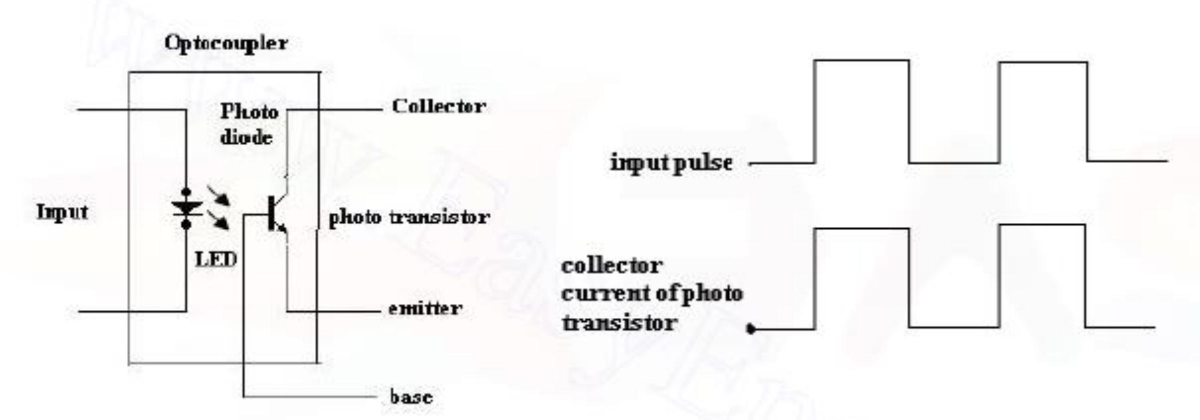


Fig.5.59 Schematic symbol and waveforms

• The LED phototransistor opto coupler shown in figure. An infrared LED acts as a light source and the phototransistor acts as a photo detector.
• This is the most popularly used opto coupler, because it does not need any additional amplification.
• When the pulse at the input goes high, the LED turns ON. The light emitted by the LED is focused on the CB junction of the phototransistor.
• In response to this light photocurrent starts flowing which acts as a base current for the phototransistor.
• The collector current of phototransistor starts flowing. As soon as the input pulse reduces to zero, the LED turns OFF & the collector current of phototransistor reduces to zero. Thus the pulse at the input is optically coupled to the output side.
• The input & output waveforms are 180º out of phase as the output is taken at the collector of the phototransistor

Advantages of Opto coupler:

- ✓ Control circuits are well protected due to electrical isolation.
- ✓ Wideband signal transmission is possible.
- ✓ Due to unidirectional signal transfer, noise from the output side does not get coupled to the input side.
- ✓ Interfacing with logic circuits is easily possible.
- ✓ It is small size & light weight device.

Disadvantages:

- ✓ Slow speed.
- ✓ Possibility of signal coupling for high power signals.

Applications:

Opto couplers are used basically to isolate low power circuits from high power circuits.
• At the same time the control signals are coupled from the control circuits to the high power circuits.
• Some of such applications are,
(i) AC to DC converters used for DC motor speed control
(ii) High power choppers
(iii) High power inverters
• One of the most important applications of an opto coupler is to couple the base driving signals to a power transistor connected in a DC-DC chopper.

Opto coupler IC:

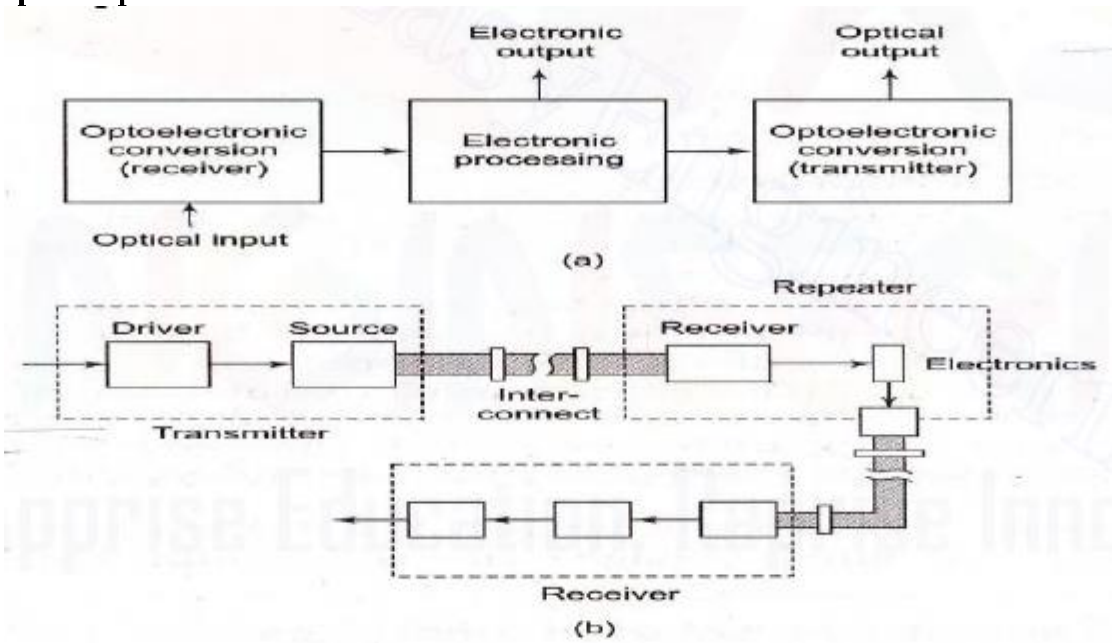


Fig. 5.60 The block diagram of opto-electronic-integrated circuit (OEIC)

The optocouplers are available in the IC form MCT2E is the standard optocoupler IC which is used popularly in many electronic application.
• This input is applied between pin 1& pin 2. An infrared light emitting diode is connected between these pins.
• The infrared radiation from the LED gets focused on the internal phototransistor.
• The base of the phototransistor is generally left open. But sometimes a high value pull down resistance is connected from the Base to ground to improve the sensitivity.
• The block diagram shows the opto-electronic-integrated circuit (OEIC) and the major components of a fiber-optic communication facility.
• The block diagram shows the opto-electronic-integrated circuit (OEIC) and the major components of a fiber-optic communication facility.