JEPPIAAR INSTITUTE OF TECHNOLOGY

"Self-Belief | Self Discipline | Self Respect"

DEPARTMENT

OF

ELECTRONICS AND COMMUNICATION ENGINEERING

LECTURE NOTES

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UNIT IV ANALOG TO DIGITAL AND DIGITAL TO ANALOG CONVERTERS **9**

Analog and Digital Data Conversions, D/A converter – specifications - weighted resistor type, R-2R Ladder type, Voltage Mode and Current-Mode *R - 2R* Ladder types - switches for D/A converters, high speed sample-and-hold circuits, A/D Converters – specifications - Flash type - Successive Approximation type - Single Slope type – Dual Slope type - A/D Converter using Voltage-to-Time Conversion - Over-sampling A/D Converters, Sigma – Delta converters.

4. 1 1Analog To Digital Conversion

The natural state of audio and video signals is analog. When digital technology was not yet around, they are recorded or played back in analog devices like vinyl discs and cassette tapes. The storage capacity of these devices is limited and doing multiple runs of re-recording and editing produced poor signal quality. Developments in digital technology like the CD, DVD, Blu-ray, flash devices and other memory devices addressed these problems. For these devices to be used, the analog signals are first converted to digital signals using analog to digital conversion (ADC). For the recorded audio and video signals to be heard and viewed again, the reverse process of digital to analog conversion (DAC) is used. ADC and DAC are also used in interfacing digital circuits to analog systems. Typical applications are control and monitoring of temperature, water level, pressure and other real-world data.

An ADC inputs an analog signal such as voltage or current and outputs a digital signal in the form of a binary number. A DAC, on the other hand, inputs the binary number and outputs the corresponding analog voltage or current signal.

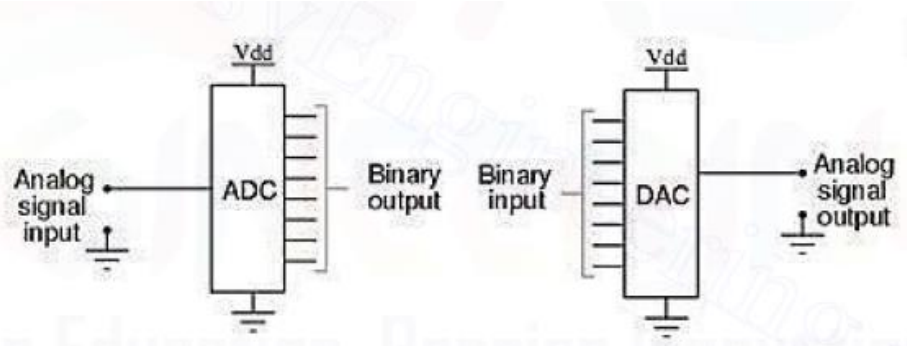


Fig 4.1 ADC and DAC circuits

- ✓ Sampling rate

The analog signal is continuous in time and it is necessary to convert this to a flow of

digital values. It is therefore required to define the rate at which new digital values are sampled from the analog signal. The rate of new values is called the *sampling rate* or *sampling frequency* of the converter. A continuously varying band limited signal can be sampled (that is, the signal values at intervals of time T, the sampling time, are measured and stored) and then the original signal can be *exactly*

reproduced from the discrete-time values by an interpolation formula. The accuracy is limited by quantization error. However, this faithful reproduction is only possible if the sampling rate is higher than twice the highest frequency of the signal. This is essentially what is embodied in the Shannon-Nyquist sampling theorem.

Since a practical ADC cannot make an instantaneous conversion, the input value must necessarily be held constant during the time that the converter performs a conversion (called the *conversion time*). An input *c*ircuit called a sample and hold performs this task—in most cases by using a capacitor to store the analog voltage at the input, and using an electronic switch or gate to disconnect the capacitor from the input. Many ADC integrated circuits include the sample and hold subsystem internally.

✓ Accuracy

An ADC has several sources of errors. Quantization error and (assuming the ADC is intended to be linear) non-linearity is intrinsic to any analog-to-digital conversion. There is also a so called *aperture error* which is due to a clock jitter and is revealed when digitizing a time-variant signal (not a constant value). These errors are measured in a unit called the *LSB*, which is an abbreviation for least significant

bit. In the above example of an eight-bit ADC, an error of one LSB is 1/256 of the full signal range, or about 0.4%.

✓ Quantization error

Quantization error is due to the finite resolution of the ADC, and is an unavoidable imperfection in all types of ADC. The magnitude of the quantization error at the sampling instant is between zero and half of one LSB. In the general case, the original signal is much larger than one LSB. When this happens, the quantization error is not correlated with the signal, and has a uniform distribution. Its RMS value is the standard deviation of this distribution, given by

$$\frac{1}{\sqrt{12}}\text{LSB} \approx 0.289\,\text{LSB}.$$

In the eight-bit ADC example, this represents 0.113% of the full signal range.

At lower levels the quantizing error becomes dependent of the input signal, resulting in distortion. This distortion is created after the anti-aliasing filter, and if these distortions are above 1/2 the sample rate they will alias back into the audio band. In order to make the Quantizing error independent of the input signal, noise with amplitude of 1 quantization step is added to the signal. This slightly reduces signal to noise ratio, but completely eliminates the distortion. It is known as dither.

✓ Non-linearity

All ADCs suffer from non-linearity errors caused by their physical imperfections, resulting in their output to deviate from a linear function (or some other function, in the case of a deliberately nonlinear ADC) of their input. These errors can sometimes be mitigated by calibration, or prevented by testing. Important parameters for linearity are integral non-linearity (INL) and differential non- linearity (DNL). These non-linear ties reduce the dynamic range of the signals that can be digitized by the
ADC, also reducing the effective resolution of the ADC.

D To A Converter- Specifications

D/A converters are available with wide range of specifications specified by manufacturer. Some of the important specifications are Resolution, Accuracy, linearity, monotonicity, conversion time, settling time and stability.

✓ Resolution:

Resolution is defined as the number of different analog output voltage levels that can be provided by a DAC. Or alternatively resolution is defined as the ratio of a change in output voltage resulting for a change of 1 LSB at the digital input. Simply, resolution is the value of LSB.

Resolution (Volts) = VoFS / (2 n - 1) = 1 LSB
increment Where ‘n’ is the number of input bits
‘VoFS’ is the full scale output voltage.
Example:
Resolution for an 8 – bit DAC for example is said to have

: 8 – bit resolution

: A resolution of 0.392 of full-Scale (1/255)

: A resolution of 1 part in 255.

Thus resolution can be defined in many different ways.

he following table shows the resolution for 6 to 16 bit DACs

Table 4.1 Resolution for DAC

S.No.	Bits	Intervals	LSB size (% of full-scale)	LSB size (For a 10 V full-scale)
1.	6	63	1.588	158.8 mV
2.	8	255	0.392	39.2 mV
3.	10	1023	0.0978	9.78 mV
4.	12	4095	0.0244	2.44 mV
5.	14	16383	0.0061	0.61 mV
6.	16	65535	0.0015	0.15 mV

✓ Accuracy:

Absolute accuracy is the maximum deviation between the actual converter output and the ideal converter output. The ideal converter is the one which does not suffer from any problem. Whereas, the actual converter output deviates due to the drift in component values, mismatches, aging, noise and other sources of errors.

The relative accuracy is the maximum deviation after the gain and offset errors have been removed. Accuracy is also given in terms of LSB increments or percentage of full-scale voltage. Normally, the data sheet of a D/A converter specifies the relative accuracy rather than absolute accuracy.

✓ Linearity:

Linearity error is the maximum deviation in step size from the ideal step size. Some D/A converters are having a linearity error as low as 0.001% of full scale. The linearity of a D/A converter is defined as the precision or exactness with which the digital input is converted into analog output. An ideal D/A converter produces equal increments or step sizes at output for every change in equal increments of binary input.

✓ Monotonicity:

A Digital to Analog converter is said to be monotonic if the analog output increases for an increase in the digital input. A monotonic characteristic is essential in control applications.

Otherwise it would lead to oscillations. If a DAC has to be monotonic, the error should be less than ± (1/2) LSB at each output level. Hence all the D/A converters are designed such that the linearity error satisfies the above condition.

When a D/A Converter doesn't satisfy the condition described above, then, the output voltage may decrease for an increase in the binary input.

✓ Conversion Time:

It is the time taken for the D/A converter to produce the analog output for the given binary input signal. It depends on the response time of switches and the output of the Amplifier. D/A converters speed can be defined by this parameter. It is also called as setting time.

✓ Settling time:

It is one of the important dynamic parameter. It represents the time it takes for the output to settle within a specified band ± (1/2) LSB of its final value following a code change at the input (Usually a full-scale change). It depends on the switching time of the logic circuitry due to internal parasitic capacitances and inductances. A typical settling time ranges from 100 ns to 10 μs depending on the word length and type of circuit used.

✓ Stability:

The ability of a DAC to produce a stable output all the time is called as Stability. The performance of a converter changes with drift in temperature, aging and power supply variations. So all the parameters such as offset, gain, linearity error & monotonicity may change from the values specified in the datasheet. Temperature sensitivity defines the stability of a D/A converter.

4.2 Digital To Analog Conversion

A DAC converts an abstract finite-precision number (usually a fixed-point binary number) into a concrete physical quantity (e.g., a voltage or a pressure). In particular, DACs are often used to convert finite-precision time series data to a continually-varying physical signal. A typical DAC converts the abstract numbers into a concrete sequence of impulses that are then processed by a reconstruction filter using some form of interpolation to fill in data between the impulses. Other DAC methods (e.g., methods based on Delta-sigma modulation) produce a pulsedensity

modulated signal that can then be filtered in a similar way to produce a smoothly-varying signal.By the Nyquist–Shannon sampling theorem, sampled data can be reconstructed perfectly provided that its bandwidth meets certain requirements (e.g., a baseband signal with bandwidth less than the Nyquist frequency). However, even with an ideal reconstruction filter, digital

sampling introduces quantization that makes perfect reconstruction practically impossible. Increasing the digital resolution (i.e., increasing the number of bits used in each sample) or introducing sampling dither can reduce this error. DACs are at the beginning of the analog signal chain, which makes them very important to system performance. The most important characteristics of these devices are:

4.3 Specifications:

✓ Resolution: This is the number of possible output levels the DAC is designed to reproduce. This is usually stated as the number of bits it uses, which is the base two logarithm of the number of levels. For instance a 1 bit DAC is designed to reproduce 2 (21) levels while an 8 bit DAC is designed for 256 (28) levels. Resolution is related to the

✓ Effective number of bits (ENOB) which is a measurement of the actual resolution attained by the DAC.

✓ Maximum sampling frequency: This is a measurement of the maximum speed at which the DACs circuitry can operate and still produce the correct output. As stated in the Nyquist–Shannon sampling theorem, a signal must be sampled at over twice the frequency of the desired signal. For instance, to reproduce signals in all the audible spectrum, which includes frequencies of up to 20 kHz, it is necessary to use DACs that operate at over 40 kHz. The CD standard samples audio at kHz, thus DACs of this frequency are often used. A common frequency in cheap computer sound cards is 48 kHz—many work at only this frequency, offering the use of other sample rates only through (often poor) internal resampling.

✓ Monotonicity: This refers to the ability of a DAC's analog output to move only in the direction that the digital input moves (i.e., if the input increases, the output doesn't dip before asserting the correct output.) This characteristic is very important for DACs used as a low frequency signal source or as a digitally programmable trim element.

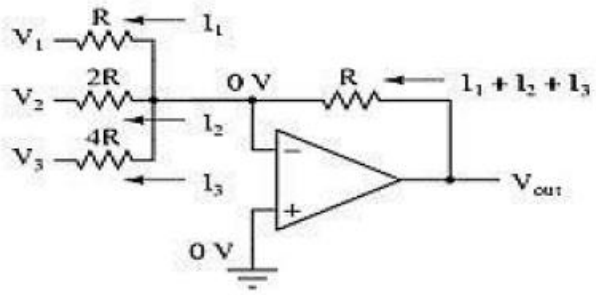
✓ THD+N: This is a measurement of the distortion and noise introduced to the signal by the DAC. It is expressed as a percentage of the total power of unwanted harmonic distortion and noise that accompany the desired signal. This is a very important DAC characteristic for dynamic and small signal DAC applications.

✓ Dynamic range: This is a measurement of the difference between the largest and smallest signals the DAC can reproduce expressed in decibels. This is usually related to DAC resolution

and noise floor. Other measurements, such as phase distortion and sampling period instability, can also be very important for some applications.

4.4 Binary-Weighted Resistor DAC

The binary-weighted-resistor DAC employs the characteristics of the inverting summer Op Amp circuit. In this type of DAC, the output voltage is the inverted sum of all the input voltages. If the input resistor values are set to multiples of two: 1R, 2R and 4R, the output voltage would be equal to the sum of V1, V2/2 and V3/4. V1 corresponds to the most significant bit (MSB) while V3 corresponds to the least significant bit (LSB).



$$V_{out} = -\left(V_1 + \frac{V_2}{2} + \frac{V_3}{4}\right)$$

Fig. 4.2 Binary weighted DAC

The circuit for a 4-bit DAC using binary weighted resistor network is shown below:

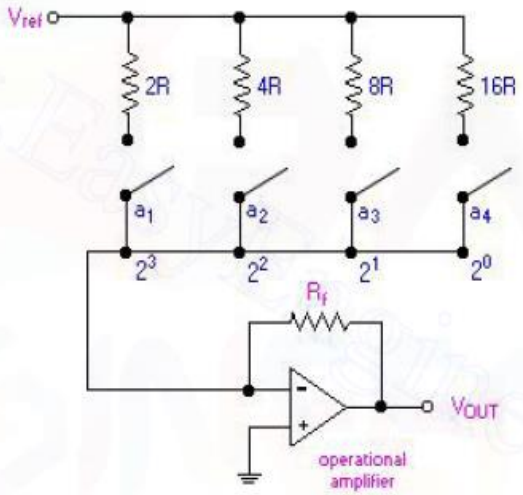


Fig. 4.3 weighted resistor DAC using Op-amp

The binary inputs, ai (where i = 1, 2, 3 and 4) have values of either 0 or 1. The value, 0, represents an open switch while 1 represents a closed switch.

The operational amplifier is used as a summing amplifier, which gives a weighted sum of the binary input based on the voltage, Vref.

For a 4-bit DAC, the relationship between Vout and the binary input is as follows:

$$\begin{aligned} V_{OUT} &= -iR_f \\ &= -\left[V_{ref}\left(\frac{a_1}{2R} + \frac{a_2}{4R} + \frac{a_3}{8R} + \frac{a_4}{16R}\right)\right]R_f \\ &= -\frac{V_{ref}R_f}{R}\left(\frac{a_1}{2} + \frac{a_2}{4} + \frac{a_3}{8} + \frac{a_4}{16}\right) \\ &= -\frac{V_{ref}R_f}{R}\left(\frac{a_1}{2^1} + \frac{a_2}{2^2} + \frac{a_3}{2^3} + \frac{a_4}{2^4}\right) \end{aligned}$$

The negative sign associated with the analog output is due to the connection to a summing amplifier, which is a polarity-inverting amplifier. When a signal is applied to the latter type of amplifier, the polarity of the signal is reversed (i.e. a + input becomes -, or vice versa).

For a n-bit DAC, the relationship between Vout and the binary input is as follows:

$$V_{OUT} = -\frac{V_{ref} R_f}{R} \sum_{i=1}^{n} \frac{a_i}{2^i}$$

The LSB, which is also the incremental step, has a value of - 0.625 V while the MSB or the full scale has a value of - 9.375 V.

Practical Limitations:

- The most significant problem is the large difference in resistor values required between the LSB and MSB, especially in the case of high resolution DACs (i.e. those that has large number of bits). For example, in the case of a 12-bit DAC, if the MSB is 1 k Ω, then the LSB is a staggering 2 MΩ.
- The maintenance of accurate resistances over a large range of values is problematic. With the current IC fabrication technology, it is difficult to manufacture resistors over a wide resistance range that maintains an accurate ratio especially with variations in temperature.

4.5 R-2R Ladder DAC

An enhancement of the binary-weighted resistor DAC is the R-2R ladder network. This type of DAC utilizes Thevenin's theorem in arriving at the desired output voltages. A disadvantage of the former DAC design was its requirement of several different precise input resistor values: one unique value per binary input bit.

The R-2R network consists of resistors with only two values - R and 2xR. If each input is supplied either 0 volts or reference voltage, the output voltage will be an analog equivalent of the binary value of the three bits. VS_2 corresponds to the most significant bit (MSB) while VS_0 corresponds to the least significant bit (LSB).

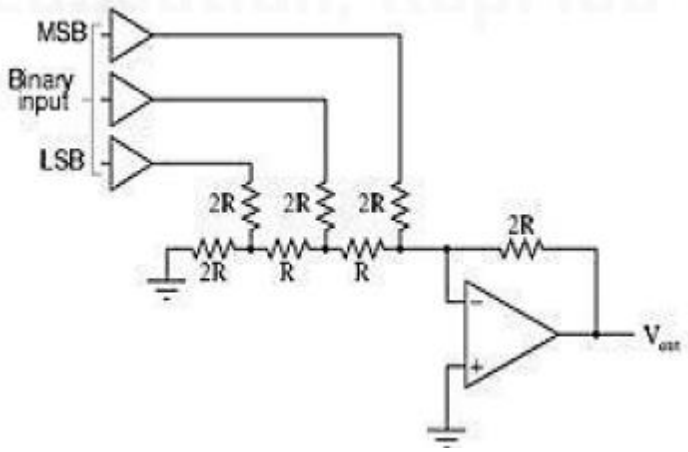


Fig.4.4 Ladder type DAC circuit

Vout = - (VMSB + Vn + VLSB) = - (VRef + VRef/2 + VRef/ 4)

Table 4.2 operation of a R-2R ladder DAC

Binary	Output voltage
000	0.00 V
001	-1.25 V
010	-2.50 V
011	-3.75 V
100	-5.00 V
101	-6.25 V
110	-7.50 V
111	-8.75 V

4.6 Inverted Or Current Mode DAC

Current mode DACs operates based on the ladder currents. The ladder is formed by

resistance R in the series path and resistance 2R in the shunt path. Thus the current is divided into *i*1 , *i*2, *i*3 ……*i*n. in each arm. The currents are either diverted to the ground bus (*io*) or to the Virtual-ground bus *(io*).

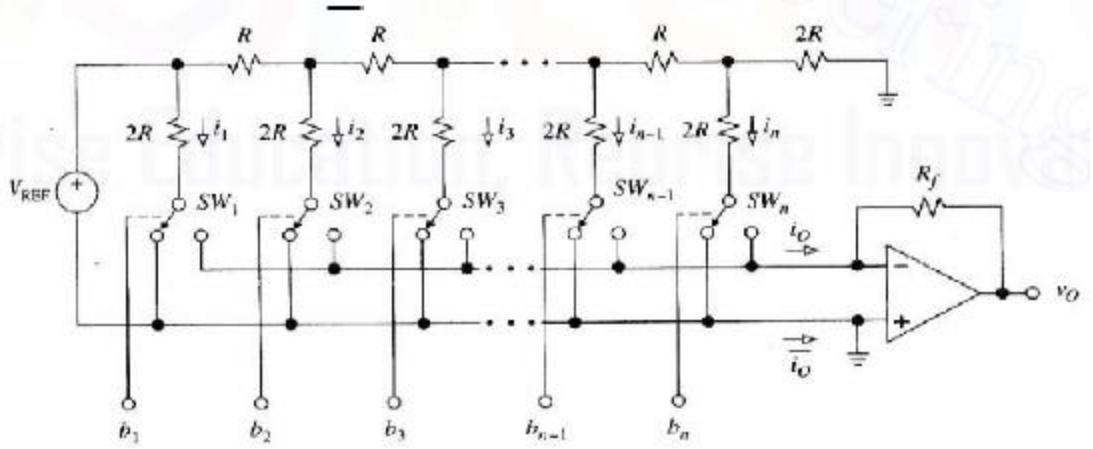


Fig.4.5 Current mode DAC

The currents are given as

*i*1 = V_{REF}/2R = (V_{REF}/R) 2-1, *i*2 = (V_{REF})/2)/2R = (V_{REF}/R) 2-2……*in* = (V_{REF}/R) 2-n.

And the relationship between the currents are given as

i2 = i1/2

i3 = i1/4

i4 = i1/8

in = i1/ 2^{n-1}

Using the bits to identify the status of the switches, and letting V0 = -Rf *io* gives

V0 = - (Rf/R) VREF (b12-1 + b22-2+ …….. + bn2-n)

The two currents *io* and *io* are complementary to each other and the potential of *io* bus must be sufficiently close to that of the *io* bus. Otherwise, linearity errors will occur. The final opamp is used as current to voltage converter.

Advantages

1. The major advantage of current mode D/A converter is that the voltage change across each switch is minimal. So the charge injection is virtually eliminated and the switch driver design is made simpler.

2. In Current mode or inverted ladder type DACs, the stray capacitance do not affect the Speed of response of the circuit due to constant ladder node voltages. So improved speed performance.

✓ Voltage Mode DAC

This is the alternative mode of DAC and is called so because the 2R resistance in the shunt path is switched between two voltages named as VL and VH. The output of this DAC is obtained from the leftmost ladder node. As the input is sequenced through all the possible binary state starting from All 0s (0…..0) to all 1s (1…..1). The voltage of this node changes in steps of 2-n (VH - VL) from the minimum voltage of Vo = VL to the maximum of Vo = VH - 2-n (VH - VL).

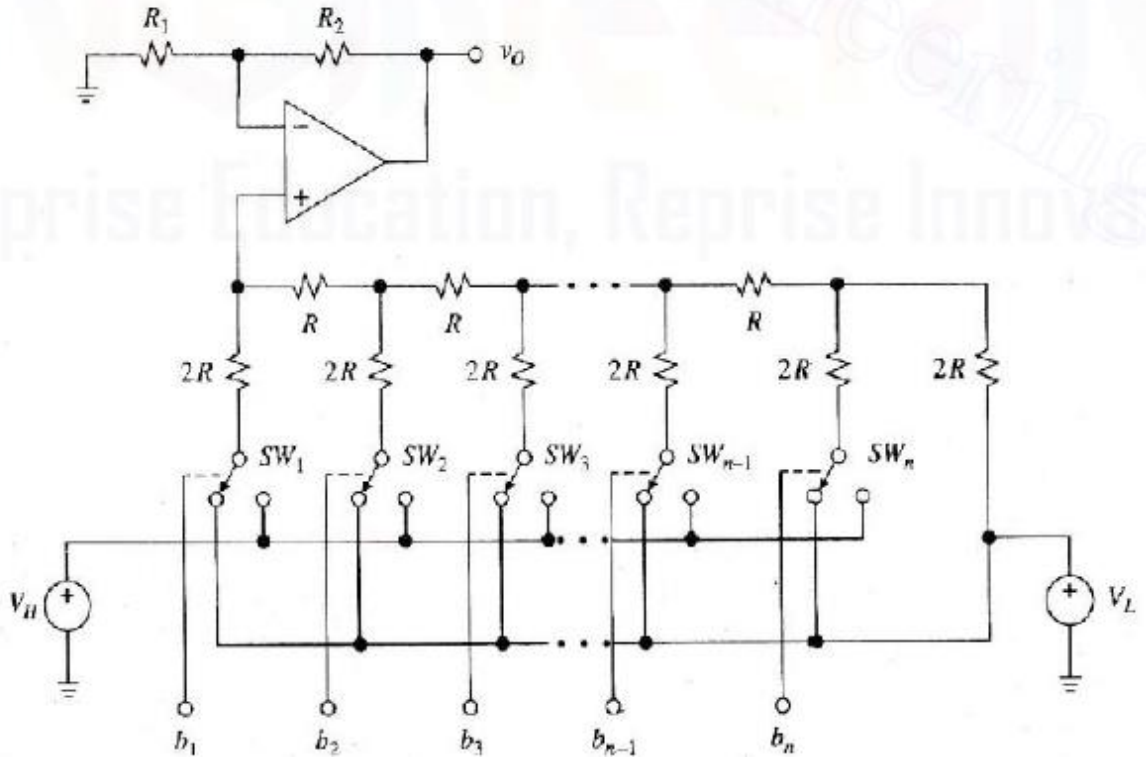


Fig. 4.6 Voltage mode DAC

The diagram also shows a non-inverting amplifier from which the final output is taken. Due to this buffering with a non- inverting amplifier, a scaling factor defined by K = 1 + (R2/R1) results.

Advantages

1. The major advantage of this technique is that it allows us to interpolate between any two voltages, neither of which need not be a zero.

2. More accurate selection and design of resistors R and 2R are possible and simple construction.

3. The binary word length can be easily increased by adding the required number or R-2R sections.

4.7 Switches For DAC

The Switches which connects the digital binary input to the nodes of a D/A converter is an electronic switch. Although switches can be made of using diodes, bipolar junction Transistors, Field Effect transistors or MOSFETs, there are four main configurations used as switches for DACs. They are

i) Switches using overdriven Emitter Followers.

ii) Switches using MOS Transistor- Totem pole MOSFET Switch and CMOS Inverter Switch.

iii) CMOS switch for Multiplying type DACs.

iv) CMOS Transmission gate switches.

These configurations are used to ensure the high speed switching operations for different types of DACs.

✓ Switches using overdriven Emitter Followers:

The bipolar transistors have a negligible resistance when they are operated in saturation. The bipolar transistor operating in saturation region indicates a minimum resistance and thus represents ON condition. When they are operating in cut-off region indicates a maximum resistance and thus represents OFF condition.

The circuit shown here is the arrangement of two transistors connected as emitter followers. A silicon transistor operating in saturation will have an offset voltage of 0.2V dropped across them. To have a zero offset voltage condition, the transistors must be overdriven because the saturation factor becomes negative. The two transistors Q1 (NPN) and Q2 (PNP) acts as a double pole switch. The bases of the transistors are driven by +5.75V and -5.75V.

Case 1:

When VB1 = VB2 = +5.75V, Q1 is in saturation and Q2 is OFF. And VE ≈ 5V
with VBE1 = VBE2 = 0.75V

Case 2:

When VB1 = VB2 = -5.75V, Q2 is in saturation and Q1 is OFF. And VE ≈ - 5V
with VBE1 = VBE2 = 0.75V

Thus the terminal B of the resistor Re is connected to either -5V or +5V depending on the input bit.

✓ Switches using MOS transistor:

i) Totem pole MOSFET Switch:

As shown in the figure, the totem pole MOSFET Switch is connected in series with resistors of R- 2R network. The MOSFET driver is connected to the inverting terminal of the summing op-amp. The complementary outputs *Q* and *Q* drive the gates of the MOSFET M1 and M2 respectively. The SR flip flop holds one bit of digital information of the binary word under conversion. Assuming the negative logic (-5V for logic 1 and +5V for logic 0) the operation is given as two cases.

Case 1:

When the bit line is 1 with S=1 and R=0 makes *Q*=1 and *Q* =0. This makes the transistor M1 ON, thereby connecting the resistor R to reference voltage -VR. The transistor M2 remains in OFF condition.

Case 2:

When the bit line is 0 with S=0 and R=1 makes *Q*=0 and *Q* =1. This makes the transistor M2 ON, thereby connecting the resistor R to Ground. The transistor M1 remains in OFF condition.

ii) CMOS Inverter Switch:

The figure of CMOS inverter is shown here. It consists of a CMOS inverter connected with an opamp acting as a buffer. The buffer drives the resistor R with very low output impedance. Assuming positive logic (+5V for logic 1 and 0V for logic 0), the operation can be explained in two cases.

Case1:

When the complement of the bit line *Q* is low, M1 becomes ON connecting VR to the non- inverting input of the op-amp. This drives the resistor R HIGH.

Case2:

When the complement of the bit line *Q* is high, M2 becomes ON connecting Ground to the non- inverting input of the op-amp. This pulls the resistor R LOW (to ground).

✓ CMOS switch for Multiplying type DACs:

The circuit diagram of CMOS Switch is shown here. The heart of the switching element is formed by transistors M1 and M2. The remaining transistors accept TTL or CMOS compatible logic inputs and provides the anti-phase gate drives for the transistors M1 and M2. The operation for the two cases is as follows.

Case 1:

When the logic input is 1, M1 is ON and M2 is OFF. Thus current IK is diverted to Io bus.

Case 2:

When the logic input is 0, M2 is ON and M1 is OFF. Thus current IK is diverted to Io bus.

✓ CMOS Transmission gate switches:

The disadvantage of using individual NMOS and PMOS transistors are threshold voltage drop (NMOS transistor passing only minimum voltage of VR- VTH and PMOS transistor passing minimum voltage of VTH). This is eliminated by using transmission gates which uses a parallel connection of both NMOS and PMOS. The arrangement shown here can pass voltages from VR to 0V acting as a ideal switch. The following cases explain the operation.

Case 1:

When the bit-line bk is HIGH, both transistors Mn and Mp are ON, offering low resistance over the entire range of bit voltages.

Case 2:

When the bit-line bk is LOW, both the transistors are OFF, and the signal transmission is inhibited (Withdrawn). Thus the NMOS offers low resistance in the lower portion of the signal and PMOS offers low resistance in the upper portion of the signal. As a combination, they offer a low parallel resistance throughout the operating range of voltage. Wide varieties of these kinds of switches were

available. Example: CD4066 and CD4051.

4.8 High Speed Sample and Hold Circuits

Introduction:

Sample-and-hold (S/H) is an important analog building block with many applications,

including analog-to-digital converters (ADCs) and switched-capacitor filters. The function of the S/H circuit is to sample an analog input signal and hold this value over a certain length of time for subsequent processing. Taking advantages of the excellent properties of MOS capacitors and switches, traditional switched capacitor techniques can be used to realize different S/H circuits [1]. The simplest S/H circuit in MOS technology is shown in Figure 1, where *Vin* is the input signal, M1 is an

MOS transistor operating as the sampling switch, Ch is the hold capacitor, ck is the clock signal, and Vout is the resulting sample-and-hold output signal. As depicted by Figure 4. , in the simplest sense, a S/H circuit can be achieved using only one MOS transistor and one capacitor. The operation of this circuit is very straight forward.

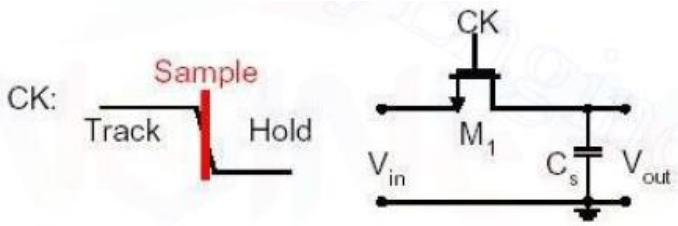


Figure 4.7 Simplest sample-and-hold circuits in MOS technology.

Figure 4, in the simplest sense, a S/H circuit can be achieved using only one MOS transistor and one capacitor. The operation of this circuit is very straightforward. Whenever *ck* is high, the MOS switch is on, which in turn allows *Vout* to track *Vin*. On the other hand, when *ck* is low, the MOS switch is off. During this time, *Ch* will keep *Vout* equal to the value of *Vin* at the instance when *ck* goes low.

Unfortunately, in reality, the performance of this S/H circuit is not as ideal as described above. The two major types of errors occur. They are charge injection and clock feed through, that are associated with this S/H implementation. Three new S/H techniques, all of which try to minimize the errors caused by charge injection and/or clock feed through.

Alternative CMOS Sample-and-Hold Circuits

Three alternative CMOS S/H circuits that are developed with the intention to minimize charge injection and/or clock feed through are

✓ Series Sampling:

The S/H circuit of Figure 4. is classified as parallel sampling because the hold capacitor is in parallel with the signal. In parallel sampling, the input and the output are dc-coupled. On the other hand, the S/H circuit shown in Figure 2 is referred to as series sampling because the hold capacitor is in series with the signal.

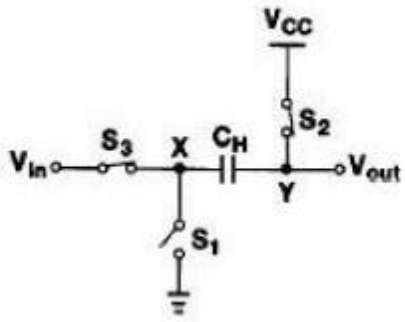


Figure 4.8 Series sampling.

When the circuit is in sample mode, both switches *S2* and *S3* are on, while *S1* is off.
Then,*S2* is turned off first, which means *Vout* is equal to *VCC* (or *VDD* for most circuits) and the voltage drop across *Ch* will be *VCC – Vin*. Subsequently, *S3* is turned off and *S1* is turned on simultaneously. By grounding node *X*, *Vout* is now equal to *VCC –Vin*, and the drop from *VCC* to *VCC – Vin* is equal to the instantaneous value of the input. As a result, this is actually an inverted S/H circuit, which requires inversion of the signal at a later stage. Since the hold capacitor is in series with the signal, series sampling can isolate the common- mode levels of the input and the output. This is one advantage of series sampling over parallel sampling. In addition, unlike parallel sampling, which suffers from signal-dependent charge injection, series sampling does not exhibit such behavior because *S2* is turned off before *S3*. Thus, the fact that the gate-to-source voltage, *VGS*, of *S2* is constant means that charge injection coming from *S2* is also constant (as
opposed to being signal-dependent), which means this error can be easily eliminated through differential operation.

Limitations:

On the other hand, series sampling suffers from the nonlinearity of the parasitic capacitance at node *Y*. This parasitic capacitance introduces distortion to the sample-and hold value, thus mandating that *Ch* be much larger than the parasitic capacitance. On top of this disadvantage, the settling time of the S/H circuit during hold mode is longer for series sampling than for parallel sampling. The reason for this is because the value of *Vout* in series sampling is being reset to *VCC*
(or *VDD*) for every sample, but this is not the case for parallel sampling.

✓ Switched Op-Amp Based Sample-and-Hold Circuit:

This S/H technique takes advantage of the fact that when a MOS transistor is in the saturation region, the channel is pinched off and disconnected from the drain. Therefore, if the hold capacitor is connected to the drain of the MOS transistor, charge injection will only go to the source junction, leaving the drain unaffected. Based on this concept, a switched op- amp (SOP) based S/H circuit, as
shown in Figure 4.9

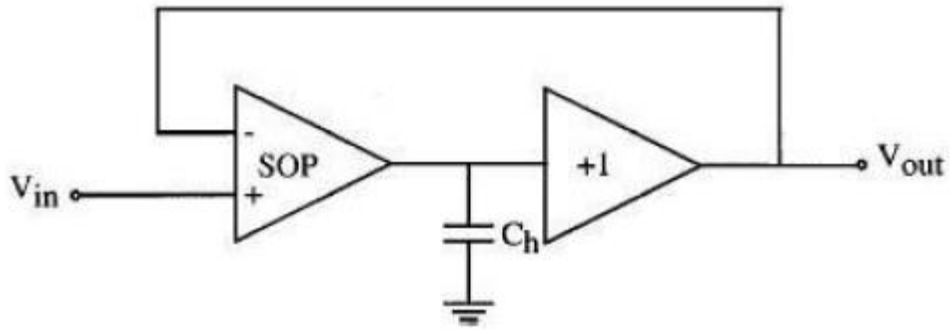


Fig. 4.9 Switched op-amp based sample and hold circuit.

During sample mode, the SOP behaves just like a regular op-amp, in which the value of the output follows the value of the input. During hold mode, the MOS transistors at the output node of the SOP are turned off while they are still operating in saturation, thus preventing any channel charge from flowing into the output of the SOP. In addition, the SOP is shut off and

its output is held at high impedance, allowing the charge on *Ch* to be preserved throughout the hold mode. On

the other hand, the output buffer of this S/H circuit is always operational during sample and hold mode and is always providing the voltage on *Ch* to the output of the S/H circuit. S/H circuits that operate in closed loop configuration can achieve high resolution, but their requirements for high gain circuit block, such as an op-amp, limits the speed of the circuits. As a result, better and faster S/H circuits must be developed.

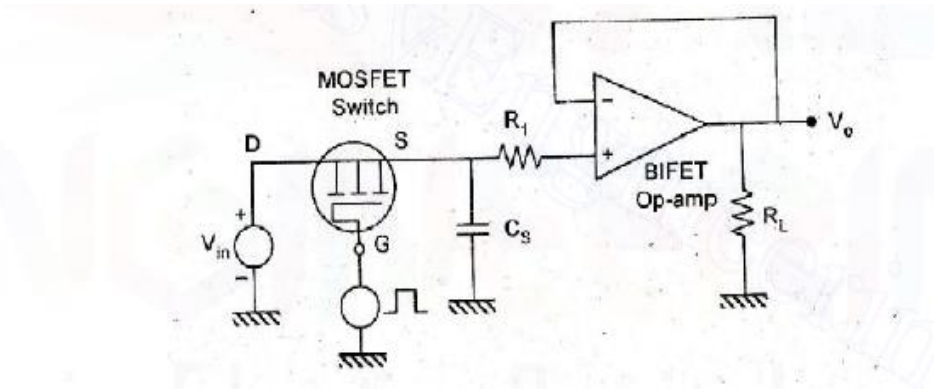


Fig.4.10 High speed Sample and Hold circuit with MOSFET

The above figure shows a sample and holds circuit with MOSFET as Switch acting as a sampling device and also consists of a holding capacitor Cs to store the sample values until the next sample comes in. This is a high speed circuit as it is apparent that CMOS switch has a very negligible propagation delay.

Three S/H circuits to reduce error:

- series sampling,
- SOP based S/H circuit,
- bottom plate S/H circuit with bootstrapped switch

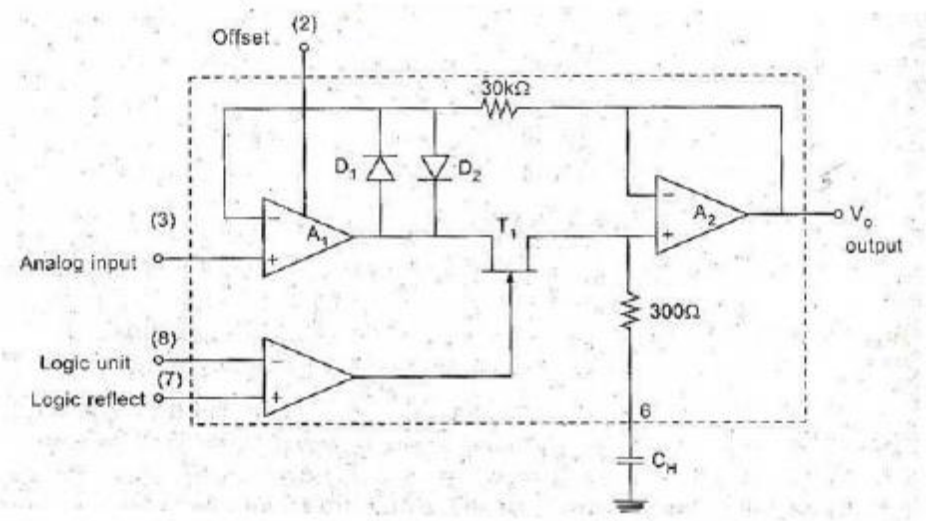


Fig.4.11 LF 398 IC- Functional Diagram

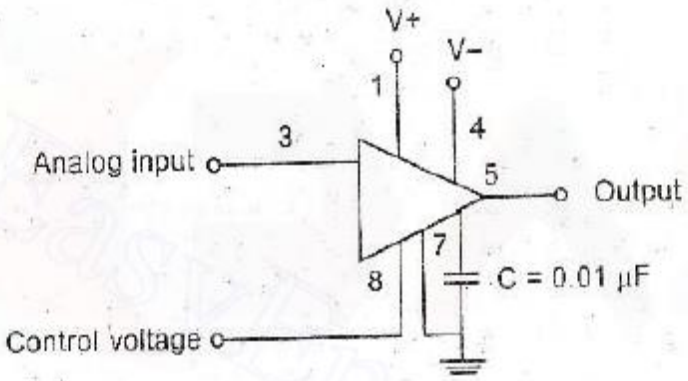


Fig.4.12 Connections of S&H IC

4.9 A to D Converter- Specifications

Like DAC, ADCs are also having many important specifications. Some of them are Resolution, Quantization error, Conversion time, Analog error, Linearity error, DNL error, INL error & Input voltage range.

✓ Resolution:

The resolution refers to the finest minimum change in the signal which is accepted for conversion, and it is decided with respect to number of bits. It is given as 1/2n, where 'n' is the number of bits in the digital output word. As it is clear, that the resolution can be improved by

increasing the number of bits or the number of bits representing the given analog input voltage. Resolution can also be defined as the ratio of change in the value of input voltage Vi, needed to change the digital output by 1 LSB. It is given as

Resolution = ViFS / (2n – 1)

Where 'ViFS' is the full-scale input voltage.

'n' is the number of output bits.

✓ Quantization error:

If the binary output bit combination is such that for all the values of input voltage Vi between any two voltage levels, there is a unavoidable uncertainty about the exact value of Vi when the output is a particular binary combination. This uncertainty is termed as quantization error. Its value is ± (1/2) LSB. And it is given as,

QE = ViFS / 2(2n – 1)

Where 'ViFS' is the full-scale input voltage

'n' is the number of output bits.

Maximum the number of bits selected, finer the resolution and smaller the quantization error.

✓ Conversion Time:

It is defined as the total time required for an A/D converter to convert an analog signal to digital output. It depends on the conversion technique and propagation delay of the circuit components.

✓ Analog error:

An error occurring due to the variations in DC switching point of the comparator, resistors, reference voltage source, ripples and noises introduced by the circuit components is termed as Analog error.

✓ Linearity Error:

It is defined as the measure of variation in voltage step size. It indicates the difference between the transitions for a minimum step of input voltage change. This is normally specified as fraction of LSB.

✓ Differential Non-Linearity(DNL) Error:

The analog input levels that trigger any two successive output codes should differ by 1 LSB. Any deviation from this 1 LSB value is called as DNL error.

✓ Integral Non-Linearity (INL) Error:

The deviation of characteristics of an ADC due to missing codes causes INL error. The maximum deviation of the code from its ideal value after nulling the offset and gain errors is called as Integral Non-Linearity Error.

✓ Input Voltage Range:

It is the range of voltage that an A/D converter can accept as its input without causing any overflow in its digital output.

✓ Analog Switches

There were two types of analog switches. Series and Shunt switch. The Switch operation is shown for both the cases VGS=0 VGS= VGs (off)

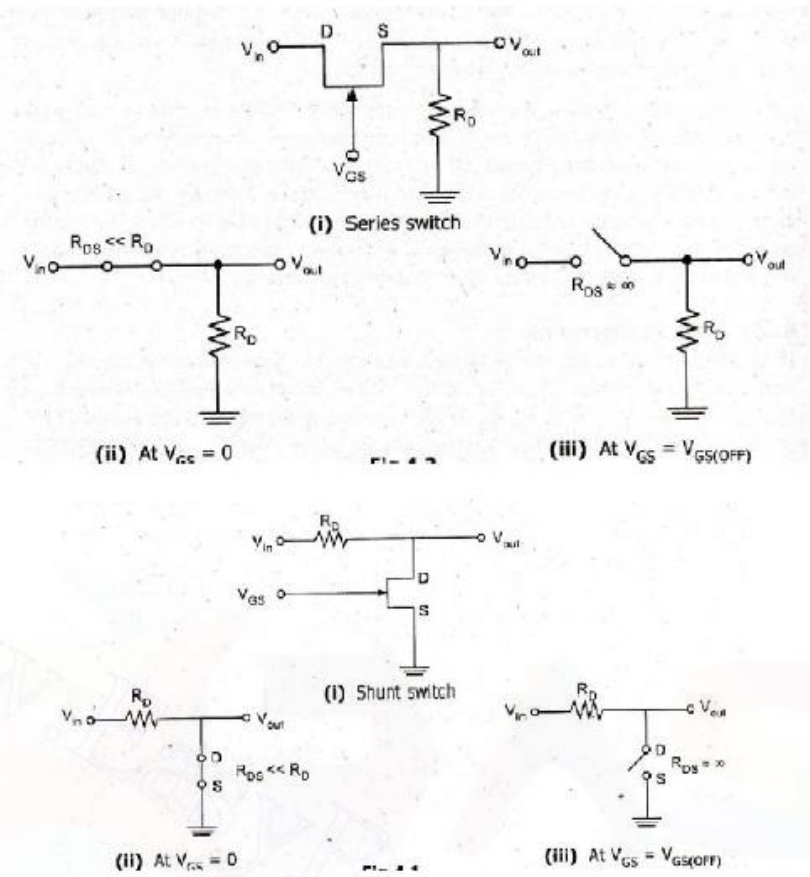


Fig 4.13 Series and shunt Analog switches

4.10 Direct-conversion ADC/Flash type ADC:

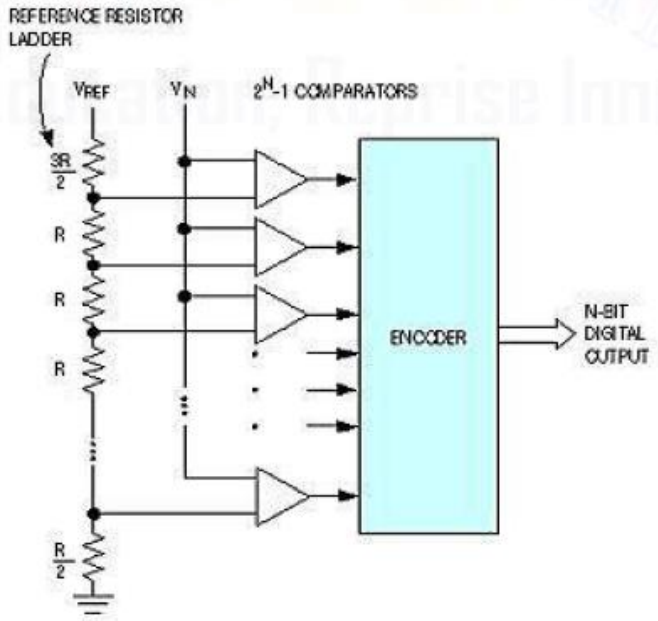


Fig.4.14 Flash ADC

This process is extremely fast with a sampling rate of up to 1 GHz. The resolution is however, limited because of the large number of comparators and reference voltages required. The input signal is fed simultaneously to all comparators. A priority encoder then generates a digital output that corresponds with the highest activated comparator.

4.12 Successive-approximation ADCs

Successive-approximation ADC is a conversion technique based on a successive approximation register (SAR). This is also called bit-weighing conversion that employs a comparator to weigh the applied input voltage against the output of an N-bit digital-to-analog converter (DAC). The final result is obtained as a sum of N weighting steps, in which each step is a single-bit conversion using the DAC output as a reference. SAR converters sample at rates up to 1Mbps, requires a low supply current, and the cheapest in terms of production cost. A successive-approximation ADC uses a comparator to reject ranges of voltages, eventually settling on a final voltage range. Successive approximation works by constantly comparing the input voltage to the output of an internal digital to analog converter (DAC, fed by the current value of the approximation) until the best approximation is achieved.

At each step in this process, a binary value of the approximation is stored in a successive approximation register (SAR). The SAR uses a reference voltage (which is the largest signal the ADC is to convert) for comparisons. For example if the input voltage is 60 V and the reference voltage is 100 V, in the 1st clock cycle, 60 V is compared to 50 V (the reference, divided by two. This is the voltage at the output of the internal DAC when the input is a '1' followed by zeros), and the voltage from the comparator is positive (or '1') (because 60 V is greater than 50 V). At this point the first binary digit (MSB) is set to a '1'. In the 2nd clock cycle the input voltage is compared to 75 V (being halfway between 100 and 50 V: This is the output of the internal DAC when its input is '11' followed by zeros) because 60 V is less than 75 V, the comparator output is now negative (or '0'). The second binary digit is therefore set to a '0'. In the 3rd clock cycle, the input voltage is compared with 62.5 V (halfway between 50 V and 75 V: This is the output of the internal DAC when its input is '101' followed by zeros). The output of the comparator is negative or '0' (because 60 V is less than 62.5 V) so the third binary digit is set to a 0. The fourth clock cycle

similarly results in the fourth digit being a '1' (60 V is greater than 56.25 V, the DAC output for

'1001' followed by zeros). The result of this would be in the binary form 1001. This is also called *bit-weighting conversion*, and is similar to a binary. The analogue value is rounded to the nearest binary value below, meaning this converter type is mid-rise (see above). Because the approximations are successive (not simultaneous), the

conversion takes one clock-cycle for each bit of resolution desired.

The clock frequency must be equal to the sampling frequency multiplied by the number of bits of resolution desired. For example, to sample audio at 44.1 kHz with 32 bit resolution, a clock frequency of over 1.4 MHz would be required.

ADCs of this type have good resolutions and quite wide ranges. They are more complex than some other designs.

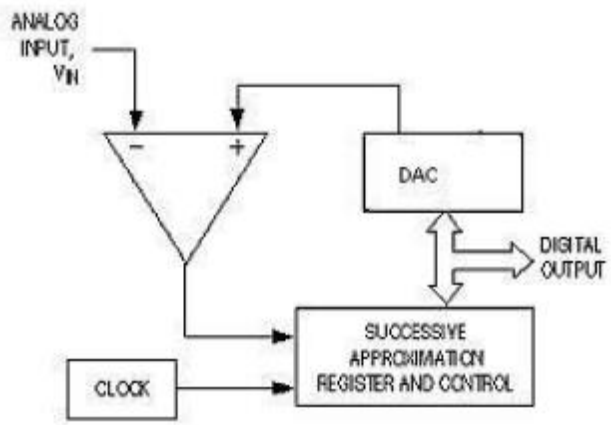


Fig.4.15 Successive approximation ADC

4.13 Dual slope ADC (Integrating ADCs)

In an integrating ADC, a current, proportional to the input voltage, charges a capacitor for a fixed time interval T charge. At the end of this interval, the device resets its counter and applies an opposite-polarity negative reference voltage to the integrator input. Because of this, the capacitor is discharged by a constant current until the integrator output voltage zero again. The T discharge interval is proportional to the input voltage level and the resultant final count provides the digital output, corresponding to the input signal. This type of ADCs is extremely slow devices with low input bandwidths. Their advantage, however, is their ability to reject high-frequency noise and AC line noise such as 50Hz or 60Hz. This makes them useful in

noisy industrial environments and typical application is in multi-meters. An integrating ADC (also dual-slope or multi-slope ADC) applies the unknown input voltage to the input of an

integrator and allows the voltage to ramp for a fixed time period (the run-up period). Then a known reference voltage of opposite polarity is applied to the
integrator and is allowed to ramp until the integrator output returns to zero (the run-down period). The input voltage is computed as a function of the reference voltage, the constant run-up time period, and the measured run-down time period.
The run-down time measurement is usually made in units of the converter's clock, so longer integration times allow for higher resolutions. Likewise, the speed of the converter can be improved by sacrificing resolution.
Use: Converters of this type (or variations on the concept) are used in most digital voltmeters for their linearity and flexibility.

4.14 A/D Using Voltage To Time Conversion:

The Block diagram shows the basic voltage to time conversion type of A to D converter. Here the cycles of variable frequency source are counted for a fixed period. It is possible to make an A/D converter by counting the cycles of a fixed-frequency source for a variable period. For this, the analog voltage required to be converted to a proportional time period. As shown in the diagram a negative reference voltage -VR is applied to an integrator, whose output is connected to the inverting input of the comparator. The output of the comparator is at 1 as long as the output of the integrator Vo is less than Va.

At t = T, Vc goes low and switch S remains open. When VEN goes high, the switch S is closed, thereby discharging the capacitor. Also the NAND gate is disabled. The waveforms are shown here.

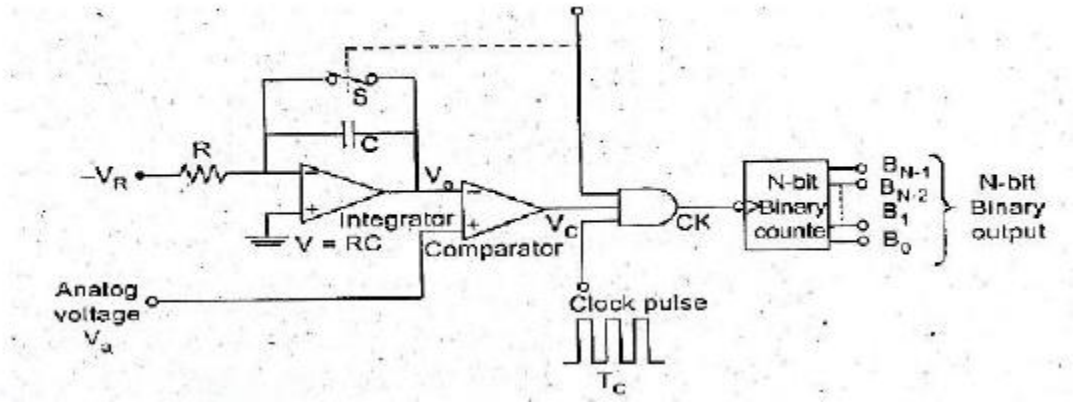


Fig. 4.16 A/D Using Voltage To Time Conversion:

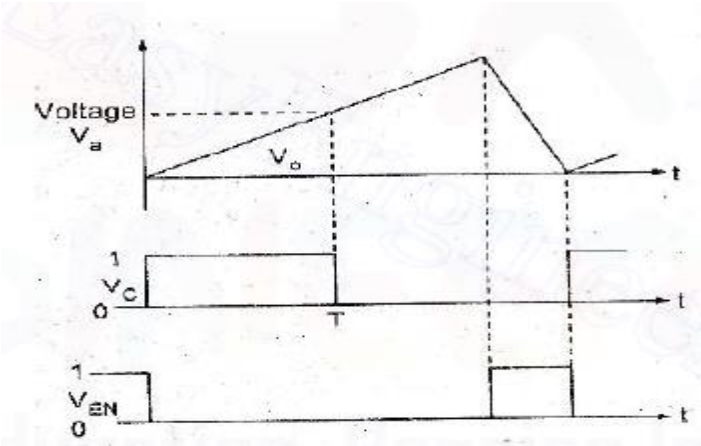


Fig.4.17 Conversion process

4.15 Sigma-delta ADCs/ Over sampling Converters:

It consists of 2 main parts - modulator and digital filter. The modulator includes an integrator and a comparator with a feedback loop that contains a 1-bit DAC. The modulator oversamples the input signal, converting it to a serial bit stream with a frequency much higher than the required sampling rate. This is then transformed by the output filter to a sequence of parallel digital words at the sampling rate. The characteristics of sigma-delta converters are high resolution, high accuracy,
Low noise and low cost.
Typical applications are for speech and audio.
A **Sigma-Delta ADC** (also known as a Delta-Sigma ADC) oversamples the desired signal by a large factor and filters the desired signal band. Generally a smaller number of bits than required are converted using a Flash ADC after the Filter. The resulting signal, along with the error generated by the discrete levels of the Flash, is fed back and subtracted from the input to the filter. This negative feedback has the effect of noise shaping the error due to the Flash so that it does not appear in the desired signal frequencies.
A digital filter (decimation filter) follows the ADC which reduces the sampling rate, filters off unwanted noise signal and increases the resolution of the output. (sigma-delta modulation, also called delta-sigma modulation)

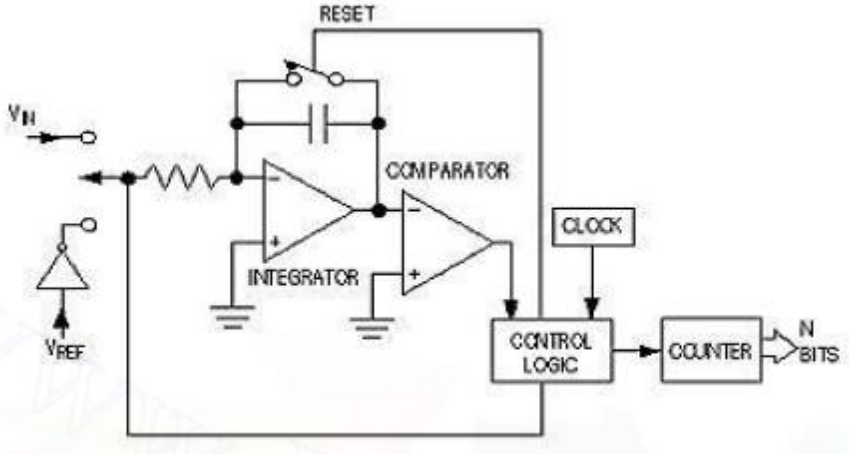


Fig 4.18 Sigma-delta ADCs/ Over sampling Converters: