JEPPIAAR INSTITUTE OF TECHNOLOGY

"Self-Belief | Self Discipline | Self Respect"

DEPARTMENT

OF

ELECTRONICS AND COMMUNICATION ENGINEERING

LECTURE NOTES

EC8453 – LINEAR INTEGRATED CIRCUITS

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Prepared by

Dr. S. Kamatchi

Associate Professor/ECE

UNIT II APPLICATIONS OF OPERATIONAL AMPLIFIERS 9

Sign Changer, Scale Changer, Phase Shift Circuits, Voltage Follower,V-to-I and I-to-VConverters, adder, subtractor, Instrumentation amplifier, Integrator, Differentiator, Logarithmic amplifier, Antilogarithmic amplifier, Comparators, Schmitt trigger, Precision rectifier, peak detector, clipper and clamper, Low-pass, high-pass and band-pass Butterworth filters.

2.1 Sign Changer (Phase Inverter)

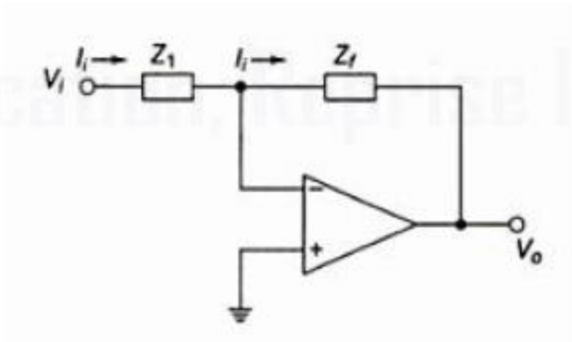


Fig 2.1 Basic inverting configuration

The basic inverting amplifier configuration using an op-amp with input impedance Z1 and feedback impedance Z_f . If the impedance Z1 and Z f are equal in magnitude and phase, then the closed loop voltage gain is -1, and the input signal will undergo a 180° phase shift at the output. Hence, such circuit is also called phase inverter. If two such amplifiers are connected in cascade, then the output from the second stage is the same as the input signal without any change of sign. Hence, the outputs from the two stages are equal in magnitude but opposite in phase and such a system is an excellent paraphase amplifier.

2.2 Scale Changer:

Referring the above diagram, if the ratio Zf / Z1 = k, a real constant, then the closed loop gain is – k, and the input voltage is multiplied by a factor –k and the scaled output is available at the output. Usually, in such applications, Zf and Z1 are selected as precision resistors for obtaining precise and scaled value of input voltage.

2.3 Phase Shift Circuits

The phase shift circuits produce phase shifts that depend on the frequency and maintain a constant gain. These circuits are also called constant-delay filters or all-pass filters. That constant delay refers to the fact the time difference between input and output remains constant when frequency is changed over a range of operating frequencies. This is called all-pass because normally a constant gain is maintained for all the frequencies within the operating range. The two types of circuits, for lagging phase angles and leading phase angles.

Phase-lag circuit:

Phase log circuit is constructed using an op-amp, connected in both inverting and non inverting modes. To analyze the circuit operation, it is assumed that the input voltage v1 drives a simple inverting amplifier with inverting input applied at(-)terminal of op-amp and a non inverting amplifier with a low-pass filter. It is also assumed that inverting gain is -1 and non-inverting gain after the low-pass circuit is $1+\frac{R_f}{R_1} = 1+1 = 2$ Since R f=R1.

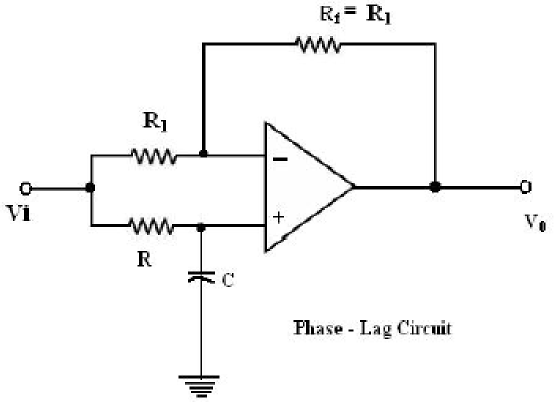


Fig. 2.2 Phase lag circuit

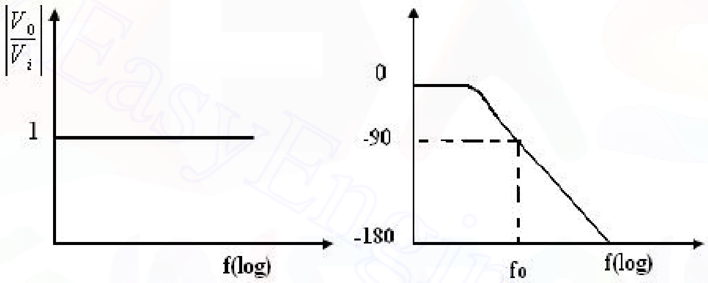


Fig 2.3 Bode plot of phase lag circuit

For the circuit fig 2.2, it can be written as

$$V_O(jw) = -V_i(jw)\left(-1 + \frac{2}{1+jwRC}\right)$$

and the relationship between output and input can be expressed by

$$\frac{V_O(jw)}{V_i(jw)} = \frac{(1-jwRC)}{(1+jwRC)}$$

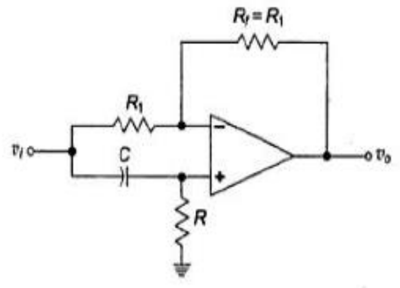
The relationship is complex as defined above equation and it shows that it has both magnitude and phase. Since the numerator and denominator are complex conjugates, their magnitudes are identical and the overall phase angle equals the angle of numerator less the angle of the denominator.

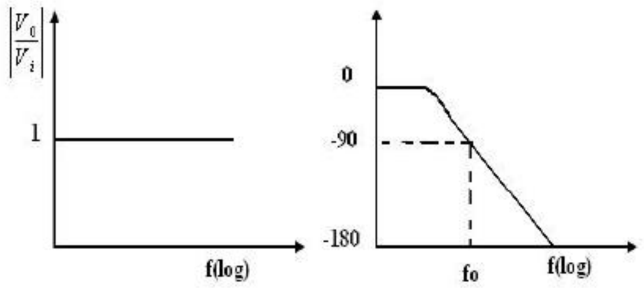
$$\theta = -2\ \tan^{-1} RC\omega$$

Phases-lead circuit:

$$\frac{V_O(jw)}{V_i(jw)} = -\frac{(1-jwRC)}{(1+jwRC)}$$

$$\theta = 180° - 2\ \tan^{-1} RC\omega$$





Figs 2.4 Phase lead circuit **Fig 2.5 Bode plot of Phase lead circuit**

2.4 Voltage follower:

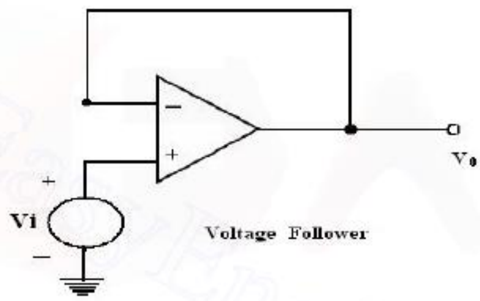


Fig 2.6 Voltage follower

If R1=∞ and R_f =0 in the non inverting amplifier configuration. The amplifier act as a unity-gain amplifier or voltage follower. The circuit consists of an op-amp and a wire connecting the output voltage to the input, i.e. the output voltage is equal to the input voltage, both in magnitude and phase. V0=Vi. Since the output voltage of the circuit follows the input voltage, the circuit is called voltage follower. It offers very
high input impedance of the order of MΩ and very low output impedance.
Therefore, this circuit draws negligible current from the source. Thus, the voltage follower can be used as a buffer between a high impedance source and a low impedance load for impedance matching applications.

2.5 Voltage to Current Converter with floating loads (V/I):

Voltage to current converter in which load resistor RL is floating (not connected to ground). V_{in} is applied to the non- inverting input terminal, and the feedback voltage across R1 devices the inverting input terminal. This circuit is also called as a current – series negative feedback amplifier. Because the feedback voltage across R1 (applied Non-inverting terminal) depends on the output current i0 and is in series with the input difference voltage Vid.

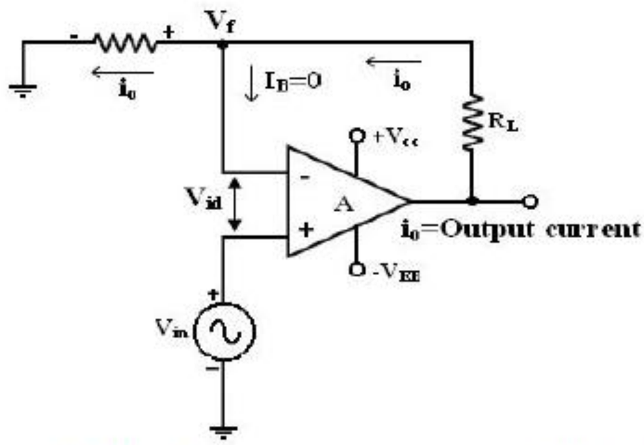


Fig. 2.7 Voltage to Current Converter with floating loads (V/I):

Writing KVL for the input loop,

Voltage $V_{id} = V_f$ and $I_B = 0$, $V_i = R_L i_o$ where $i_o = \frac{V_i}{R_L}$

From the fig input voltage Vin is converted into output current of Vin/RL [Vin -> i0].

In other words, input volt appears across R1. If RL is a precision resistor, the output current (i0 = Vin/R1) will be precisely fixed.

Applications:

1. Low voltage ac and dc voltmeters
2. Diode match finders
3. LED and Zener diode testers.

Voltage – to current converter with Grounded load:

This is the other type V – I converter, in which one terminal of the load is connected to ground.

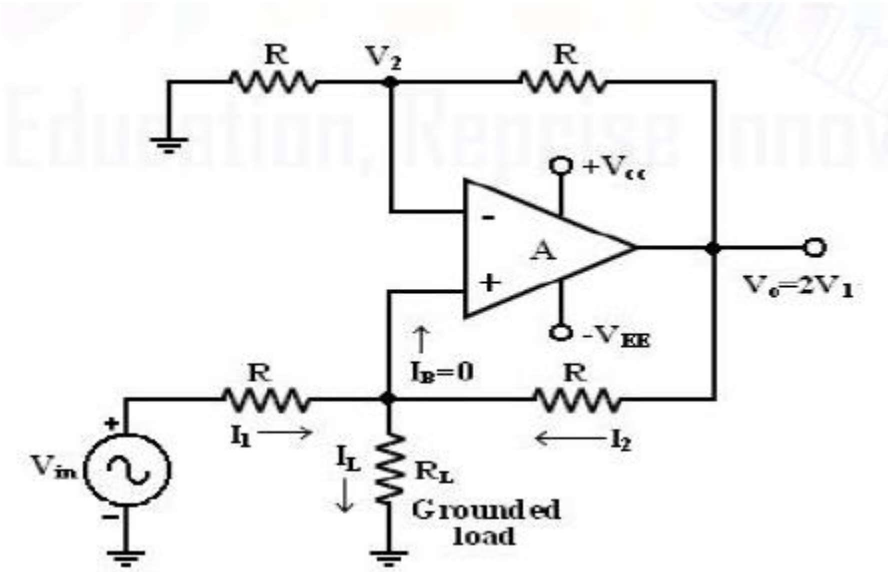


Fig 2.8 V – I converter with grounded load

Analysis of the circuit:

The analysis of the circuit can be done by following 2 steps.

1. To determine the voltage V1 at the non-inverting (+) terminals and

2. To establish relationship between V1 and the load current IL. Applying KCL at node a,

$$R = R_f$$

$$I_1 + I_2 = I_L$$

$$(V_i + V_a)/R + (V_o - V_a)/R = I_L$$

$$V_o = (V_i + V_o - I_L R)/2 \text{ and gain } = 1 + R/R = 2.$$

$$\therefore V_i = I_L R \;;\; I_L = V_i/R$$

Current to Voltage Converter (I –V):

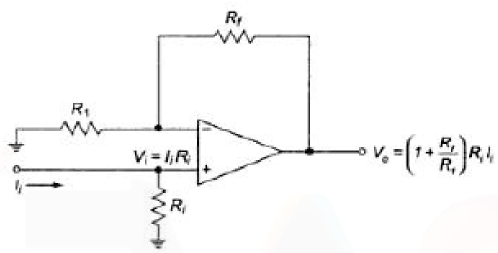


Fig. 2.9 Non inverting current to voltage convertor

Open – loop gain A of the op-amp is very large. Input impedance of the op amp is very high.

Sensitivity of the I – V converter:

1. The output voltage V0 = -RF Iin.

2. Hence the gain of this converter is equal to -RF. The magnitude of the gain (i.e.) is called as sensitivity of I to V converter.

3. The amount of change in output volt $\Delta V0$ for a given change in the input current ΔI_{in} is decide by the sensitivity of I-V converter.

4. By keeping RF variable, it is possible to vary the sensitivity as per the requirements.

Applications of V-I converter with Floating Load:

1. Diode Match finder:

In some applications, it is necessary to have matched diodes with equal voltage drops at a particular value of diode current. The circuit can be used in finding matched diodes and is obtained from fig (V-I converter with floating load) by replacing RL with a diode. When the switch is in position 1: (Diode Match Finder) Rectifier diode (IN 4001) is placed in the f/b loop, the current through this loop is set by input voltage Vin and Resistor R1. For Vin = 1V and R1 = 100Ω, the current through this I0 = Vin/R1 = 1/100 = 10mA. As long as V0 and R1 constant, I0 will be constant. The Voltage drop across the diode can be found either by measuring the volt across it or o/p voltage.

The output voltage is equal to (Vin +VD) V0= Vin + VD.

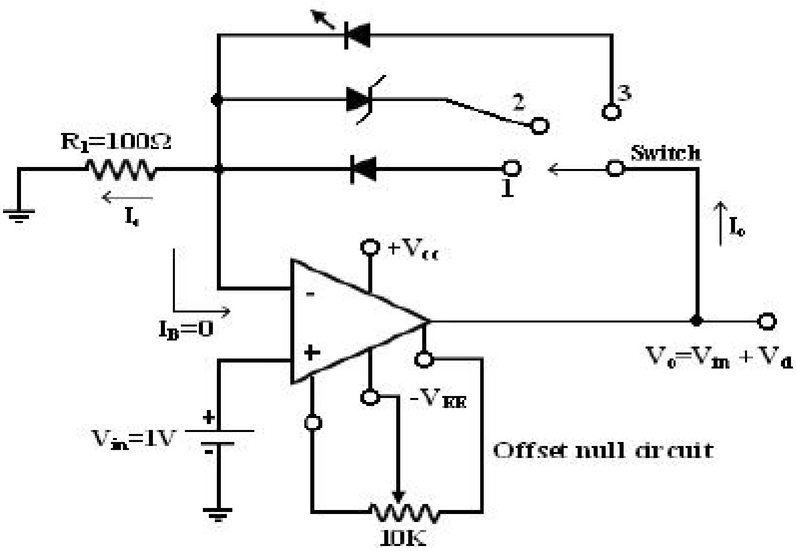


Fig. 2.10 Diode Match finder:

To avoid an error in output voltage the op-amp should be initially nulled. Thus the matched diodes can be found by connecting diodes one after another in the feedback path and measuring voltage across them.

2. Zener diode Tester:

(When the switch position 2) when the switch is in position 2, the circuit becomes a Zener diode tester. The circuit can be used to find the breakdown voltage of Zener diodes. The Zener current is set at a constant value by Vin and R1. If this current is larger than the knee current (I_{ZK}) of the Zener, the Zener blocks (V_Z) volts. For Ex: I_{ZK} = 1mA , V_Z = 6.2V, Vin = 1V, R_1 = 100Ω Since the current through the Zener is , I0 = Vin/R_1 = 1/100 =10mA > I_{ZK} the voltage across the Zener will be approximately equal to 6.2V.

3. When the switch is in position 3: (LED)

The circuit becomes a LED when the switch is in position 3. LED current is set at a constant value by Vin and R1. LEDs can be tested for brightness one after another at this current. Matched LEDs with equal brightness at a specific value of current are useful as indicates and display devices in digital applications.

Applications of I – V Converter:

One of the most common uses of the current to voltage converter is

1. Digital to analog Converter (DAC)
2. Sensing current through Photo detector. Such as photo cell, photo diodes and photovoltaic cells. Photoconductive devices produce a current that is proportional to an incident energy or light (i.e). It can be used to detect the light.

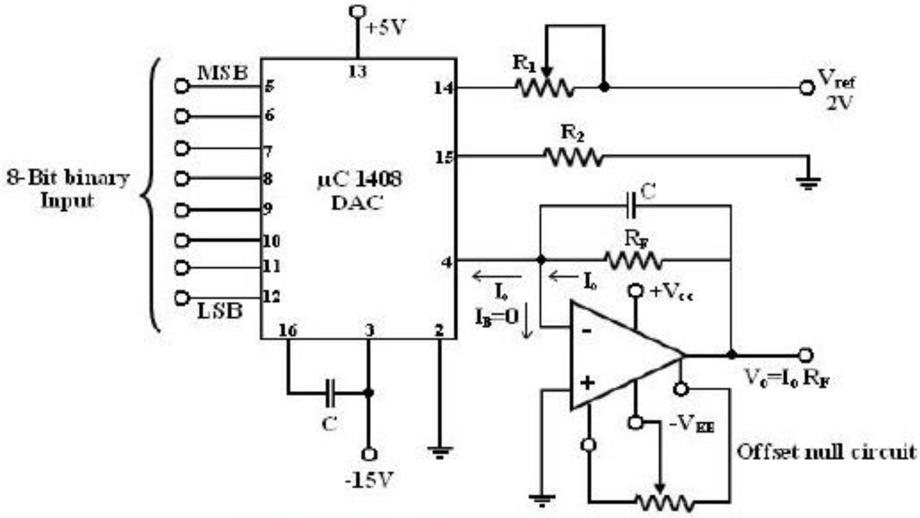


Fig. 2.11 I – V Converter DAC

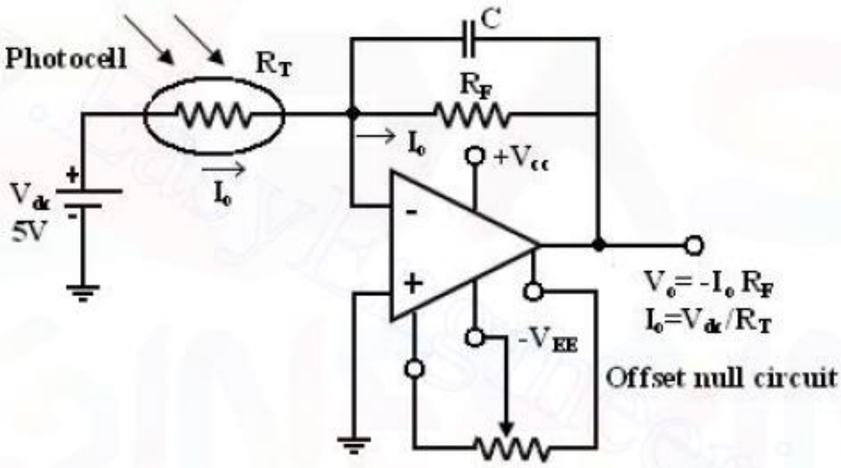


Fig. 2.12 Photo cell detector

Photocells, photodiodes, photovoltaic cells give an output current that depends on the intensity of light and independent of the load. The current through these devices can be converted to voltage by I – V converter and it can be used as a measure of the amount of light. In this fig photocell is connected to the I – V Converter. Photocell is a passive transducer it requires an external dc voltage (Vdc). The dc voltage can be eliminated if a photovoltaic cell is used instead of a photocell. The Photovoltaic Cell is a semiconductor device that converts the radiant energy to electrical power. It is a self-generating circuit because it does not require dc voltage externally.

Ex of Photovoltaic Cell: used in space applications and watches.

2.6 Adder:

Op-amp may be used to design a circuit whose output is the sum of several input signals. Such a circuit is called a summing amplifier or a summer or adder. An inverting summer or a non-inverting summer may be discussed now.

Inverting Summing Amplifier:

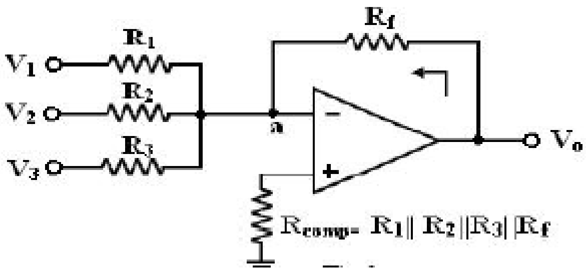


Fig. 2.13 inverting summer

A typical summing amplifier with three input voltages V1, V2 and V3 three input resistors R1, R2, R3 and a feedback resistor Rf is shown in figure 2.

The following analysis is carried out assuming that the op-amp is an ideal one, AOL= ∞. Since the input bias current is assumed to be zero, there is no voltage drop across the resistor Rcomp and hence the non-inverting input terminal is at ground potential.

$I= V_1/R_1+V_2/R_2.....+V_n/R_n$;

$V_o= - R_f\, I=R_f/R(V_1+V_2+....V_n)$.

To find Rcomp, make all inputs V1 = V2 = V3 = 0.

So the effective input resistance Ri = R1 || R2 || R3.

Therefore, Rcomp = Ri || Rf = R1 || R2 || R3 || R,f.

Non-Inverting Summing Amplifier:

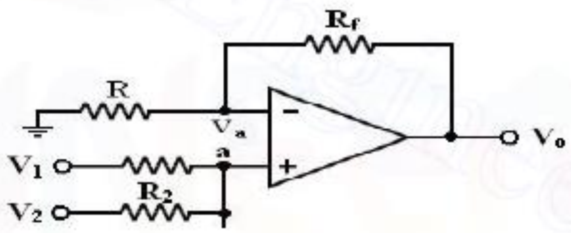


Fig.2.14 Non inverting summer

A summer that gives a non-inverted sum is the non-inverting summing amplifier of figure Let the voltage at the (-) input terminal be Va. which is a non-inverting weighted sum of inputs. Let R1 = R2 = R3 = R = Rf/2, then Vo = V1+V2+V3

2.7 Subtractor:

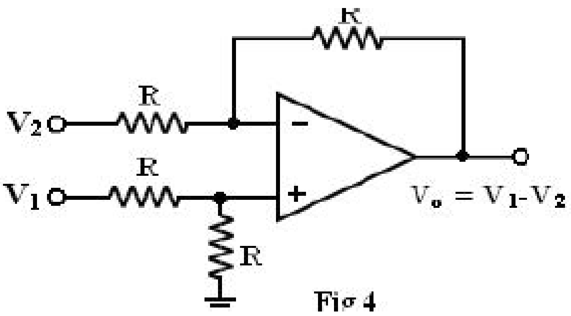


Fig. 2.15 Subtractor

A basic differential amplifier can be used as a subtractor as shown in the above figure. If all resistors are equal in value, then the output voltage can be derived by using superposition principle. To find the output V01 due to V1 alone, make V2 = 0.

Then the circuit of figure as shown in the above becomes a non-inverting amplifier having input voltage V1/2 at the non-inverting input terminal and the output becomes

$V_{01} = V_1/2(1+R/R)$ = V1 when all resistances are R in the circuit.

Similarly the output V02 due to V2 alone (with V1 grounded) can be written simply for an inverting amplifier as

$V_{02} = -V_2$

Thus the output voltage Vo due to both the inputs can be written as

V_0 =V01 - V02 =V1 - V2

Adder/Subtractor:

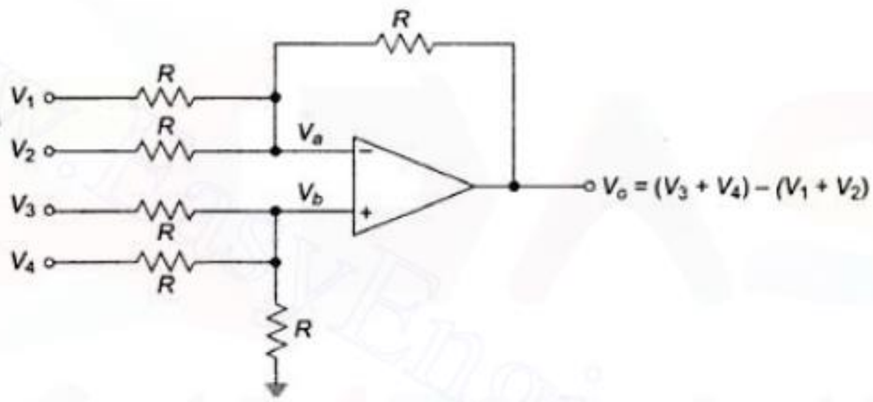


Fig. 2.16 Adder-Subtractor

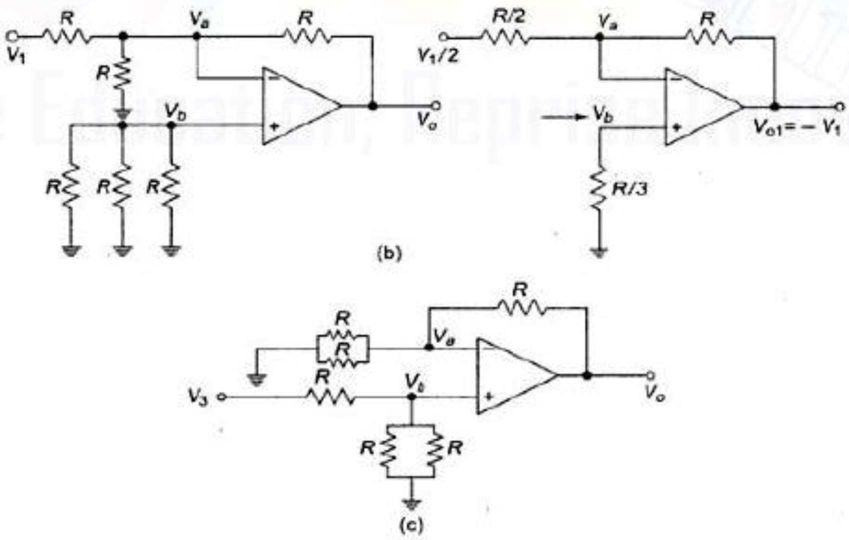


Fig. 2.17 (b) equivalent circuit for $V_2=V_3=V_4=0$ and (c) for $V_1=V_2=V_4=0$

It is possible to perform addition and subtraction simultaneously with a single op-amp using the circuit shown in figure 2.16.

The output voltage Vo can be obtained by using superposition theorem. To find output voltage V01 due to V1 alone, make all other input voltages V2, V3 and V4 equal to zero. The simplified circuit is shown in figure 2.17. This is the circuit of an inverting amplifier and its output voltage is, $V_{01}= -R/(R/2) * V_1/2= - V_1$ by Thevenin‘s equivalent circuit at inverting input terminal). Similarly, the output voltage V02 due to V2 alone is,

$V_{02} = -V_2$

Now, the output voltage V03 due to the input voltage signal V3 alone applied at the (+) input terminal can be found by setting V1, V2 and V4 equal to zero.

$V_{03} = V_3$

The circuit now becomes a non-inverting amplifier as shown in fig.(c).

So, the output voltage V03 due to V3 alone is

$V03 = V3$

Similarly, it can be shown that the output voltage V04 due to V4 alone is

$V04 = V4$

Thus, the output voltage Vo due to all four input voltages is given by

$Vo = V01 = V02 = V03 = V04$

$Vo = -V1 - V2 + V3 + V4$

$Vo = (V3 + V4) – (V1 + V2)$

So, the circuit is an adder-subtractor.

2.8 Instrumentation Amplifier:

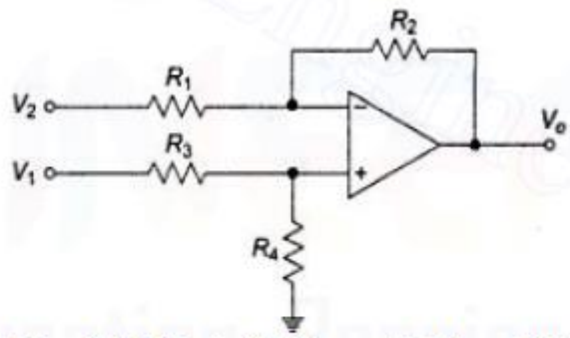


Fig. 2.18 Basic Differential Amplifier

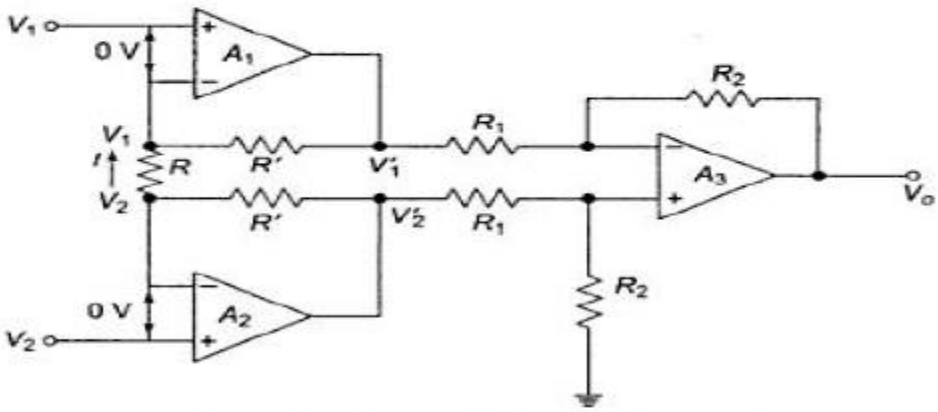


Fig. 2.19 Instrumentation Amplifier

Current flowing in resistor R is I= $(V_1-V_2)/R$ and it flow through R' in the direction shown, Voltage

at non-inverting terminal op-amp A3 is $R_2V_1'/(R_1+R_2)$. By superposition theorem,

$V_o= (R_2/R_1)V_1+(1+R_2/R_1)(R_2V_2/(R_1+R_2)=R_2/R_1(V_1'-V_2');$

$V_1'= R'I+V_1=R'/R(V_1-V_2)+V_1$

$V_2'= R'I+V_1=R'/R(V_1-V_2)+V_2;$

$V0= (R_2/R_1)[(2R'/R(V_2-V1)+ (V_2-V1)]= (R_2/R_1)[(1+2R'/R)(V_2-V1)$

In a number of industrial and consumer applications, one is required to measure and control physical quantities. Some typical examples are measurement and control of temperature, humidity, light intensity, water flow etc. these physical quantities are usually measured with help of transducers. The output of transducer has to be amplified so that it can drive the indicator or display system. This function is performed by an instrumentation amplifier. The important features of an instrumentation amplifier are

1. High gain accuracy
2. High CMRR

3. High gain stability with low temperature coefficient
4. Low output impedance

There are specially designed op-amps such as μA725 to meet the above stated requirements of a good instrumentation amplifier. Monolithic (single chip) instrumentation amplifier are also available commercially such as AD521, AD524, AD620, AD624 by Analog Devices, LM363.XX (XX -->10,100,500) by National Semiconductor and INA101, 104, 3626, 3629 by Burr Brown. In the circuit of figure 6(a), source V1 sees an input impedance = R3+R4 (=101K) and the impedance seen by source V2 is only R1 (1K). This low impedance may load the signal source

heavily. Therefore, high resistance buffer is used preceding each input to avoid this loading effect as shown in figure

The op-amp A1 and A2 have differential input voltage as zero. For V1=V2, that is, under common mode condition, the voltage across R will be zero. As no current flows through R and R‘ the non-inverting amplifier. A1 acts as voltage follower, so its output V2‘=V2. Similarly op-amp A2 acts as voltage follower having output V1‘=V1. However, if V1≠V2, current flows in R and R‘, and (V2‘-V1‘)>(V2- V1). Therefore, this circuit has differential gain and CMRR more compared to the single opamp circuit of figure 2.10. The difference gain of this instrumentation amplifier R, however should never be made zero, as this will make the gain infinity. To avoid such a situation, in a practical circuit, a fixed resistance in series with a potentiometer is used in place of R. Figure (c) shows a differential instrumentation amplifier using Transducer Bridge. The circuit uses a resistive transducer whose resistance changes as a function of the physical quantity to be measured. The bridge is initially balanced by a dc supply voltage Vdc so that V1=V2. As the physical quantity changes, the resistance RT of the transducer also changes, causing an unbalance in the bridge (V1≠V2). This differential voltage now gets amplified by the three opamp differential instrumentation amplifier.

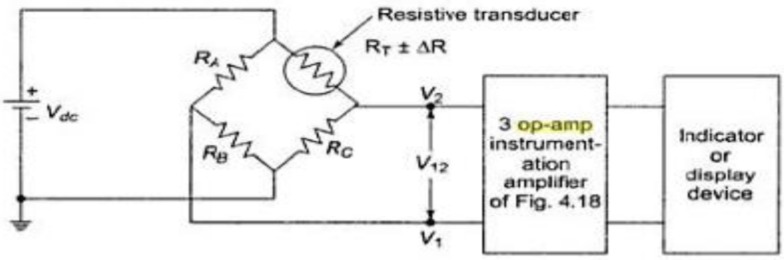


Fig.2.20 Instrumentation bridge using transducer Bridge

$R_B(V_{dc})/(R_B+R_A)= R_C V_{dc}/(R_C+R_T)$

Applications of instrumentation amplifier with the transducer bridge,

- temperature indicator,
- temperature controller and
- light intensity meter .

2.9 Integrator:

A circuit in which the output voltage waveform is the integral of the input voltage waveform is the integrator or Integration Amplifier. Such a circuit is obtained by using a basic inverting amplifier configuration if the feedback resistor RF is replaced by a capacitor CF. The expression for the output voltage V0 can be obtained by KVL eqn. at node V2.

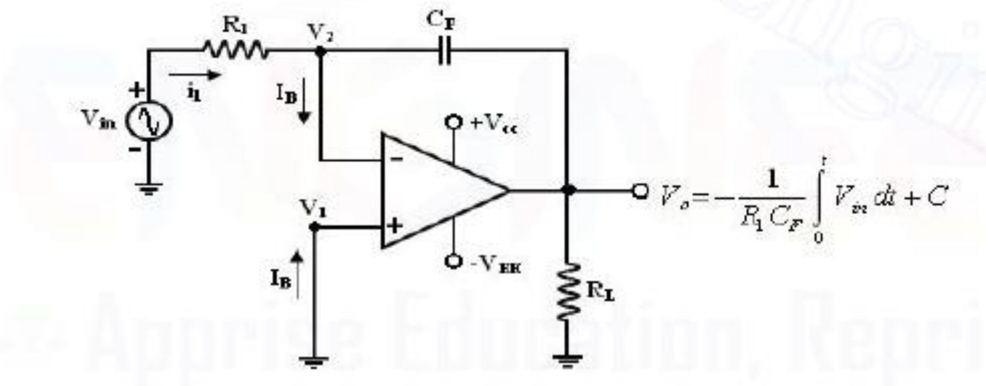


Fig 2.21 Integrator Circuit

$$i_1 = I_B + i_f$$

Since I_B is negligible small, $i_1 = i_F$

Relation between current through and voltage across the capacitor is

iC (t) = Cdvc(t)/dt

V 1=0 because A is very large,

The output voltage can be obtained by integrating both sides with respect to time

$$V_0(jw) = \frac{1}{jwR_1C_f} V_i\ (jw)$$

Indicates that the output is directly proportional to the negative integral of the input volts and inversely proportional to the time constant R1 CF.

Ex: If the input is sine wave -> output is cosine wave.

If the input is square wave -> output is triangular wave.

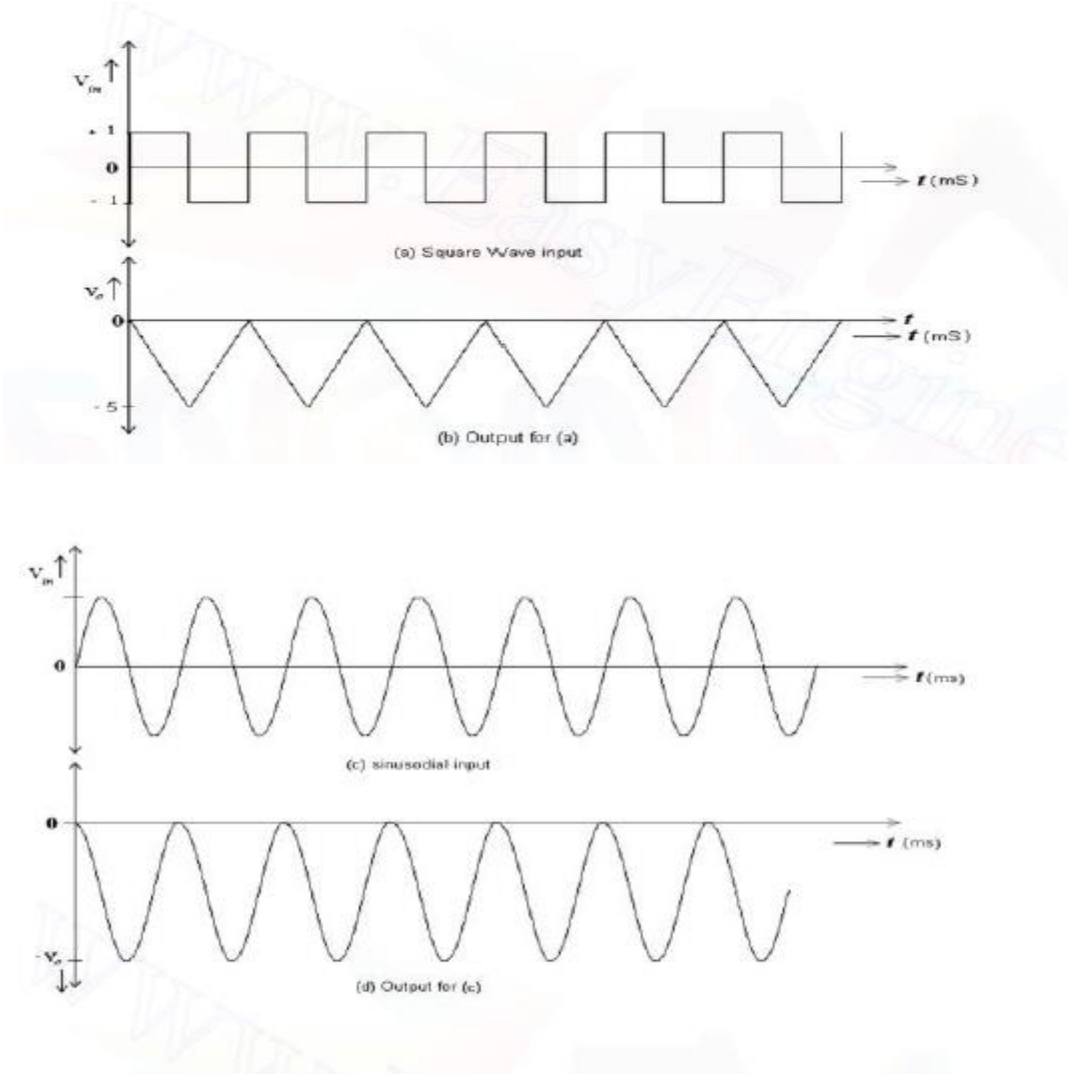


Fig.2.22 Waveforms from Integrator

These waveform with assumption of R1 Cf = 1, Vout =0V (i.e) C =0.

When Vin = 0 the integrator works as an open loop amplifier because the capacitor CF acts an open circuit to the input offset voltage Vio. The Input offset voltage V_{io} and the part of the input is charging capacitor CF produce the error voltage at the output of the integrator.

Practical Integrator:

Practical Integrator to reduce the error voltage at the output, a resistor RF is connected across the feedback capacitor CF. Thus RF limits the low frequency gain and hence minimizes the variations in the output voltages. The frequency response of the basic integrator, shown from this fb is the frequency at which the gain is dB and is given by

$$f_b = \frac{1}{2\pi R_1 C_F}$$

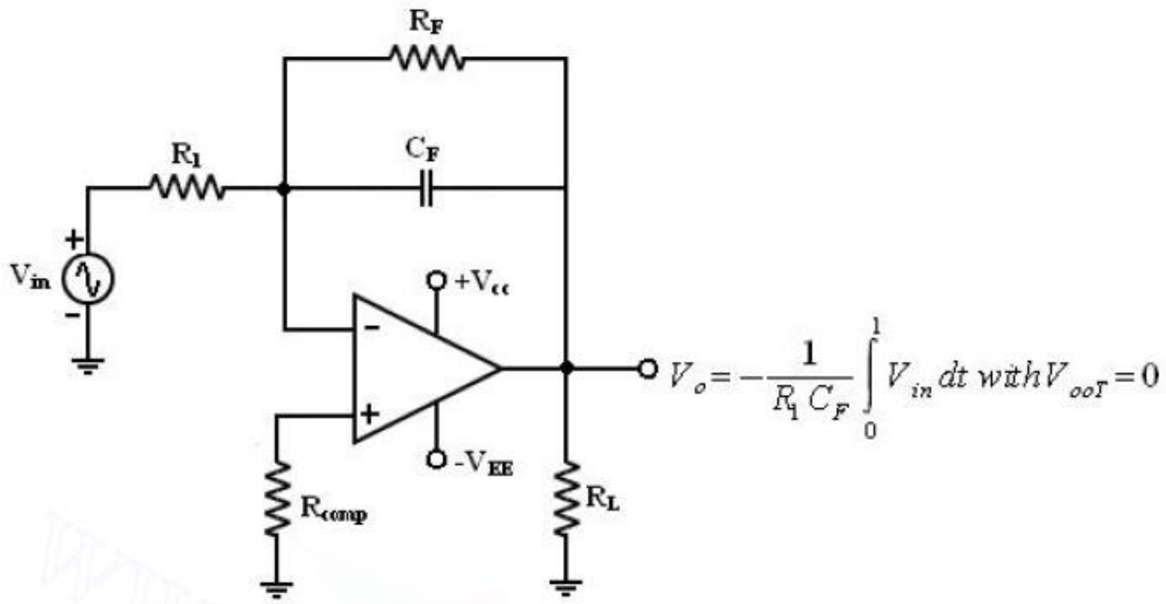


Fig. 2.23 Practical Integrator Circuit

- Both the stability and low frequency roll-off problems can be corrected by the addition of a resistor RF in the practical integrator.
- Stability refers to a constant gain as frequency of an input signal is varied over a certain range.
- Low frequency -> refers to the rate of decrease in gain roll off at lower frequencies.
- From the fig of practical Integrators, f is some relative operating frequency and for frequencies f to fa to gain RF / R1 is constant. After fa the gain decreases at a rate of 20dB/decade or between fa and fb the circuit act as an integrator.
- The gain limiting frequency fa is given by

$$f_a = \frac{1}{2\pi R_1 C_F}$$

• The value of fa and R1 CF and RF CF values should be selected such that fa<fb.

• The input signal will be integrated properly if the time period T of the signal is larger than or equal to RF CF,

$$f_b = \frac{1}{2\pi R_F C_F}$$

Uses:

Most commonly used in

- ✓ analog computers
- ✓ ADC
- ✓ Signal wave shaping circuits.

2.10 Differentiator:

The circuit performs the mathematical operation of differentiation (i.e.) the output waveform is the derivative of the input waveform. The differentiator may be constructed from a basic inverting amplifier if an input resistor R1is replaced by a capacitor C1. Since the differentiator performs the reverse of the integrator function. Thus the output V0 is equal to RF C1 times the negative rate of change of the input voltage Vin with time. The –sign indicates a 180 phase shift of the output waveform V0 with respect to the input signal. The below circuit will not do this because it has some practical problems. The gain of the circuit (RF /XC1) R with R in frequency at a rate of 20dB/decade. This makes the circuit unstable. Also input impedance XC1s with R in frequency which makes the circuit very susceptible to high frequency noise.

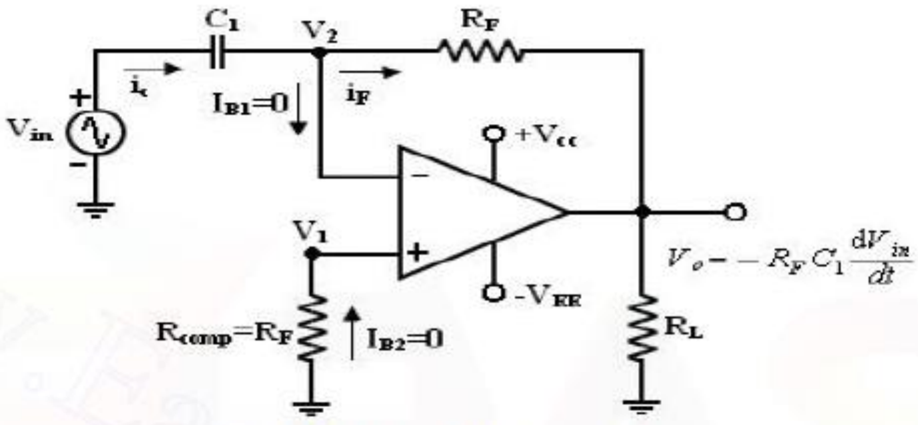


Fig 2.24 Basic Differentiator

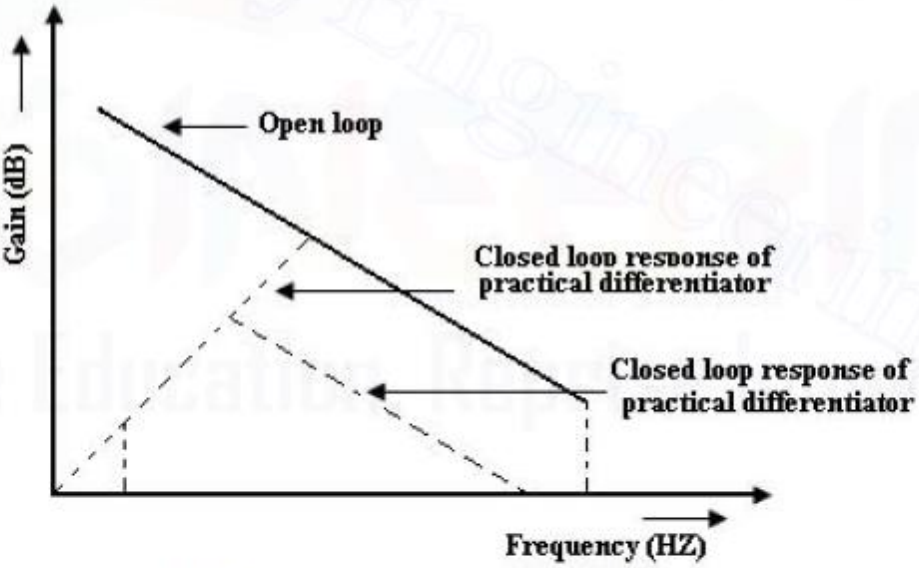


Fig. 2.25 Frequency response of differentiator

From the above fig. fa = frequency at which the gain is 0dB and is given by

$$f_a = \frac{1}{2\pi R_f C_1}$$

Both stability and high frequency noise problems can be corrected by the addition of two components. R_1 and C_F. This circuit is a practical differentiator. From Frequency fa to feedback the gain Rs at 20dB/decade after feedback the gain S at 20dB/decade. This 40dB/ decade change in gain is caused by the R_1 C_1 and R_F C_F combinations.

The gain limiting frequency f_b is given by,

$$f_b = \frac{1}{2\pi R_1 C_1}$$

Where $R_1 C_1 = R_F C_F$

$R_1 C_1$ and $R_F C_F$ help to reduce the effect of high frequency input, amplifier noise and offsets. All R1 C1 and RF CF make the circuit more stable by preventing the R in gain with frequency. The input signal will be differentiated properly, if the time period T of the input signal is larger than or equal to $R_F C_1$ (i.e) $T > R_F C_1$ generally, the value of Feedback and in turn $R_1 C_1$ and $R_F C_F$ values should be selected such that

$R_F C_1 >> R_1 C_1$

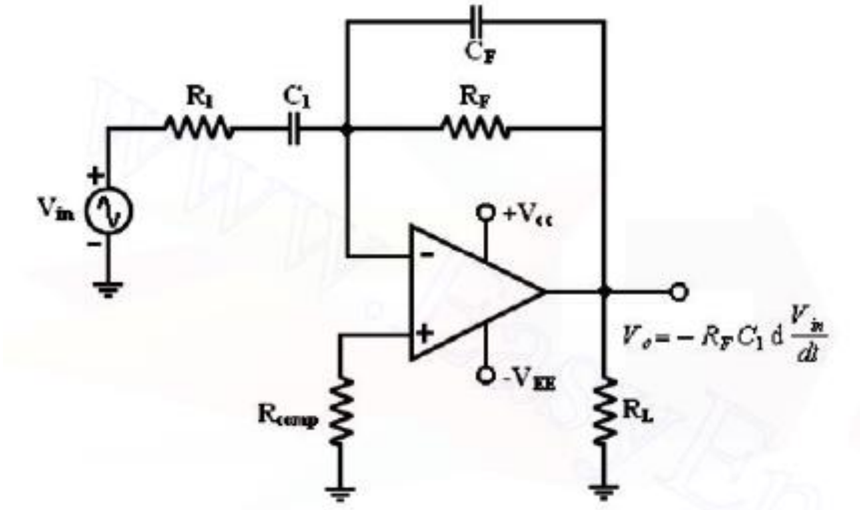


Fig 2.26 Practical Differentiator

A workable differentiator can be designed by implementing the following steps.

1. Select f_a equal to the highest frequency of the input signal to be differentiated then assuming a value of $C_1 < 1\mu f$. Calculate the value of RF.

2. Choose $f_b = 20f_a$ and calculate the values of R_1 and C_F so that $R_1 C_1 = R_F C_F$.

Uses:

It is used in wave shaping circuits to detect high frequency components in an input signal and alsoas a rate of change and detector in FM modulators.

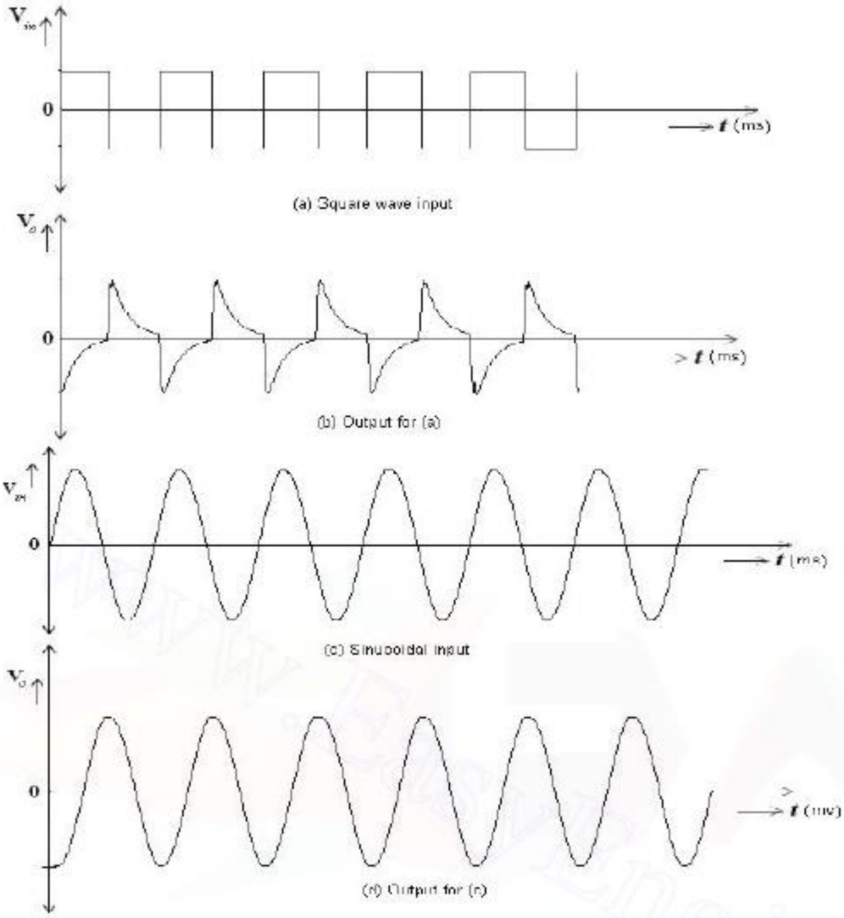


Fig.2.27 Output for practical differentiator.

2.11 Log and Antilog Amplifier:

Log Amplifier:

$$V_o = V_i ln\ \left(I_f / I_i\right)$$

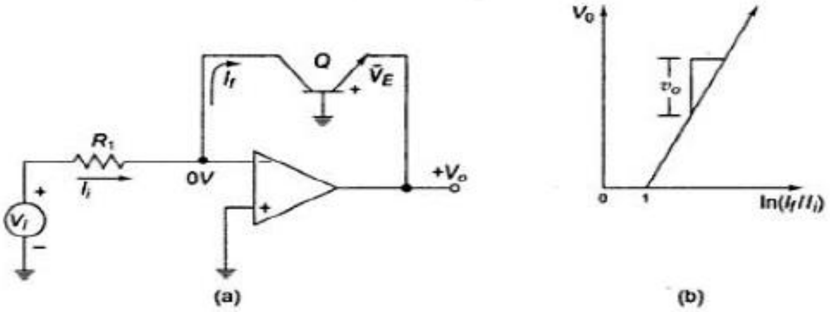


Fig 2.28 Fundamental log-amp Circuit and its characteristics

There are several applications of log and antilog amplifiers.

Antilog computation may require functions such as ln x, log x or sin hx.

Uses:

Direct dB display on a digital Voltmeter and Spectrum analyzer. Log-amp can also be used to compress the dynamic range of a signal. A grounded base transistor is placed in the feedback path. Since the collector is placed in the feedback path. Since the collector is held at virtual ground and the base is also grounded, the transistor's voltage-current relationship becomes that of a diode and is given by,

$I_E = I_S[e^{\frac{qV_{BE}}{kT}} - 1]$ and since $I_c = I_E$ for a grounded base transistor $I_C = I_S\, e^{kT}$

Is-emitter saturation current $\approx 10^{-13}$ A
k=Boltzmann's constant
T=absolute temperature (in ^{o} K)

$$V_o = -\frac{kT}{q} ln\left(\frac{V_i}{R_1 I_S}\right) = -\frac{kT}{q} ln\left(\frac{V_i}{V_R}\right)$$

where Vref =R1Is

The output voltage is thus proportional to the logarithm of input voltage.

Although the circuit gives natural log (ln), one can find log10, by proper scaling

Log10X=0.4343 ln X

The circuit has one problem. The emitter saturation current Is varies from transistor to transistor and with temperature. Thus a stable reference voltage V ref cannot be obtained. This is eliminated by the circuit given below

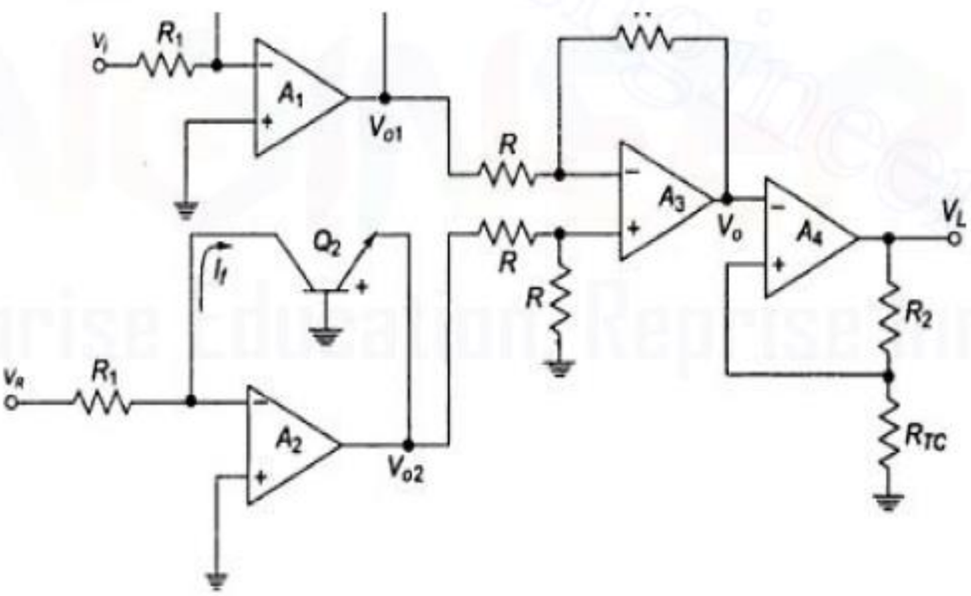


Fig. 2.29 Logarithmic amplifier with compensation of emitter saturation current

The input is applied to one log-amp, while a reference voltage is applied to one log-amp, while a reference voltage is applied to another log-amp. The two transistors are integrated close together in the same silicon wafer. This provides a close match of saturation currents and ensures good thermal tracking.

Assume IS1=IS2=IS

Thus the reference level is now set with a single external voltage source. Its dependence on device and temperature has been removed. The voltage V_o is still dependent upon temperature and is directly proportional to T. This is compensated by the last op-amp stage A4 which provides a non-inverting gain of (1+R2/RTC). Temperature compensated output voltage V_L

$$V_L = \left(1 + \frac{R_2}{R_{TC}}\right)\frac{kT}{q} ln\left(\frac{V_i}{V_R}\right)$$

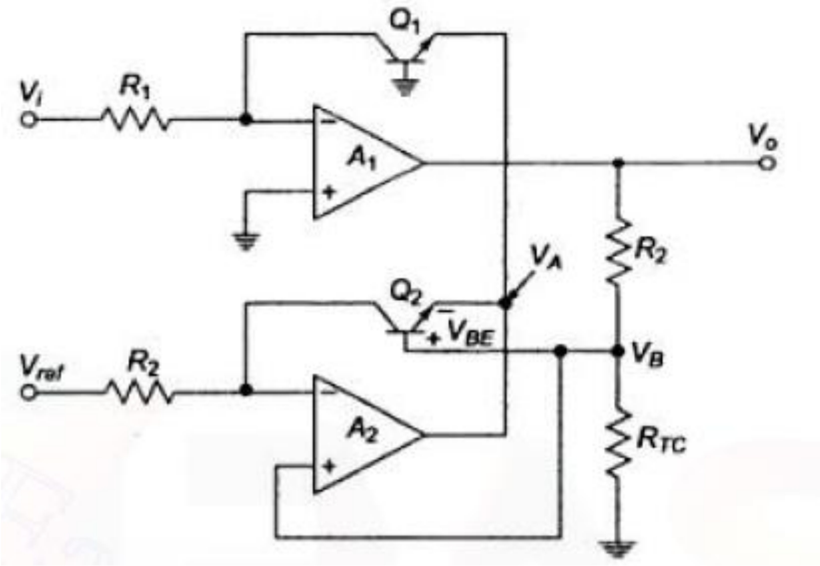


Fig.2.30 Logarithmic amplifier using two op amps

Where RTC is a temperature-sensitive resistance with a positive coefficient of temperature (sensor) so that the slope of the equation becomes constant as the temperature changes.

2.12 Antilog Amplifier

A circuit to convert logarithmically encoded signal to real signals. Transistor in inverting input converts input voltage into logarithmically varying currents

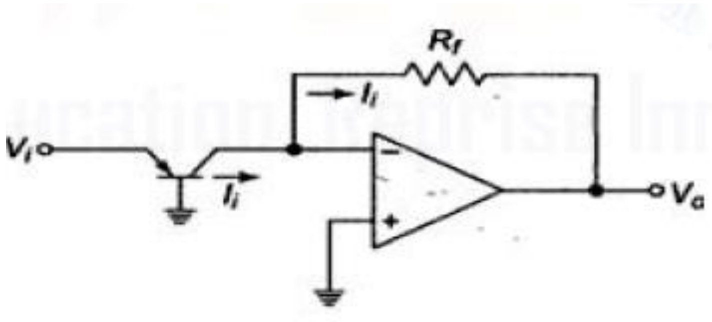


Fig. 2.31 Antilog amplifier

$$I_i = I_c = I_s(e^{\frac{\eta V_{BE}}{kT}}) \text{ and } V_0 = R_f I_s(e^{\frac{\eta V_{BE}}{kT}})$$

The circuit is shown in figure below. The input V_i for the antilog-amp is fed into the temperature compensating voltage divider R_2 and R_{TC} and then to the base of Q2. The output of A2 is fed back to R1 at the inverting input of op amp A_1. The non-inverting inputs are grounded

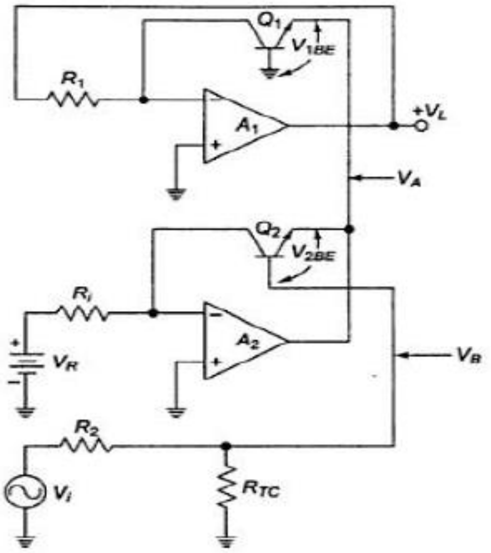


Fig 2.32 Antilog amplifier

$V_{1BE} = \frac{kT}{q}\ln[\frac{V_L}{R_1 I_S}]$ and $V_{2BE} = \frac{kT}{q}\ln[\frac{V_B}{R_1 I_S}]$ and $V_A = - V_{1BE}$ and $V_B = R_{TC}/(R_2+R_{TC})\ V_i$

$V_{Q2E} = V_B + V_{2BE} = R_{TC}/(R_2+R_{TC})\ V_i - \frac{kT}{q}\ln[\frac{V_B}{R_1 I_S}]$

$V_{Q2E} = V_A$

Therefore,

$$-\frac{kT}{q}ln\left(\frac{V_L}{R_1 I_S}\right) = \frac{R_{TC}}{R_2 + R_{TC}}V_i + \frac{kT}{q}ln\left(\frac{V_R}{R_1 I_S}\right)$$

Rearranging, we get

$$\frac{R_{TC}}{R_2 + R_{TC}}V_i = -\frac{kT}{q}ln\left(\frac{V_L}{R_1 I_S}\right) - \frac{kT}{q}ln\left(\frac{V_R}{R_1 I_S}\right)$$

$$= -\frac{kT}{q}ln\left(\frac{V_L}{V_R}\right)$$

We know that $\log_{10} x = 0.4343\, ln\, x$.

Therefore, $-0.4343\left(\frac{q}{kT}\right)\left(\frac{R_{TC}}{R_2 + R_{TC}}\right)V_i = 0.4343\, ln\ \left(\frac{V_L}{V_R}\right)$

$$-0.4343\left(\frac{q}{kT}\right)\left(\frac{R_{TC}}{R_2 + R_{TC}}\right)V_i = \log_{10}\ \left(\frac{V_L}{V_R}\right)$$

$$-KV_i = \log\left(\frac{V_L}{V_R}\right)$$

$$K = 0.4343\left(\frac{q}{kT}\right)\left(\frac{R_{TC}}{R_2 + R_{TC}}\right)$$

$$V_L = V_R 10^{-KV_i}$$

The output Vo of the antilog- amp is fed back to the inverting input of A1 through the resistor R_1. Hence an increase of input by one volt causes the output to decrease by a decade.

2.13 Comparator

A comparator compares a signal voltage on one input of an op-amp with a known voltage called a reference voltage on the other input. Comparators are used in circuits such as,

- ✓ Digital Interfacing
- ✓ Schmitt Trigger
- ✓ Discriminator
- ✓ Voltage level detector and oscillators

2.13.1 Non-inverting Comparator:

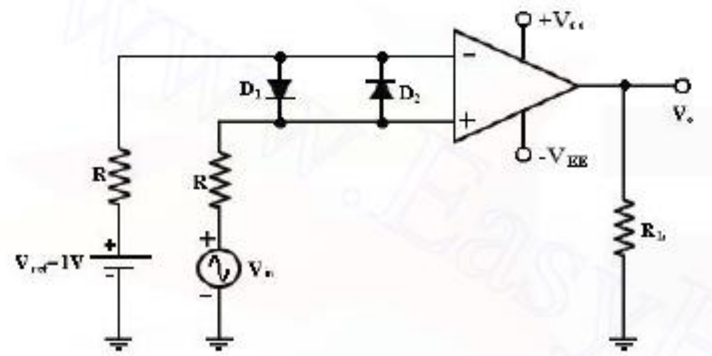


Fig. 2.33 non-inverting comparator circuit

A fixed reference voltage V_{ref} of 1 V is applied to the negative terminal and time varying signal voltage Vin is applied to the positive terminal.

When Vin is less than Vref the output becomes V0 at –Vsat

[Vin < Vref => V0 (-Vsat)].

When Vin is greater than Vref, the (+) input becomes positive, the V0 goes to +Vsat.

[Vin > Vref => V0 (+Vsat)].

Thus the V0 changes from one saturation level to another.

The diodes D1 and D2 protect the op-amp from damage due to the excessive input voltage Vin. Because of these diodes, the difference input voltage Vid of the op-amp diodes are called clamp diodes.

The resistance R in series with Vin is used to limit the current through D1 and D2. To reduce offset problems, a resistance Rcomp = R is connected between the (-ve) input and Vref.

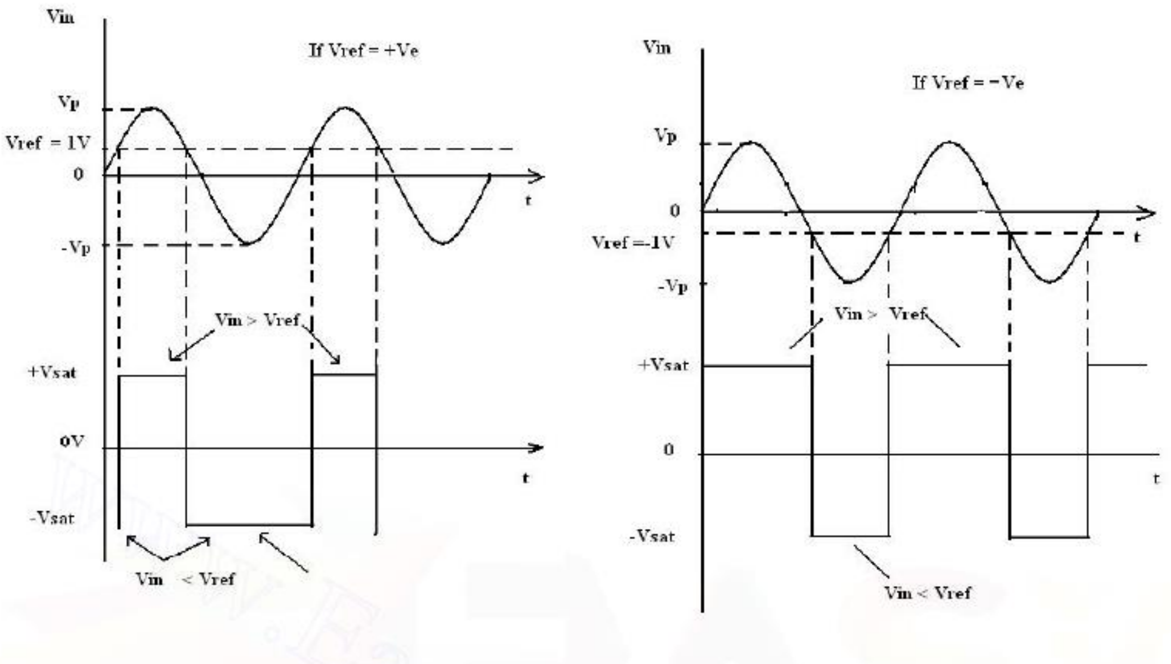


Fig. 2.34 Input and Output Waveforms of non-inverting comparator

2.13.2 Inverting Comparator:

This fig shows an inverting comparator in which the reference voltage Vref is applied to the (+) input terminal and Vin is applied to the (-) input terminal.

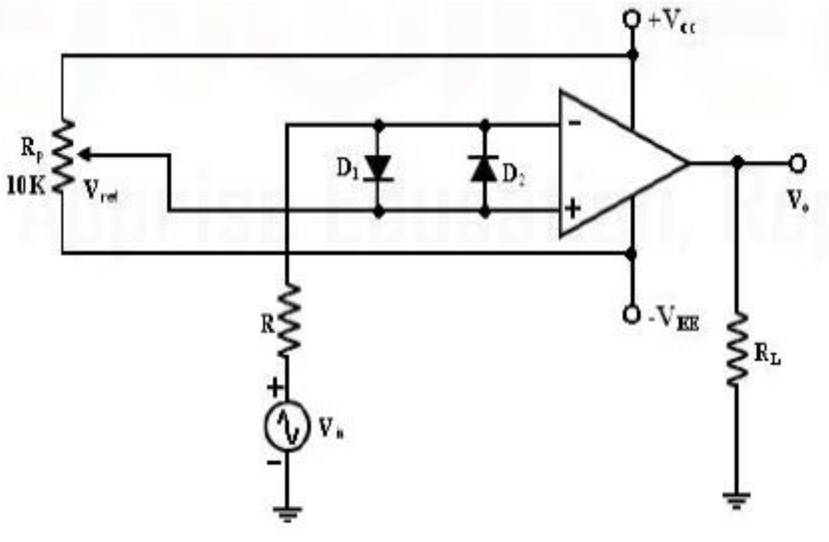


Fig. 2.35 Inverting comparator circuit

In this circuit Vref is obtained by using a 10K potentiometer that forms a voltage divider with DC supply volt +Vcc and -1 and the wiper connected to the input. As the wiper is moved towards +Vcc, Vref becomes more positive. Thus a Vref of a desired amplitude and polarity can be got by simply adjusting the 10k potentiometer.

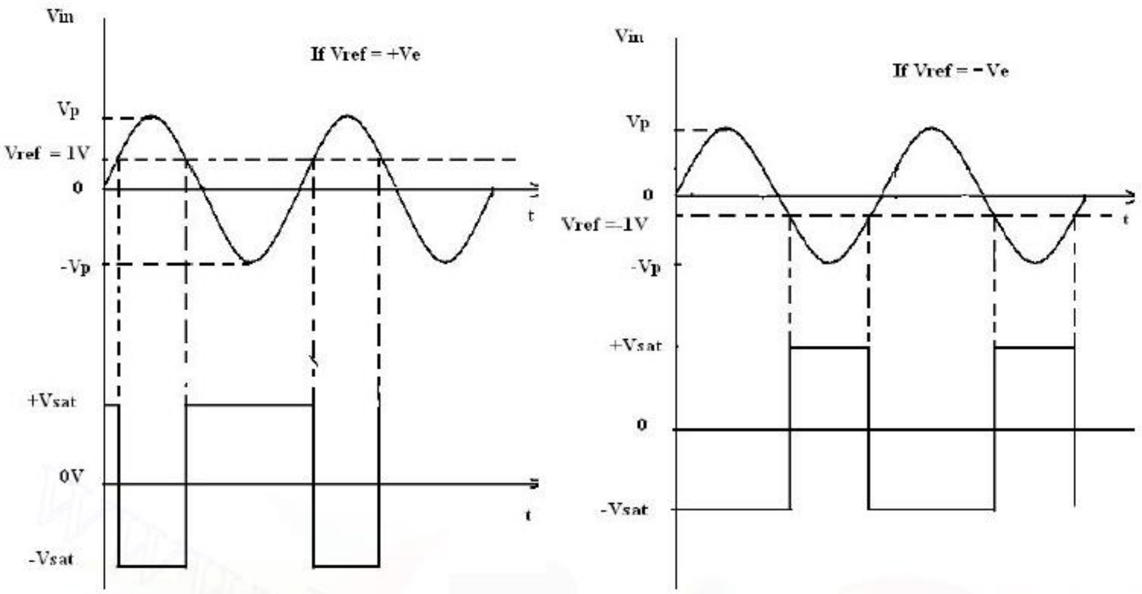


Fig. 2.36 Input and Output Waveforms of non-inverting comparator

Applications:

- ✓ **Zero Crossing Detector: [Sine wave to Square wave converter]**

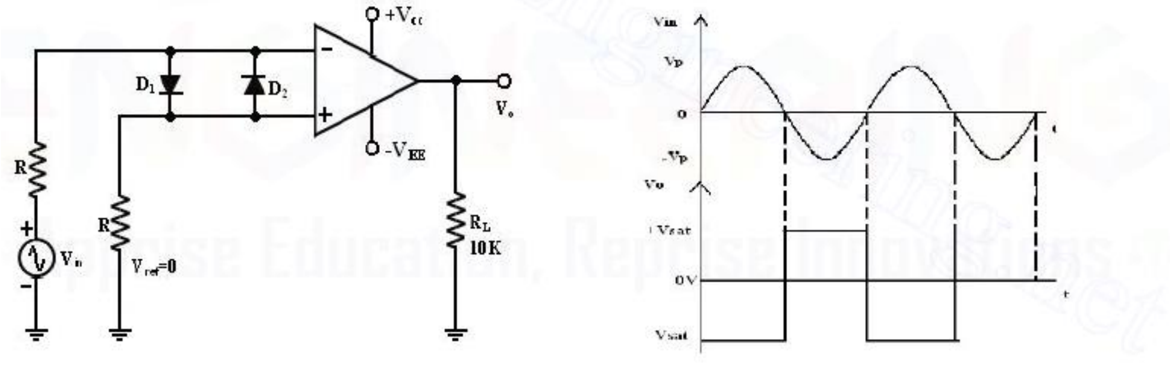


Fig. 2.37 Zero crossing detector circuit and input-output waveforms

One of the applications of comparator is the zero crossing detector or —sine wave to Square wave Converter. The basic comparator can be used as a zero crossing detector by setting Vref is set to Zero. This Fig shows when in what direction an input signal Vin crosses zero volts. (i.e.) the o/p V0 is driven into negative saturation when the input the signal Vin passes through zero in positive direction. Similarly, when Vin passes through Zero in negative direction the output V0 switches and saturates positively.

- ✓ Drawbacks of Zero- crossing detector:

In some applications, the input Vin may be a slowly changing waveform, (i.e) a low frequency signal. It will take Vin more time to cross 0V, therefore V0 may not switch quickly from one saturation voltage to the other. Because of the noise at the op-amp‘s input terminals the output V0 may fluctuate between 2 saturations voltages +Vsat and –Vsat. Both of these problems can be cured with the use of regenerative or positive feedback that cause the output V0 to change faster and eliminate any

false output transitions due to noise signals at the input Inverting comparator with positive feedback . This is known as Schmitt Trigger.

2.14 Schmitt Trigger: [Square Circuit]

This circuit converts an irregular shaped waveform to a square wave or pulse. The

circuit is known as Schmitt Trigger or squaring circuit. The input voltage Vin triggers (changes the state of) the o/p V0 every time it exceeds certain voltage levels called the upper threshold Vut and lower threshold voltage.

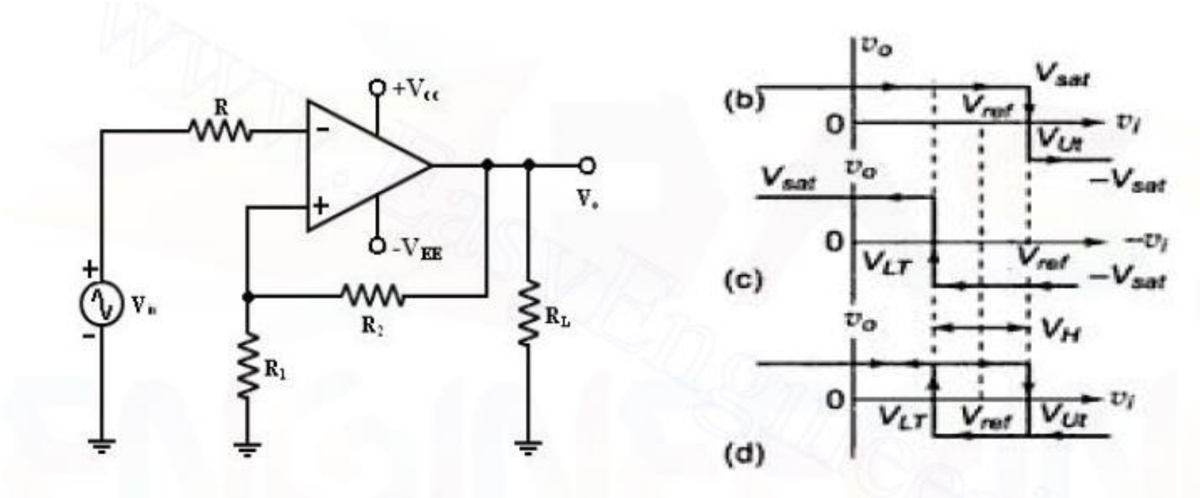


Fig.2.38 Schmitt Trigger circuit and hysteresis phenomenon

These threshold voltages are obtained by using the voltage divider R1– R2, where the voltage across R_1 is feedback to the (+) input. The voltage across $R_1$is variable reference threshold voltage that depends on the value of the output voltage. When V0 = +Vsat, the voltage across R1 is called upper threshold voltage Vut.

The input voltage Vin must be more positive than Vut in order to cause the output V0 to switch from +Vsat to -Vsat using voltage divider rule, Voltage at (+) input terminal is $V_{UT}=V_{ref}+ R_2 (V_{sat}-V_{ref})/(R_1+R_2)$ when $V_0= +v_{sat}$.

When v0= -vsat. Hysteris width VH= $V_{UT} - V_{LT} = 2 R_2 (V_{sat})/ (R_1+R_2)$

When V0 = -Vsat, the voltage across R1 is called lower threshold voltage Vlt .the Vin must be more negative than Vlt in order to cause V0 to switch from –Vsat to +Vsat.

for Vin > Vlt , V0 is at –Vsat.

Voltage at (+) terminal is $V_{LT}=V_{ref} - R_2 (V_{sat}+V_{ref})/(R_1+R_2)$.

- If the threshold voltages Vut and Vlt are made larger than the input noise voltages, the positive feedback will eliminate the false o/p transitions.
- Also the positive feedback, because of its regenerative action, will make V0 switch faster between +Vsat and –Vsat.
- Resistance Rcomp=R1 || R2 is used to minimize the offset problems.
- The comparator with positive feedback is said to exhibit hysteresis, a dead band condition. (i.e) when the input of the comparator exceeds Vut its output switches from +Vsat to –Vsat and reverts to its original state, +Vsat when the input goes below V_{LT}. The hysteresis voltage is equal to the difference between Vut and Vlt. Therefore

V_H= Vut – Vlt.

- If Vref=0, Vut= $-V_{LT} = 2 R_2(V_{sat})/(R_1+R_2)$

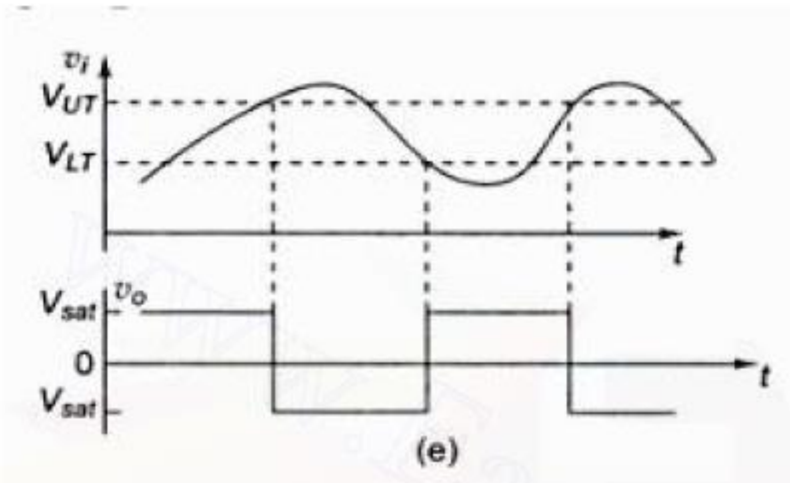


Fig. 2.39 Schmitt Trigger as squarer

2.15 Precision Rectifier:

The ordinary diodes cannot rectify voltages below the cut-in-voltage of the diode. A circuit which can act as an ideal diode or precision signal – processing rectifier circuit for rectifying voltages which are below the level of cut-in voltage of the diode can be designed by placing the diode in the feedback loop of an op-amp.

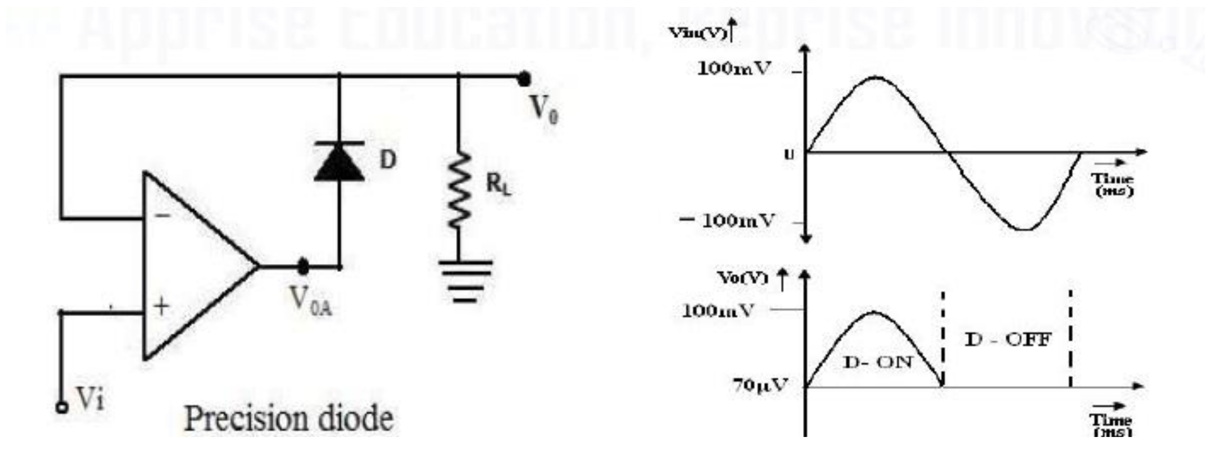


Fig.2.40 Precision diode and its waveform

Precision diodes:

Figure shows the arrangement of a precision diode. It is a single diode arrangement and functions as a non-inverting precision half– wave rectifier circuit. If V1 in the circuit of figure is positive, the op-amp output VOA also becomes positive. Then the closed loop condition is achieved for the op-amp and the output voltage V0 = Vi . When Vi < 0, the voltage V0A becomes negative and the diode is reverse biased. The loop is then broken and the output V0 = 0.

Consider the open loop gain AOL of the op-amp is approximately 104 and the cut-in voltage Vγ for silicon diode is ≈ 0.7V. When the input voltage Vi > Vγ / AOL, the output of the op-amp VOA exceeds Vγ and the diode D conducts. Then the circuit acts like a voltage follower for input voltage level Vi > Vγ / AOL ,(i.e.

when Vi > 0.7/104 = 70μV), and the output voltage V0 follows the input voltage during the positive half cycle for input voltages higher than 70μV as shown in figure.

When Vi is negative or less than Vγ / AOL, the output of op-amp VOA becomes

negative, and the diode becomes reverse biased. The loop is then broken, and the op-amp swings down to negative saturation. However, the output terminal is now isolated from both the input signal and the output of the op-amp terminal thus V0 =0.

No current is then delivered to the load RL except for the small bias current of the op-amp and the reverse saturation current of the diode.

This circuit is an example of a non-linear circuit, in which linear operation is achieved

over the remaining region (Vi < 0). Since the output swings to negative saturation level when Vi < 0, the circuit is basically of saturating form. Thus the frequency response is also limited.

Applications: The precision diodes are used in

- ✓ half wave rectifier,
- ✓ Full-wave rectifier,
- ✓ peak value detector,
- ✓ Clipper and clamper circuits.

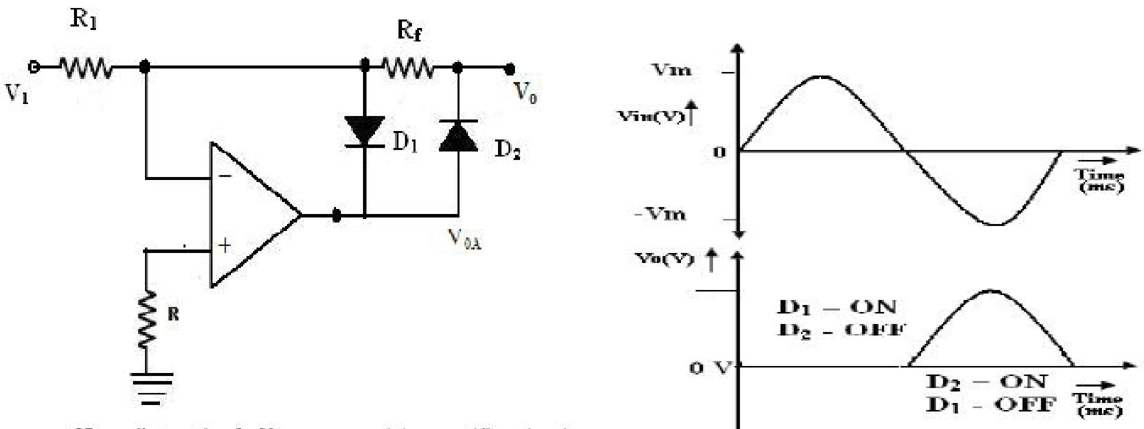
Disadvantage:

It can be observed that the precision diode as shown in figure operated in the first quadrant with Vi > 0 and V0 > 0. The operation in third quadrant can be achieved by connecting the diode in reverse direction.

2.15.1 Half – wave Rectifier:

A non-saturating half wave precision rectifier circuit is shown in figure. When Vi > 0V, the voltage at the inverting input becomes positive, forcing the output VOA to go negative. This results in forward biasing the diode D1 and the op-amp output drops only by ≈ 0.7V below the inverting input voltage. Diode D2 becomes reverse biased. The output voltage V0 is zero when the input is positive.

When Vi > 0, the op-amp output VOA becomes positive, forward biasing the diode D2 and reverse biasing the diode D1. The circuit then acts like an inverting amplifier circuit with a nonlinear diode in the forward path. The gain of the circuit is unity when Rf = Ri.



Non - Saturating half - wave precision rectifier circuit

Input and Output Waveforms

Fig. 2.41 Half wave rectifier and its operation

The circuit operation can mathematically be expressed as

$V_0 = 0$ when $V_i > 0$ and

$V_0 = R_f/R_i V_1$ for $V_i < 0$

The voltage V_{OA} at the op amp output is $V_{OA} = -0.7V$ for $V_i > 0$

$V_{OA} = R_f/R_i V_1 + 0.7V$ for $V_i < 0$

Advantages:

- ✓ it is a precision half wave rectifier and
- ✓ it is a non saturating one.

The inverting characteristics of the output V0 can be circumvented by the use of an additional inversion for achieving a positive output.

2.15.2 Full wave Rectifier:

The first part of the Full wave circuit is a half wave rectifier circuit. The second part of the circuit is an inverting amplifier.

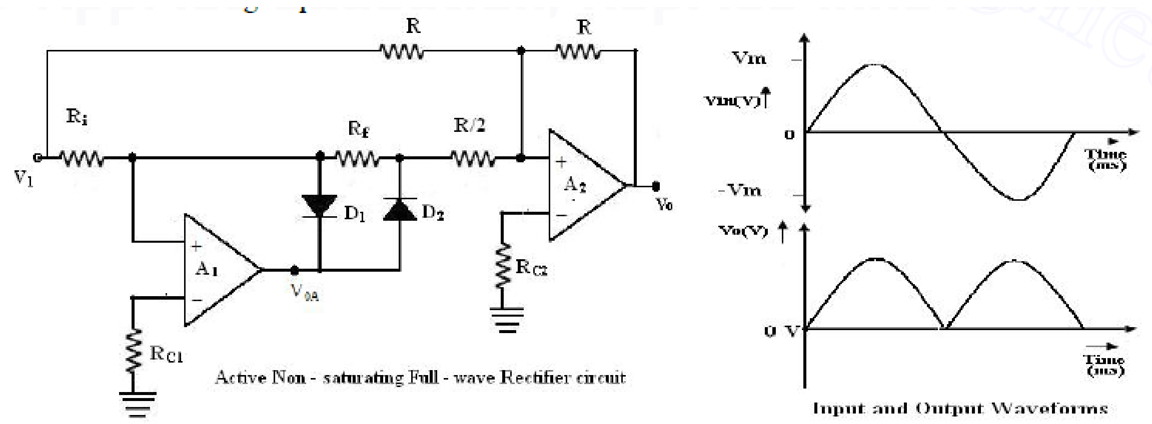


Fig. 2.42 Full wave rectifier and its operation

For positive input voltage Vi > 0V and assuming that RF =Ri = R, the output voltage VOA = Vi. The voltage V0 appears as (-) input to the summing op-amp circuit formed by A2, The gain for the input V‘0 is R/(R/2), as shown in figure.

The input Vi also appears as an input to the summing amplifier. Then, the net output is V0 =-Vi -2V0= -Vi -2(-Vi) = Vi. Since Vi > 0V, V0 will be positive, with its input output characteristics in first quadrant. For negative input Vi < 0V, the output V‘0 of the first part of rectifier circuit is zero. Thus, one input of the summing circuit has a value of zero. However, Vi is also applied as an input to the summer circuit formed by the op-amp A2.

The gain for this input id (-R/R) = -1, and hence the output is V0 = -Vi. Since Vi is negative, V0 will be inverted and will thus be positive. This corresponds to the second quadrant of the circuit.

To summarize the operation of the circuit,

V0 = Vi when Vi < 0V and

V0 = Vi for Vi > 0V, and hence

V0 = |Vi |

2.16 Peak Detector

Square, Triangular, Saw tooth and pulse waves are typical examples of non-sinusoidal waveforms. A conventional AC voltmeter cannot be used to measure these sinusoidal waveforms because it is designed to measure the RMS value of the pure sine wave. One possible solution to this problem is to measure the peak values of the non-sinusoidal waveforms. Peak detector measures the +ve peak value of the square wave input.

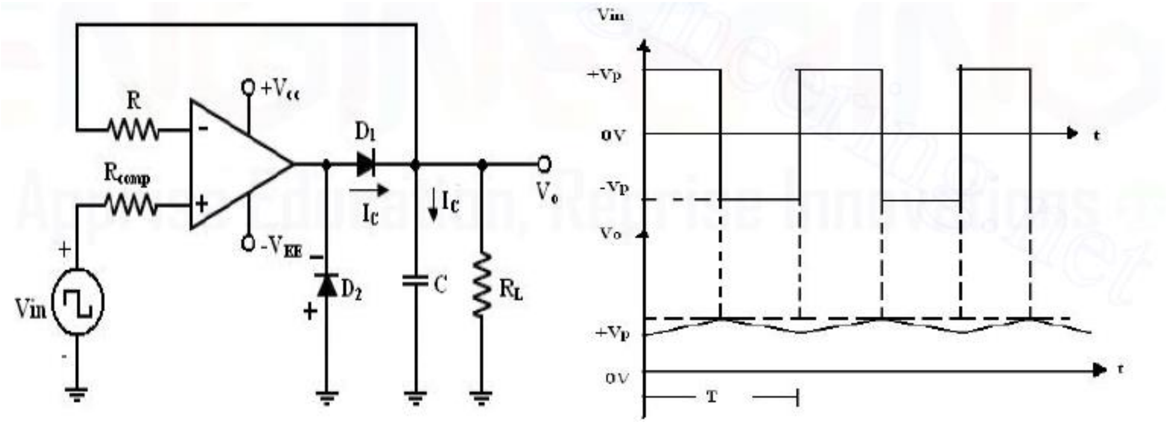


Fig. 2.43 Peak detector circuit and input and output waveforms

i) During the positive half cycle of Vin:

the o/p of the op-amp drives D1 on. (Forward biased)

Charging capacitor C to the positive peak value Vp of the input volt Vin.

ii) During the negative half cycle of Vin:

D1 is reverse biased and voltage across C is retained.

The only discharge path for C is through RL since the input bias IB is negligible.

For proper operation of the circuit, the charging time constant (CRd) and discharging time constant (CR_L) must satisfy the following condition.

CRd <= T/10

Where Rd = Resistance of the forward-biased diode.

T = time period of the input waveform.

CRL >= 10T (2)

Where R_L = load resistor.

If R_L is very small so that eqn. (2) cannot be satisfied.

- Use a (buffer) voltage follower circuit between capacitor C and RL load resistor.
- R is used to protect the op-amp against the excessive discharge currents.
- Rcomp = minimizes the offset problems caused by input current
- D2 conducts during the –ve half cycle of Vin and prevents the op-amp from going into negative saturation.

Note: -ve peak of the input signal can be detected simply by reversing diode D1 and D2

2.17 Clipper and clipper

Applications:

Wave shaping circuits are commonly used in digital computers and communication such as TV and FM receiver.

Wave shaping technique include clipping and clamping.

In op-amp clipper circuits a rectifier diode may be used to clip off a certain portion of the input signal to obtain a desired o/p waveform.

The diode works as an ideal diode (switch) because when on, the voltage drop across the diode is divided by the open loop gain of the op-amp. When off (reverse biased) the diode is an open circuit.

In an op-amp clamper circuits, however a predetermined dc level is deliberately inserted in the o/p volt. For this reason, the clamper is sometimes called a dc inverter.

2.17.1 Positive and Negative

Clipper: Positive Clipper:

A circuit that removes positive parts of the input signal can be formed by using an op-amp with a rectifier diode. T he clipping level is determined by the reference voltage Vref, which should less than the i/p range of the op-amp ($V_{ref} < V_{in}$). The Output voltage has the portions of the positive half cycles above V_{ref} clipped off.

The circuit works as follows:

During the positive half cycle of the input, the diode D1 conducts only until Vin = Vref.

This happens because when Vin <Vref, the output volts V_0 of the op-amp becomes negative to device D_1 into conduction when D_1 conducts it closes feedback loop and op-amp operates as a voltage follower. (i.e.) Output V0 follows input until Vin = Vref.

When Vin > Vref => the V0 becomes +ve to derive D1 into off. It opens the feedback loop and op- amp operates open loop. When Vin drops below Vref (Vin<Vref) the o/p of the op-amp V0 again becomes –ve to device D1 into conduction. It closes the feedback path. (o/p follows the i/p).

Thus diode D1 is on for vin<Vref (o/p follows the i/p) and D1 is off for Vin>Vref.

The op-amp alternates between open loop (off) and closed loop operation as the D1 is turned off and on respectively. For this reason the op-amp used must be high speed and preferably compensated for unity gain.

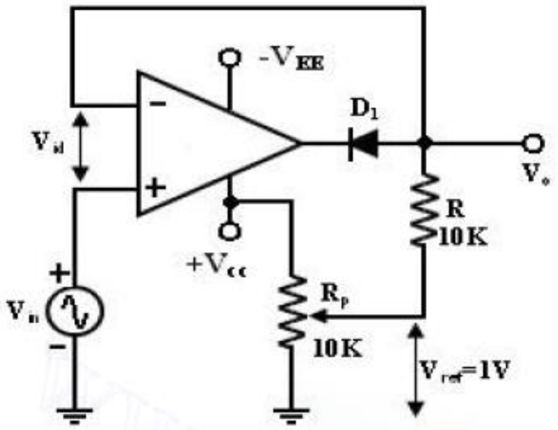


Fig. 2.44 Positive Clipper

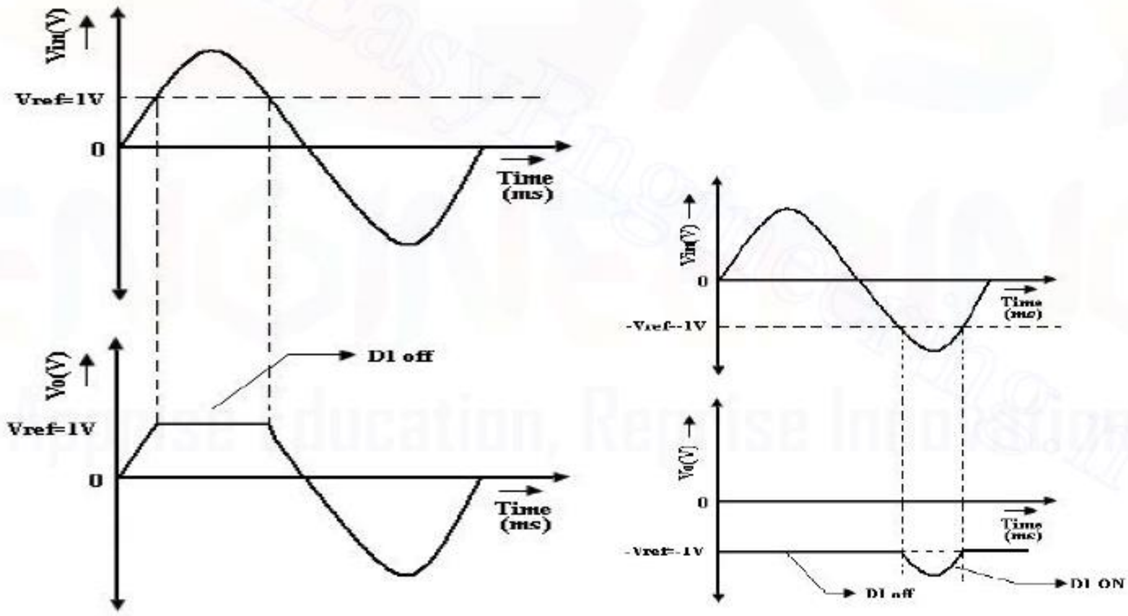


Fig 2.45 Positive clipper input output waveforms

Ex: for high speed op-amp HA 2500, LM310, μA 318. In addition the difference input voltage (Vid=high) is high during the time when the feedback loop is open (D1 is off) hence an op-amp with a high difference input voltage is necessary to prevent input breakdown. If Rp (pot) is connected to –VEE instead of +Vcc, the ref voltage Vref will be negative (Vref = -ve). This will cause the entire o/p waveform above –Vref to be clipped off.

2.17.2 Negative Clipper:

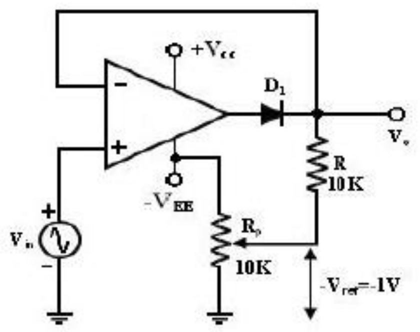


Fig.2.46 Negative clipper

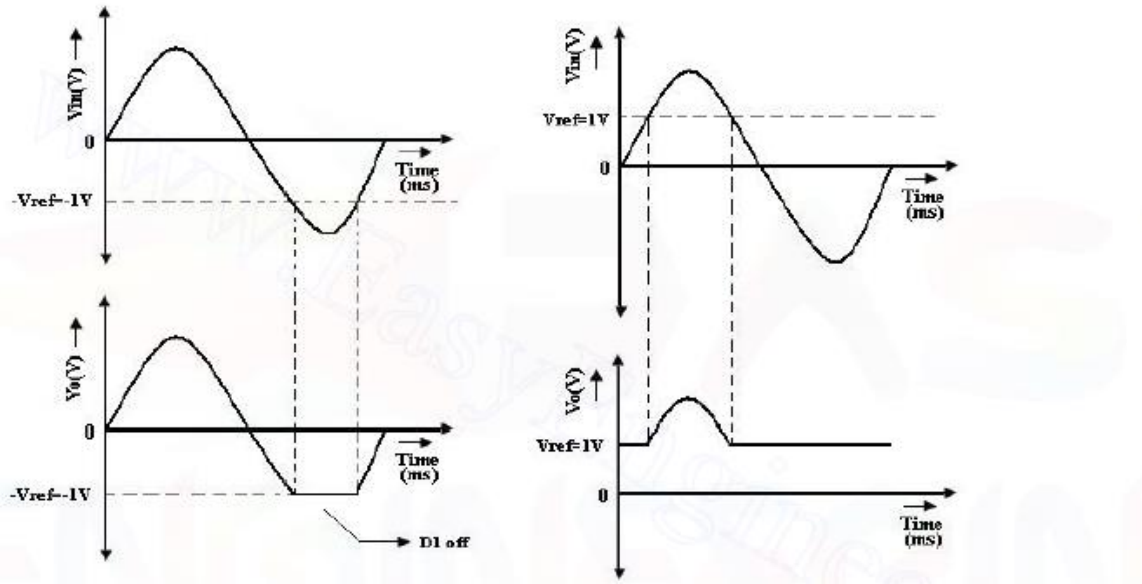


Fig. 2.47 Input output waveforms

The positive clipper is converted into a –ve clipper by simply reversing diode D1 and changing the polarity of Vref voltage. The negative clipper clips off the –ve parts of the input signal below the reference voltage. Diode D1 conducts -> when Vin > -Vref and therefore during this period o/p volt V0 follows the i/p volt Vin. The –Ve portion of the output volt below –Vref is clipped off because (D1 is off) Vin<-Vref. If –Vref is changed to –Vref by connecting the potentiometer Rp to the +Vcc, the V0 below +Vref will be clipped off. The diode D1 must be on for Vin > Vref and off for Vin.

2.17.3 Positive and Negative Clampers:

In clamper circuits a predetermined dc level is added to the output voltage. (or) The output is clamped to a desired dc level.

1. If the clamped dc level is +ve, the clamper is positive clamper
2. If the clamped dc level is –ve, the clamper is negative clamper.

Other equivalent terms used for clamper are dc inserter or restorer. Inverting and Non-Inverting that uses this technique.

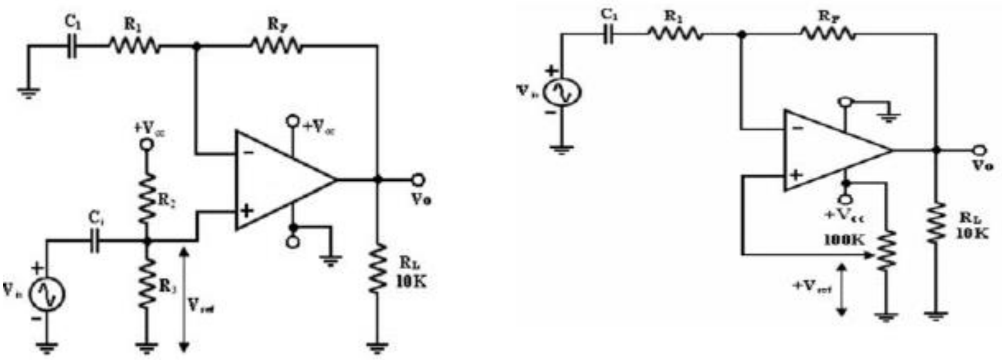


Fig.2.48 Positive –Negative campers

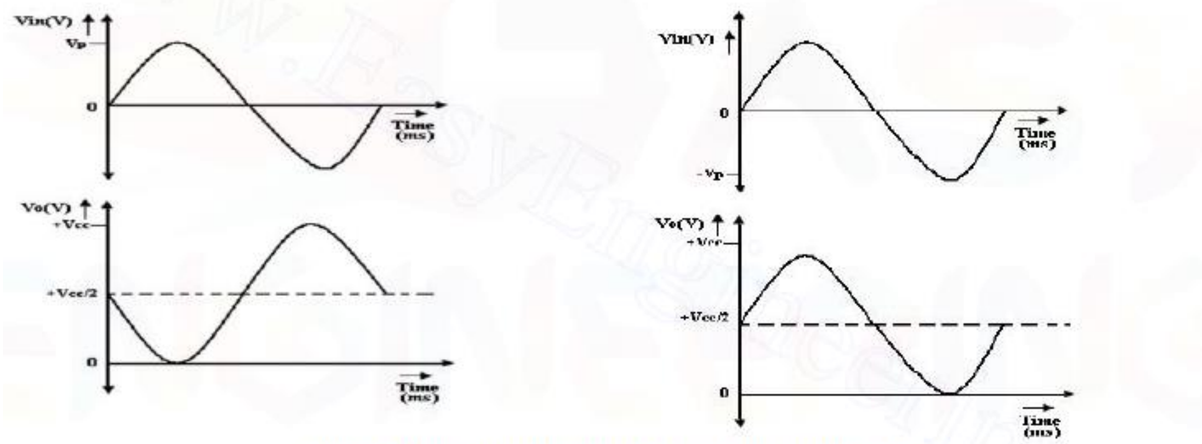


Fig.2.49 Input **and output waveform with +Vref**

Capacitor:

The Value of the capacitors in these circuits depends on different input rates and pulse widths.

1. In both circuits the dc level added to the o/p voltage is approximately equal to Vcc/2.
2. This +ve fixed dc level is needed to obtain a maximum undistorted symmetrical sine wave.

Peak clamper circuit:

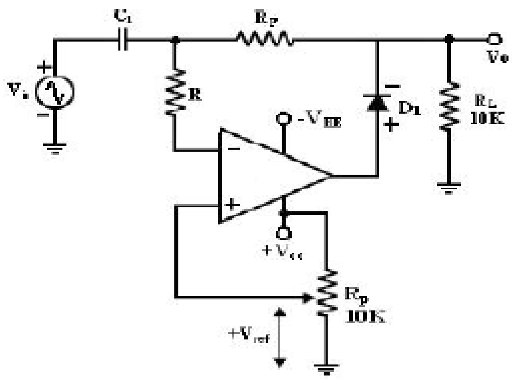


Fig.2.50 Peak clamper circuit

In this circuit, the input waveform peak is clamped at Vref. For this reason, the circuit is called the peak clamper. First consider the input voltage Vref at the (+) input: since this volt is +ve, V'0 is also +ve which forward biases D1. This closed the feedback loop. Voltage Vin at the (-) input: During its –ve half cycle, diode D1 conducts, charging c; to the –ve peak value of Vp. During the +ve half cycle, diode D1 in reverse biased. Since this voltage Vp is in series with the +ve peak volt Vp the o/p volt V0 = 2 Vp. Thus the nett o/p is Vref plus 2 Vp. So the – ve peak of 2 Vp is at Vref. For precision clamping, CiRd << T/2

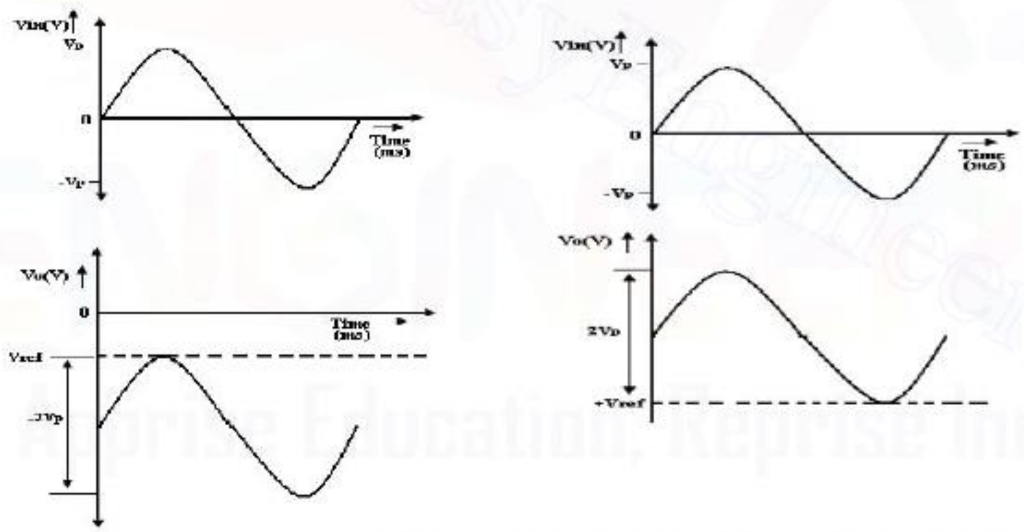


Fig. 2.51 Input and Output Waveform with –Vref

Where Rd = resistance of diode D1 when it is forward biased.

T = time period of the input waveform. Resistor R is used to protect the op-amp against excessive discharge currents from capacitor Ci especially when the dc supply voltages are switched off. A +ve peak clamping is accomplished by reversing D1 and using –ve reference voltage (-Vref).

Note:

Inv and Non-Inv clamper – Fixed dc level

Peak clamper – Variable dc level

2.18 Active filters:

An electric filter is often a frequency selective circuit that passes a specified band of frequencies and blocks or alternates signal and frequencies outside this band.

Filters may be classified as

1. Analog or digital.
2. Active or passive
3. Audio (AF) or Radio Frequency (RF)

1. Analog or digital filters:

Analog filters are designed to process analog signals, while digital filters process analog signals using digital technique.

2. Active or Passive:

Depending on the type of elements used in their construction, filter may be classified as passive or Active elements used in passive filters are Resistors, capacitors, inductors. Elements used in active filters are transistor, or op-amp.

Active filters offer the following advantages over passive filters:

1. Gain and Frequency adjustment flexibility:

Since the op-amp is capable of providing gain, the i/p signal is not attenuated as it is in a passive filter. [Active filter is easier to tune or adjust].

2. No loading problem:

Because of the high input resistance and low o/p resistance of the op-amp, the active filter does not cause loading of the source or load.

3. Cost:

Active filters are more economical than passive filter. This is because of the variety of cheaper op-amps and the absence of inductors.

✓ The most commonly used filters are these:

1. Low pass Filters
2. High pass Filters
3. Band pass filters

4. Band –reject filters
5. All pass filters.

Frequency response of the active filters:

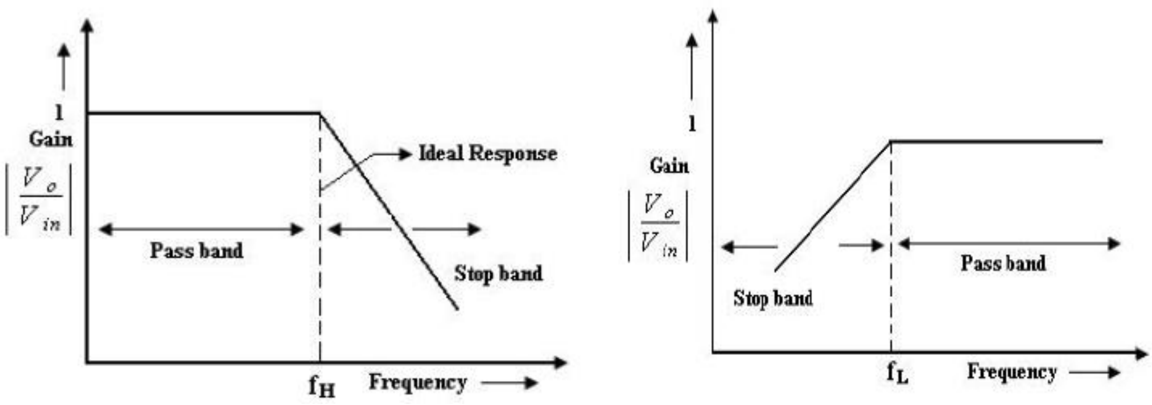


Fig 2.52 Frequency response of Low Pass filter and High pass Filter

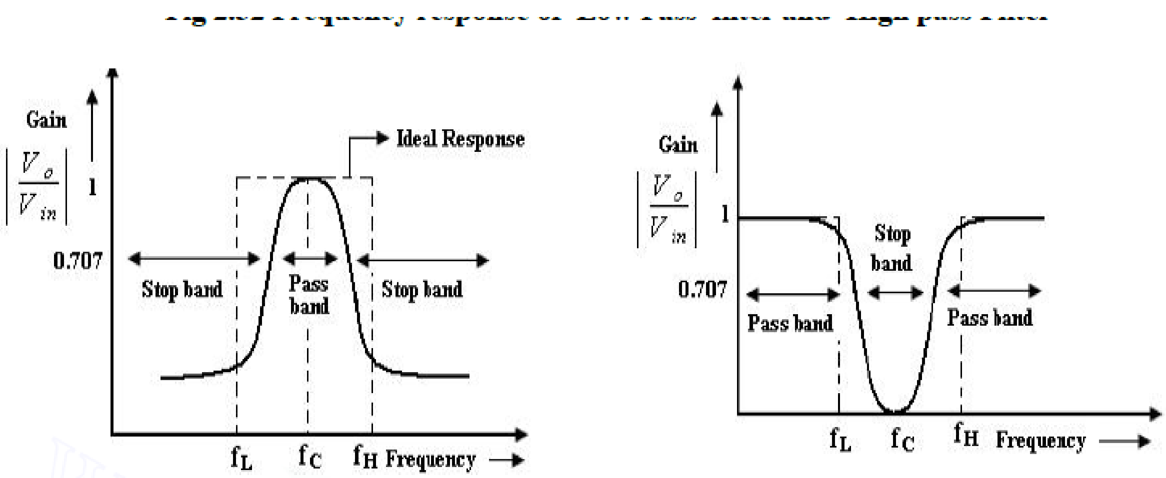


Fig 2.53 Frequency response of Band Pass filter and Band reject Filter

Low pass filters:

1. It has a constant gain from 0 Hz to a high cutoff frequency f1.
2. At fH the gain in down by 3db.
3. The frequency between 0 Hz and fH are known as the pass band frequencies where as the range of frequencies those beyond fH, that are attenuated includes the stop band frequencies.
4. Butterworth, Chebyshev and Cauer filter are some of the most commonly used practical filters.
5. The key characteristics of the butter worth filter are that it has a flat pass band as well as stop band. For this reason, it is sometimes called flat- flat filters.

6. Chebyshev filter -> has a ripple pass band & flat stop band.
7. Causer Filter -> has a ripple pass band & ripple stop band. It gives best stop band response among the three.

High pass filter:

High pass filter with a stop band 0 <f< f L and a pass band f> f L

fL -> low cut off frequency

f -> operating frequency.

Band pass filter:

It has a pass band between 2 cut off frequencies fH and fL where fH > fL and two, stop bands: 0<f< fL and f > fH between the band pass filter (equal to fH - fL.

Band –reject filter: (Band stop or Band elimination)

It performs exactly opposite to the band pass.

It has a band stop between 2 cut-off frequency fL and fH and 2 pass bands: 0<f< fL and f> fH

fC -> center frequency.

Note:

The actual response curves of the filters in the stop band either Ror S or both with Rin frequencies.

The rate at which the gain of the filter changes in the stop band is determined by the order of the filter.

Ex: 1st order low pass filter the gain rolls off at the rate of 20dB/decade in the stop band.

(i.e) for f > fH.

2nd order LPF -> the gain roll off rate is 40dB/decade.

1st order HPF -> the gain rolls off at the rate of 20dB (i.e.) until f:fL

2nd order HPF -> the gain rolls off at the rate of 40dB/decade

First order LPF Butterworth filter:

First order LPF that uses an RC for filtering op-amp is used in the non inverting configuration. Resistor R1 & Rf determine the gain of the filter. According to the voltage –divider rule, the voltage at the non-inverting terminal (across capacitor) C is,

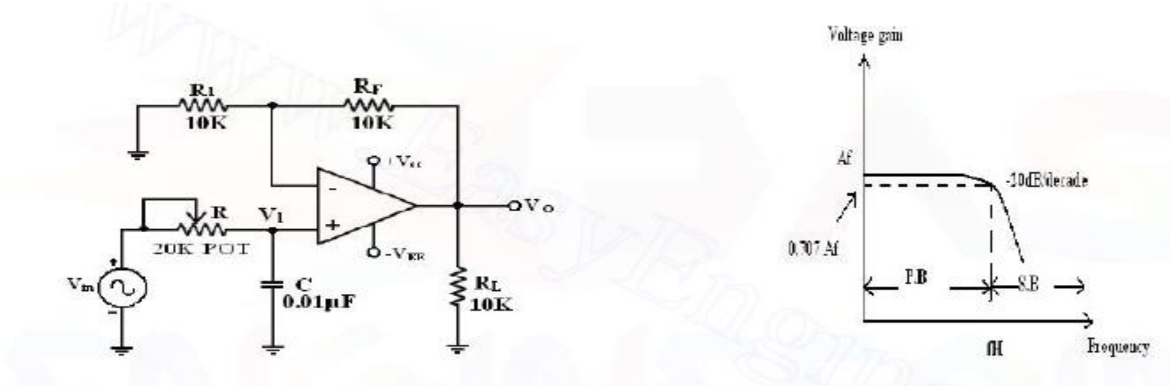


Fig. 2.54 First order LPF Butterworth filter

Gain A= $(1+R_f/R_1)$

Voltage across capacitor $V_1 = V_i / (1+j2\pi fRC)$

Output voltage V0 for non inverting amplifier $=AV_1$

$= (1+R_f/R_1)\ V_i/(1+j2\pi fRC)$

Overall gain V0/Vi = $(1+R_f/R_1)\ V_i/(1+j2\pi fRC$

Transfer function H(s) $=A/(jf/f_h+1)$ if $f_h = 1/2\pi RC$

H (jω) = A/(j RC+1) = A/(j RC+1).

The gain magnitude and phase angle of the equation of the LPF can be obtained by converting eqn. (1) b into its equivalent polar form as follows.

1. At very low frequency, f < fH

|H (jω)| =A

2. At f =fH

|H (jω)| =A/√2=0.707A

3. At f> fH

|H (jω)| <<A ≅ 0

When the frequency increases by tenfold (one decade), the volt gain is divided by 10. The gain falls by 20 dB (=20log10) each time the frequency is reduces by 10. Hence the rate at which the gain rolls off fH = 20 dB or 6dB/octave (twofold Rin frequency). The frequency f = fH is called the cut off frequency because the gain of the filter at this frequency is down by 3 dB (=20 log 0.707).

Filter design:

A LPF can be designed by implementing the following steps.

1. Choose a value of high cut off frequency fH.
2. Select a value of C less than or equal to 1μf.
3. Choose the value of R using $f_h=1/2\pi RC$
4. Finally select values of R1 and RF dependent on the desired pass band gain AF

Using A= (1+Rf/R1)

Second order LP Butterworth filter:

A second order LPF having a gain 40dB/decade in stop band. A First order LPF can be converted into a II order type simply by using an additional RC network.

The gain of the II order filter is set by R1 and RF, while the high cut off frequency fH is determined by R2, C2, R3 and C3.

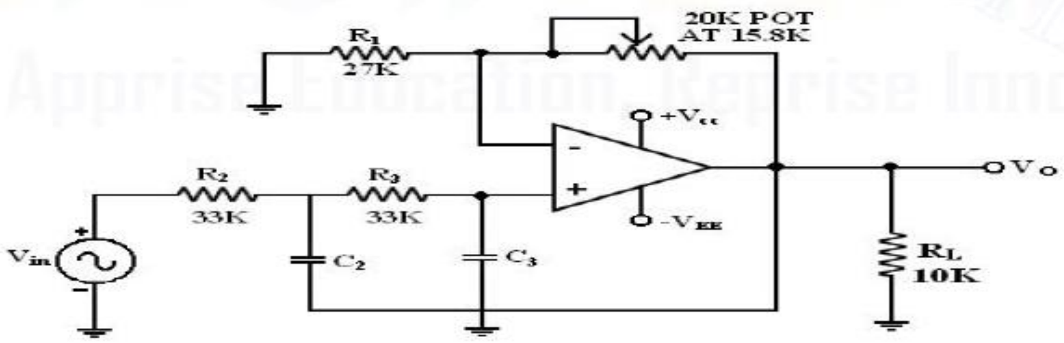


Fig. 2.55 second order LP Butterworth filter

Let $Y_1 = Y_2 = 1/R$, $Y_3 = sC_3$ and $Y_4 = sC_4$. Then the transfer function is

$$H(s) = \frac{\frac{1}{R^2}}{\frac{1}{R^2} + sC_4\left(\frac{2}{R} + sC_3\right)} = \frac{1}{1 + sRC_4\left(2 + sRC_3\right)}$$

Let the time constant $\tau_1 = RC_3$ and $\tau_2 = RC_4$. Substituting $s = j\omega$, we get

$$H(j\omega) = \frac{1}{1 + j\omega\tau_2(2 + j\omega\tau_1)} = \frac{1}{\left(1 - \omega^2\tau_1\right) + j\left(2\omega\tau_2\right)}$$

Therefore, its magnitude is

$$|H(j\omega)| = \left[\left(1 - \omega^2\tau_1\tau_2\right)^2 + \left(2\omega\tau_2\right)^2\right]^{-1/2}$$

A maximally flat Butterworth filter will have a minimum rate of change. Therefore,

$$\frac{d|H|}{d\omega}\bigg|_{\omega=0} = 0$$

Differentiating $|H(j\omega)|$, we obtain

$$\frac{d|H|}{d\omega} = -\frac{1}{2}\left[\left(1 - \omega^2\tau_1\tau_2\right)^2 + \left(2\omega\tau_2\right)^2\right]^{-3/2}\left[-4\omega\tau_1\tau_2\left(1 - \omega^2\tau_1\tau_2\right) + 8\omega\tau_2^2\right]$$

Letting the derivative to zero at $\omega = 0$, we get

$$\frac{d|H|}{d\omega}\bigg|_{\omega=0} = \left[-4\omega\tau_1\tau_2\left(1 - \omega^2\tau_1\tau_2\right) + 8\omega\tau_2^2\right]$$

$$= 4\omega\tau_2\left[-\tau_1\left(1 - \omega^2\tau_1\tau_2\right) + 2\tau_2\right]$$

The above equation is satisfied when $2\tau_2 = \tau_1$. That is, $C_3 = 2C_4$. Therefore the magnitude of the transfer function becomes

$$|H| = \frac{1}{\left[1 + 4\left(\omega\tau_2\right)^4\right]^{1/2}}$$

The cut-off frequency occurs when $|H| = \frac{1}{\sqrt{2}}$, or $4\left(\omega_{3dB}\tau_2\right)^4 = 1$. Therefore,

$$\omega_{3dB} = 2\pi f_{3dB} = \frac{1}{\tau_2\sqrt{2}} = \frac{1}{\sqrt{2}RC_4}$$

We know that the cut-off frequency is $\omega_H = \omega_{3dB} = \frac{1}{RC}$.

Comparing the above equations, we get

$$C_4 = 0.707C$$
$$C_3 = 1.414C$$

The magnitude of the voltage transfer function for the second order low-pass Butterworth filter is $\left|H(jf)\right| = \frac{1}{\sqrt{1 + \left(\frac{f}{f_H}\right)^4}}$

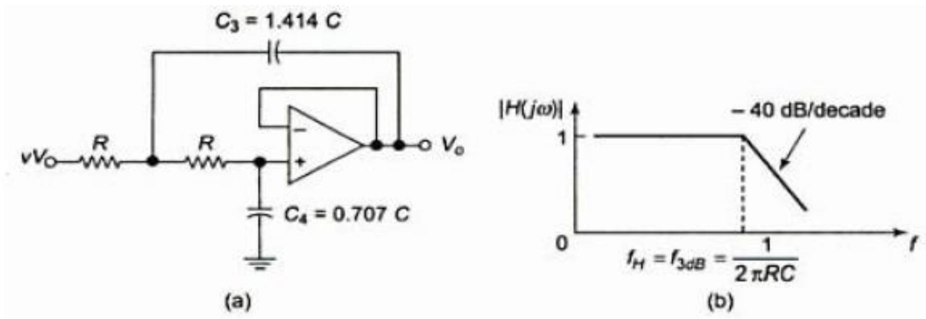


Fig. 2.56 Second order Low pass Butterworth and filter with unity gain and its transfer function

Filter Design:

1. Choose a value for a high cut off freq. (fH).

2. To simplify the design calculations, set R2 = R3 = R and C2 = C3 = C then choose a value of C<=1μf.

3. Calculate the value of R $R = 1/2\pi f_h C$

4. Finally, because of the equal resistor (R2 = R3) and capacitor (C2 = C3) values, the pass band volt gain AF = 1 + RF / R1 of the second order had to be = to 1.586. RF = 0.586 R1. Hence choose a value of R1 <=100kΩ.

5. Calculate the value of RF.

First order HP Butterworth filter:

High pass filters are often formed simply by interchanging frequency-determining resistors and capacitors in low-pass filters. (i.e) I order HPF is formed from a I order LPF by interchanging components R & C. Similarly II order HPF is formed from a II order LPF by interchanging R & C.

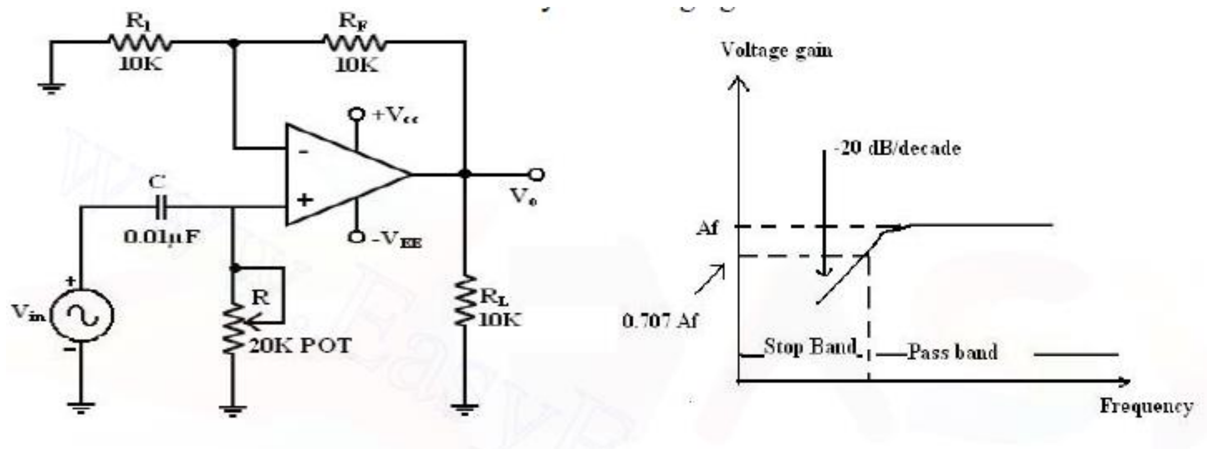


Fig. 2.57 I order HPF and its frequency response

Here I order HPF with a low cut off frequency of fL. This is the frequency at which the magnitude of the gain is 0.707 times its passband value. Here all the frequencies higher than fL are passband frequencies.

The output voltage V0 of the first order active high pass filter is

$$V_o = \left(1 + \frac{R_f}{R_i}\right) \frac{j2\pi fRC}{1 + j2\pi fRC} V_i$$

The gain of the filter:

$$\frac{V_o}{V_i} = A\left(\frac{j\left(\frac{f}{f_L}\right)}{1 + j\left(\frac{f}{f_L}\right)}\right)$$

Frequency response of the filter $|H(jf)| = \left|\frac{V_o}{V_i}\right| = \frac{A\left(\frac{f}{f_L}\right)}{\sqrt{1+\left(\frac{f}{f_L}\right)^2}} = \frac{A}{\sqrt{1-\left(\frac{f_L}{f}\right)^2}}$ **is**

- At high frequencies f>fL gain = A.
- At f= fL gain = 0.707 A.
- At f < fL the gain decreases at a rate of -20 db /decade. The frequency below cutoff frequency is stop band.

✓ Second – order High Pass Butterworth Filter:

I order Filter, II order HPF can be formed from a II order LPF by interchanging the frequency

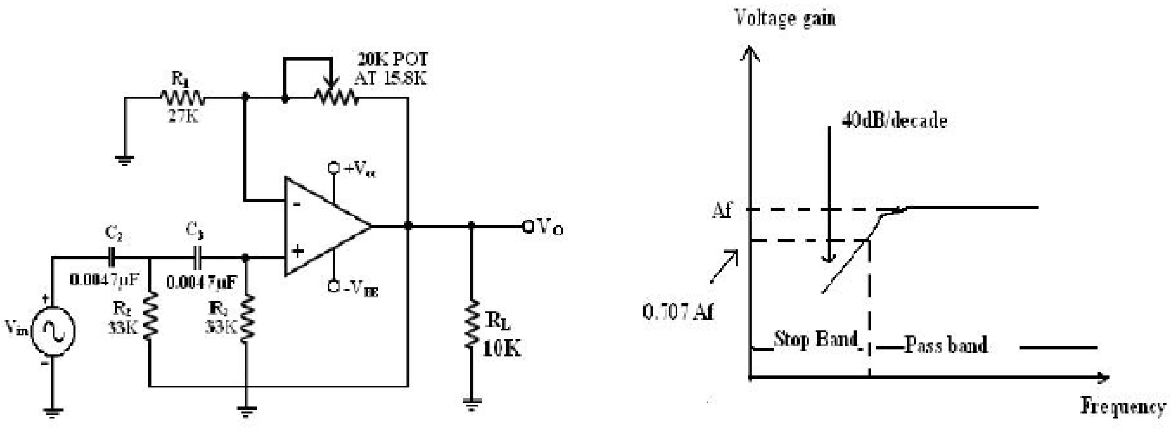


Fig. 2.58 II order HPF and its frequency response

2.20 Band pass filters

- Filters that pass band of frequencies and attenuates others. Its high cutoff frequency and low cutoff frequency are related as $f_H > f_L$ and maximum gain at resonant frequency

- $f_r = f_H f_L$
- Figure of merit Q= $f_r/(f_H - f_L) = f_r/B$ where B= bandwidth.
- 2 types of filters are Narrow band pass and wide band pass filters

Wide band pass filter:

It is connection of a low pass filter and a high pass filter in cascade. The f_H of low pass filter and f_L of high pass filter are related as $f_H > f_L$

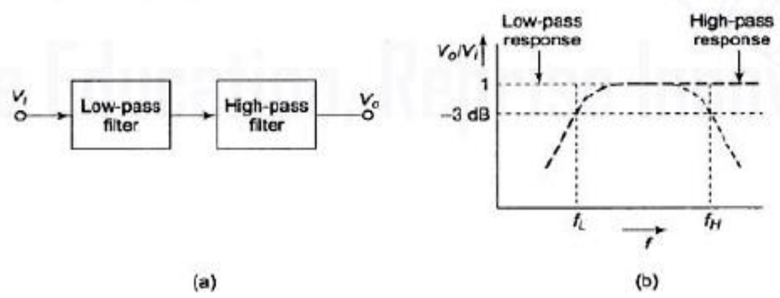


Fig. 2.59 (a) Wide band pass filter and (b) its frequency response