JEPPIAAR INSTITUTE OF TECHNOLOGY

"Self-Belief | Self Discipline | Self Respect"

DEPARTMENT

OF

ELECTRONICS AND COMMUNICATION ENGINEERING

LECTURE NOTES

EC8453 – LINEAR INTEGRATED CIRCUITS

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UNIT I BASICS OF OPERATIONAL AMPLIFIERS 9

Current mirror and current sources, Current sources as active loads, Voltage sources, Voltage References, BJT Differential amplifier with active loads, Basic information about op-amps – Ideal Operational Amplifier - General operational amplifier stages -and internal circuit diagrams of IC 741, DC and AC performance characteristics, slew rate, Open and closed loop configurations – JFET Operational Amplifiers – LF155 and TL082.

1.1 Constant current source (Current Mirror):

A constant current source makes use of the fact that for a transistor in the active mode of operation, the collector current is relatively independent of the collector vo

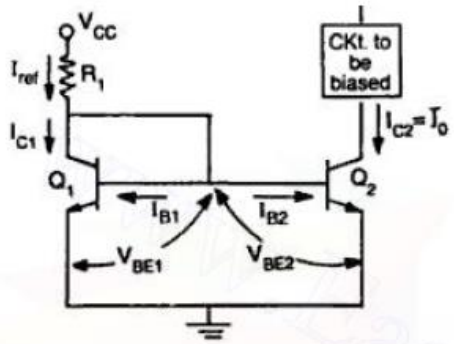

Fig. 1.1 Current mirror circuit

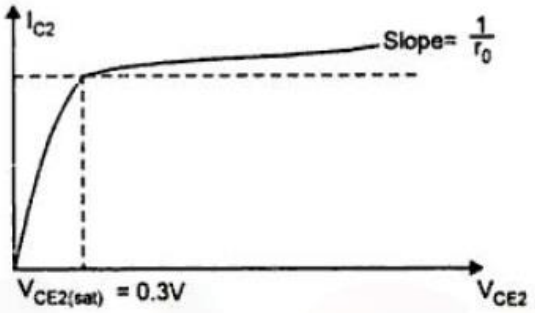

Fig 1.2 Current source output current characteristics

Transistors Q1&Q2 are matched as the circuit is fabricated using IC technology. Base and emitter of Q1& Q2 are tied together and thus have the same VBE. In addition, transistor Q1 is connected as a diode by shorting its collector to base. The input current Iref flows through the diode connected transistor Q1 and thus establishes a voltage across Q1. This voltage in turn appears between the base and emitter of Q2 .Since Q2 is identical to Q1, the emitter current of Q2 will be equal to emitter current of Q1 which is approximately equal to Iref. As long as Q2 is maintained in the active region ,its collector current IC2=Io will be approximately equal to Iref . Since the output current Io is a reflection or mirror of the reference current Iref, the circuit is often referred to as a current mirror.

Analysis:

The collector current IC1 and IC2 for the transistor Q1 and Q2 can be approximately expressed as

$$I_{C1(t)=\alpha} I_{ESe^{V_{BE1}/V_T}} \text{ ---------- (1)}$$

$$I_{C2(t)=\alpha} I_{ESe^{V_{BE2}/V_T}} \text{ ---------- (2)}$$

Where I_{ES} is reverse saturation current in emitter junction and V_T is temperature equivalent of voltage.

From equation (1) & (2)

Since $V_{BE1}=V_{BE2}$ we obtain $I_{C2}=I_{C1}=I\backslash_C=I_O$

Also since both the transistors are identical, $I_{C1}= I_{C2}$

KCL at the collector of Q1 gives

Iref = IC1+IB1+IB2

$$= I_{C1} + \frac{I_{C1}}{\beta} + \frac{I_{C2}}{\beta} = I_{C1} + 2\frac{I_{C1}}{\beta} \quad \text{When } I_{C1} = I_{C2} = I_C = I_o \text{ ---------- (4)}$$

Solving Eq (4)

$$I_{ref=}(V_{CC} - V_{BE(ON)})/R$$

$$I_{ref=}I_{C1} + 2\frac{I_{C1}}{\beta} = I_{C1}(1 + \frac{2}{\beta})$$

$$I_C = I_{C1} = I_{C2} = \frac{I_{ref}}{1+\frac{2}{\beta}} = \frac{\beta}{\beta+2}(V_{CC} - V_{BE(ON)})/R \text{ ---------- (5)}$$

$$I_0 = I_{ref}$$

From Eq.5 for β>>1, is almost unity and the output current I0 is equal to the reference current, ref which for a given R1 is constant. Typically Io varies by about 3% for 50 ≤ β ≤200. The circuit however operates as a constant current source as long as Q2 remains in the active region.

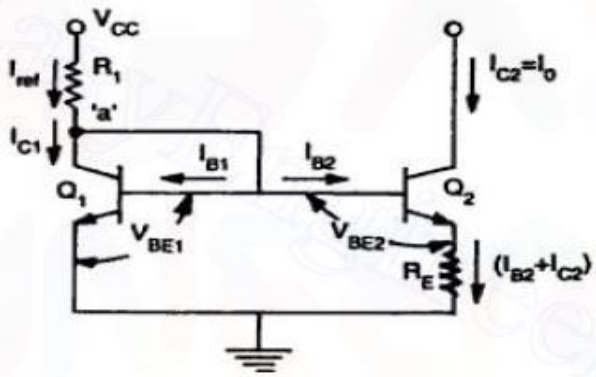

Fig.1.3 Simple current source

1.1.1 Widlar current source:

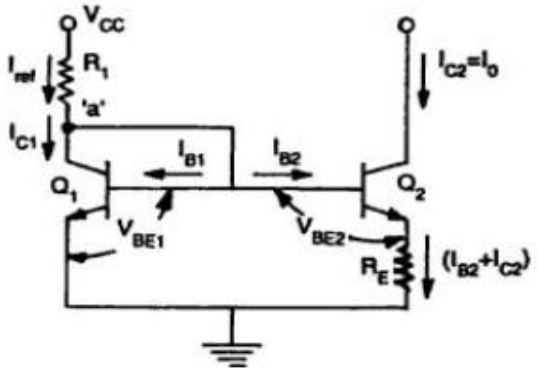

Fig.1.4 Widlar current source

Widlar current source which is particularly suitable for low value of currents. The circuit differs from the basic current mirror only in the resistance RE that is included in the emitter lead of Q2. It can be seen that due to RE the base-emitter voltage VBE2 is less than VBE1 and consequently current Io is smaller than IC1

The ratio of collector currents IC1&IC2 using

$$\frac{I_{C1}}{I_{C2}} = e^{\frac{V_{BE1}-V_{BE2}}{V_T}} \quad \text{(1)}$$

Taking natural logarithm of both sides, we get

$$V_{BE1} - V_{BE2} = V_T \ln \frac{I_{C1}}{I_{C2}} \quad \text{----- (2)}$$

Writing KVL for the emitter base loop

$$V_{BE1}=V_{BE2}+(I_{B2}+I_{C2})R_E \quad \text{----------(3)}$$

Or $$V_{BE1}-V_{BE2}=(1/\beta +1)I_{C2}R_E \quad \text{----------(4)}$$

From eqn. (2) & (4) we obtain

$$V_T \ln \frac{I_{C1}}{I_{C2}} = (1/\beta +1)\, I_{C2}R_E \quad \text{----------}$$

(5)

A relation between I_{C1} and the reference current I_{ref} is obtained by writing KCL at the collector point of Q1

$$I_{ref} = I_{C1}+I_{B1}+I_{B2}$$

$$I_{ref} = IC1 + IC1/\beta + IC2/\beta$$

Neglecting $IC2/\beta$,

$$I_{ref} = IC1(1 + \frac{1}{\beta})$$

$$I_{ref} = \frac{V_{cc}-V_{BE}}{R_1}$$

When $\beta >> 1$, $IC1 = I_{ref}$

1.1.2 Wilson current source:

The Wilson current source shown in figure

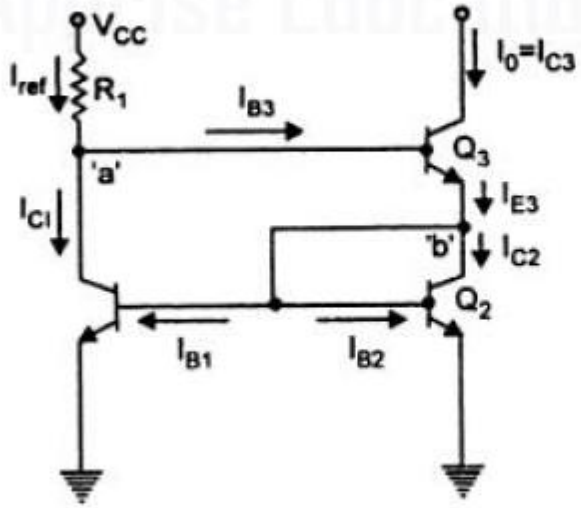

Fig.1.5 Wilson current source

It provides an output current I_0 which is very nearly equal to V_{ref} and also exhibits a very high output resistance.

Analysis:

Since $V_{BE1}=V_{BE2}$

$I_{C1}=I_{C2}$ and $I_{B1}=I_{B2}=I_B$

At node 'b'

$I_{E3}=2I_B+I_{C2}=(\frac{2}{\beta}+1)I_{C2}$ ---------- (1)

I_{E3} is equal to

$I_{E3}=I_{C3}+I_{B3}=I_{C3}(1+1/\beta)$ ---------- (2)

From (1) and (2)

$I_{C3}(1+1/\beta)=I_{C2}(1+2/\beta)$

From Eqn. (1) & (2) we obtain

$I_{C3}-I_O=I_{C2}(\beta\ 2)/(\beta+1)=I_{C1}(\beta\ 2)/(\beta+1)$ Since $I_{C1}=I_{C2}$

At node 'a' $I_{ref}=I_{C1}+I_{B3}=\frac{\beta+1}{\beta+2}I_O+\frac{I_O}{\beta}=$

$I_{ref}=\frac{\beta^2+2\beta+2}{\beta^2+2\beta}I_O$ and $I_{ref}=\frac{V_{cc}-2V_{BE}}{R_1}$; $I_O-I_{ref}=\frac{2}{\beta^2+2\beta+2}$ I ref is very small for modest β.

But output resistance is greater than Widlar source.

1.2 Current sources as Active loads

The current source can be used as an active load in both analog and digital IC's. The active load realized using current source in place of the passive load (i.e. a resistor) in the collector arm of differential amplifier makes it possible to achieve high voltage gain without requiring large power supply voltage. The active load so achieved is basically R0 of a PNP transistor.

1.3 Voltage Sources

A voltage source is a circuit that produces an output voltage V_0, which is independent of the load driven by the voltage source, or the output current supplied to the load. The voltage source is the circuit dual of the constant current source.

A number of IC applications require a voltage reference point with very low ac impedance and a stable dc voltage that is not affected by power supply and temperature variations. There are two methods which can be used to produce a voltage source, namely,

1. Using the impedance transforming properties of the transistor, which in turn determines the current gain of the transistor and

2. Using an amplifier with negative feedback.

1.3.1 Voltage source circuit using Impedance transformation:

The voltage source circuit using the impedance transforming property of the transistor is shown in figure. The source voltage Vs drives the base of the transistor through a series resistance RS and the output is taken across the emitter. From the circuit, the output ac resistance looking Into emitter is given by

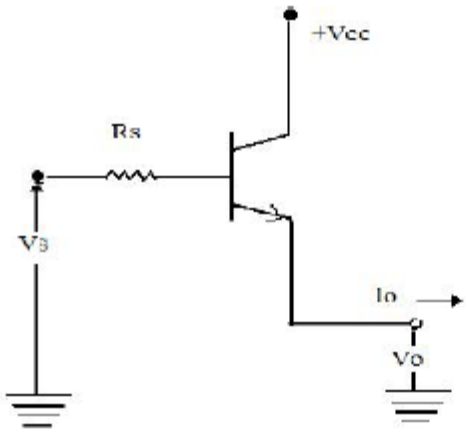

Fig.1.6 Voltage source circuit using Impedance transformation:

$$\frac{d_\vartheta}{dI_o} = R_0 = \frac{R_S}{\beta+1} + r_{eb} \;;$$

With $\beta >> 100$, $R_0 = \frac{R_S}{\beta+1}$

It is to be noted that, equation is applicable only for small changes in the output current. The load regulation parameter indicates the changes in V_0 resulting from large changes in output current I_0 , Reduction in V_0 occurs as I_0 goes from no-load current to full-load current and this factor determines the output impedance of the voltage sources.

1.3.2 Emitter– follower or Common Collector Type Voltage source:

The figure shows an emitter follower or common collector type voltage source.

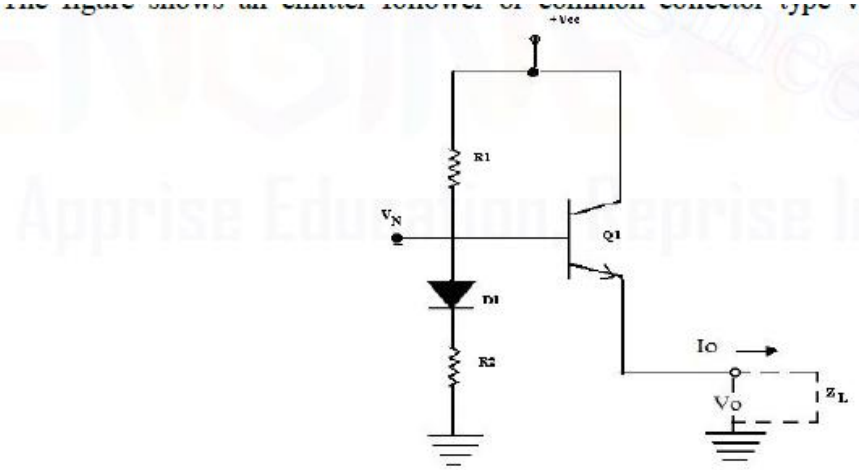

Fig.1.7 Emitter– follower or Common Collector Type Voltage source

This voltage source is suitable for the differential gain stage used in op-amps. This circuit has the advantages of

1. Producing low ac impedance and
2. Resulting in effective decoupling of adjacent gain stages.

The low output impedance of the common-collector stage simulates a low impedance voltage source with an output voltage level of V0 represented by

$$V_0 = V_{CC}\frac{R_2}{R_1 + R_2}$$

The diode D1 is used for offsetting the effect of dc value VBE , across the E-B junction of the transistor, and for compensating the temperature dependence of VBE drop of Q1. The load ZL shown in dotted line represents the circuit biased by the current through Q1. The impedance R0 looking into the emitter of Q1 derived from the hybrid π model is given by

$$R_o = \frac{V_T}{I_1} + \frac{R_1 R_2}{\beta(R_1+R_2)}$$

1.3.3 Voltage Source Using Temperature compensated Avalanche Diode

The voltage source using common collector stage has the limitations of its vulnerability for changes in bias voltage VN and the output voltage V0 with respect to changes in supply voltage Vcc. This is overcome in the voltage source circuit using the breakdown voltage of the base-emitter junction shown below. The emitter – follower stage of common – collector is eliminated

in this circuit, since the impedance seen looking into the bias terminal N is very low. The current source I1 is normally

simulated by a resistor connected between Vcc and node n. Then, the output voltage level V0 at node N is given by V0 = VB +VBE Where VB is the breakdown voltage of diode DB and VBE is the diode drop across D1. The breakdown diode DB is normally realized using the base-emitter junction of the transistor. The diode D1 provides partial compensation for the positive temperature coefficient effect of VB. In a monolithic IC structure, DB and D1 can be conveniently realized as a single

transistor with two individual emitters as shown in figure. transistor. The diode D1 provides partial compensation for the positive temperature coefficient effect of VB. In a monolithic IC structure, DB and D1 can be conveniently realized as a single

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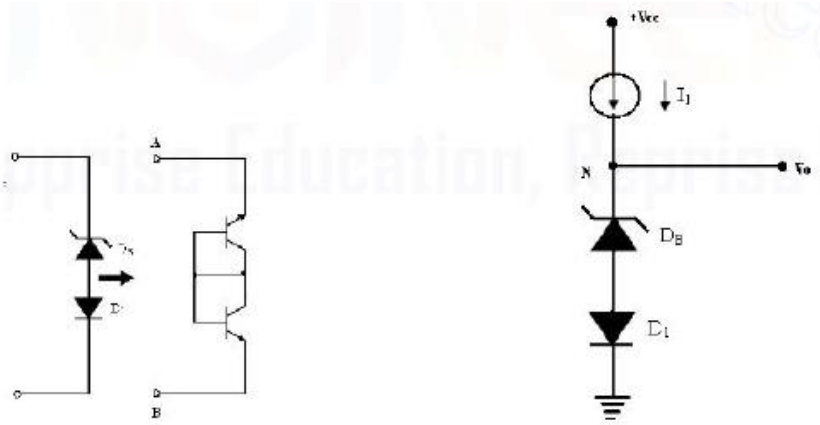


Fig.1.8 Temperature Compensated avalanche diode

1.3.4 Voltage source using breakdown voltage of the base- emitter junction

The structure consists of composite connection of two transistors which are diode connected back-to back. Since the transistors have their base to collector terminals common, they can be designed as a single transistor with two emitters.

The output resistance R0 looking into the output terminal in figure is given by $R_o=R_B+V_T/I_1$ where RB and VT /I1 are the ac resistances of the base–emitter resistance of diode D_B and D_1 respectively. Typically RB is in the range of 40Ω to 100Ω, and V0 in the range of 6.5V to 9V.

1.3.5 Voltage Source using VBE as a reference:

The output stage of op-amp requires stabilized bias voltage source, which can be obtained using a forward-biased diode connected transistor. The forward voltage drop for such a connection is approximately 0.7V, and it changes slightly with current. When a voltage level greater than 0.7V, is needed, several diodes can be connected in series, which can offer integral multiples of 0.7V. Alternatively, the figure shows a multiplier circuit, which can offer voltage levels that need not be integral multiplied of 0.7V. The drop across R2 equals VBE drop of Q1. Considering negligible base current for Q1, current through R2 is thesame as that flowing through R1.

Therefore, the output voltage V0 can be expressed as

$$V_0 = I_2(R_1 + R_2) = \frac{V_{BE}}{R_2}(R_1 + R_2) = V_{BE}(\frac{R_1}{R_2} + 1)$$

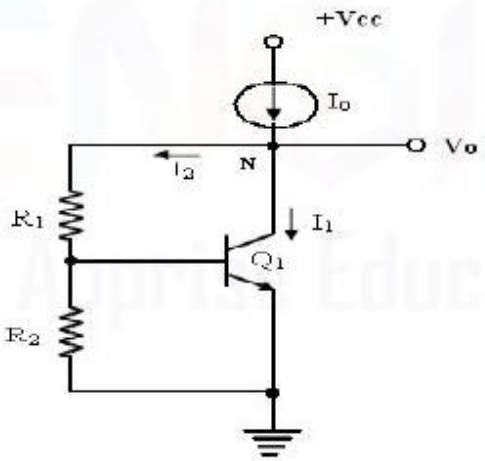


Fig.1.9 VBE multiplier Circuit

Hence, the voltage V_0 can be any multiple of V_{BE} by properly selecting the resistors R_1 and R_2. Due to the shunt feedback provided by R_1, the transistor current I1 automatically adjusts itself, towards maintaining I_2 and V_0 relatively independent of the changes in supply voltage. The ac output resistance of the circuit R_0 is given by,

$$R_O = \frac{dV_0}{dI_o} = \frac{R_1+R_2}{1+g_m R_2} \approx \frac{(R_1+R_2)}{R_2 g_m} \quad \text{When } g_m R_2 >> 1$$

$$R_O = \frac{V_0}{V_{BE}} \frac{1}{g_m} = \frac{V_O}{V_{BE}} \frac{V_1}{ic} \quad \text{as } \frac{V_O}{V_{BE}} = \frac{(R_1+R_2)}{R_2}$$

1.4 Voltage References

The circuit that is primarily designed for providing a constant voltage independent of changes in temperature is called a voltage reference. The most important characteristic of a voltage reference is the temperature coefficient of the output reference voltage T_{CR}, and it is expressed as

$$T_{CR} = \frac{dV_R}{dT}$$

The desirable properties of a voltage reference are:

1. Reference voltage must be independent of any temperature change.
2. Reference voltage must have good power supply rejection which is as independent of the supply voltage as possible and
3. Output voltage must be as independent of the loading of output current as possible, or in other words, the circuit should have low output impedance.

The voltage reference circuit is used to bias the voltage source circuit, and the combination can be called as the voltage regulator. The basic design strategy is producing a zero TCR at a given temperature, and thereby achieving good thermal ability. Temperature stability of the order 100ppm/0 C is typically expected.

1.4.1 Voltage Reference circuit using temperature compensation scheme

The voltage reference circuit using basic temperature compensation scheme is shown below. This design utilizes the close thermal coupling achievable among the monolithic components and this technique compensates the known thermal drifts by introducing an opposing and compensating drift source of equal magnitude.

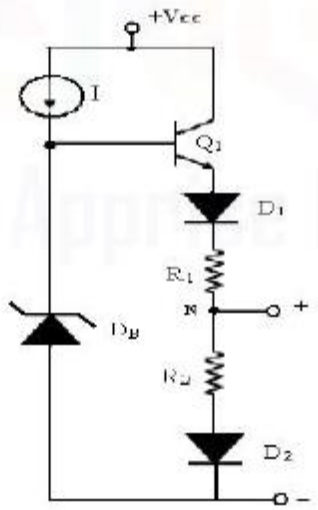


Fig.1.10 Voltage reference circuit using temperature compensation scheme

A constant current I is supplied to the avalanche diode D_B and it provides a bias voltage of V_B to the base of Q_1. The temperature dependence of the V_{BE} drop across Q_1 and those across D_1 and D_2 results in respective temperature coefficients. Hence, with the use of resistors R_1 and R_2 with tapping across them at point N compensates for the temperature drifts in the base emitter loop of Q_1. This results in generating a voltage reference V_R with normally zero temperature coefficient.

Explain supply independent biasing using zener-referenced bias circuit. Also, design a temperature compensated zener-reference source.

1.4.2 Voltage Reference circuit using Avalanche Diode Reference:

A voltage reference can be implemented using the breakdown phenomenon condition of a heavily doped PN junction. The Zener breakdown is the main mechanism for junctions, which breakdown at a voltage of 5V or less. For integrated transistors, the base-emitter breakdown voltage falls in the range of 6 to 8V. Therefore, the breakdown in the junctions of the integrated transistor is primarily due to avalanche multiplication. The avalanche breakdown voltage VB of a transistor

incurs a positive temperature coefficient, typically in the range of 2mV/0 C to 5mV/0 C.

Figure depicts a current reference circuit using avalanche diode reference. The base bias for transistor Q1 is provided through register R1 and it also provides the dc current needed to bias DB, D1 and D2 .The voltage at the base of Q1 is equal to the Zener voltage VB added with

two diode drops due to D1 and D2. The voltage across R2 is equal to the voltage at the base of Q1 less the sum of the base – emitter voltages of Q1 and Q2.

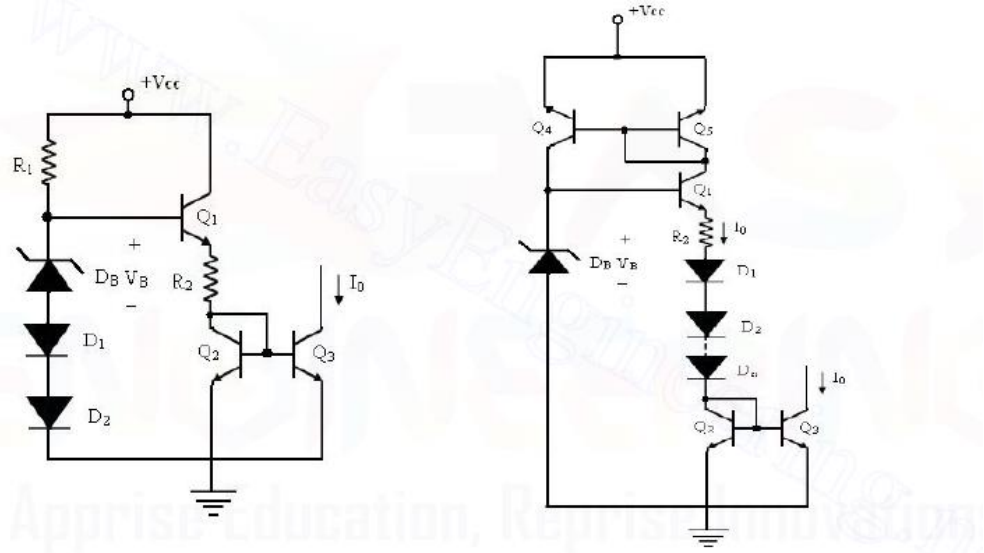


Fig. 1.11 Voltage reference using avalanche diodes and temperature compensated

Hence, the voltage across R2 is approximately equal to that across DB = VB. Since Q2 and Q3 act as a current mirror circuit, current I0 equals the current through R2.

$$I_O = \frac{V_B}{R_2}$$

It shows that, the output current I0 has low temperature coefficient, if the temperature coefficient of R2 is low, such as that produced by a diffused resistor in IC fabrication. The zero temperature coefficients for output current can be achieved, if diodes are added in series with R2, so that they can compensate for the temperature variation of R2 and VB. The temperature compensated avalanche diode reference source circuit is shown in figure. The transistor Q4 and Q5 form an active load current mirror circuit. The base voltage of Q1 is the voltage VB across Zener DB.

Then, $V_B = (V_{BE} * n) + V_{BE}$ across $Q_1 + V_{BE}$ across Q_2 + drop across R_2. Here, n is the number of diodes.

It can be expressed as $V_B = (n+2)\ V_{BE} + I_0 * R_2$

Differentiating for V_B, I_0, R_2 and V_{BE} partially, with respect to temperature T, we get

$$\frac{\partial V_B}{\partial T} = n + 2\frac{\partial V_{BE}}{\partial T} + R_2\frac{\partial I_0}{\partial T} + I_0\frac{\partial R_2}{\partial T}$$

Dividing throughout by $I_0 R_2$, we get

$$\frac{I}{I_O}\frac{\partial I_O}{\partial T} = 0 = \frac{1}{R_2 I_0}\left[\frac{\partial V_B}{\partial T} - (n+2)\frac{\partial V_{BE}}{\partial T} - \frac{1}{R_2}\frac{\partial R_2}{\partial T}\right.$$

Therefore, zero temperature coefficient of I0 can be obtained, if the above condition is satisfied.

Design an active load for an emitter-coupled pair (differential amplifier) and perform a detailed analysis to find its differential mode gain and the output resistance.

1.5 Differential amplifier

The function of a differential amplifier is to amplify the difference between two signals. The need for differential amplifier arises in many physical measurements where response from DC to many MHz of frequency is required. This forms the basic input stage of an integrated amplifier. The basic differential amplifier has the following important properties of

Excellent stability

High versatility and

High immunity to interference signals

The differential amplifier as a building block of the op-amp has the advantages of

Lower cost

Easier fabrication as IC component and

closely matched components.

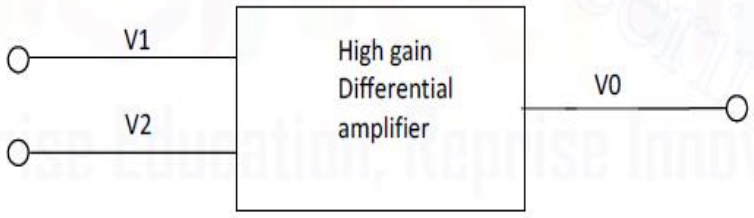


Fig. 1.12 Block diagram of Differential amplifier

The above figure shows the basic block diagram of a differential amplifier, with two input terminals and one output terminal. The output signal of the differential amplifier is proportional to the difference between the two input signals.

$$V0 = Adm\ (V1 - V2\ )$$

If V1 = V2, then the output voltage is zero. A non-zero output voltage V0 is obtained when V1 and V2 are not equal. The difference mode input voltage is defined as Vm = V1 – V2 and the common mode input voltage is defined as

$$V_{CM} = \frac{V1+V2}{2}$$

These equation show that if V1 = V2, then the differential mode input signal is zero and common mode input signal is Vcm = V1 =V2.

1.5.1 Differential Amplifier with Active load:

Differential amplifier is designed with active loads to increase the differential mode voltage gain. The open circuit voltage gain of an op-amp is needed to be as large as possible. This is got by cascading the gain stages which increase the phase shift and the amplifier also becomes vulnerable to oscillations. The gain can be increased by using large values of collector resistance. For such a circuit, the voltage gain is given by

Adm = gm RC

To increase the gain the IC RC product must be made very large. However, there are limitations in IC fabrication such as,

1. A large value of resistance needs a large chip area.

2. For large RC, the quiescent drop across the resistor increase and a large power supply will be required to maintain a given operating current.

3. Large monolithic resistor introduces large parasitic capacitances which limits the frequency response of the amplifier.

4. for linear operation of the differential pair, the devices should not be allowed to enter into saturation. This limits the max input voltage that can be applied to the bases of transistors Q1 and Q2 the base-collector junction must be allowed to become forward-biased by more than 0.5V. The large value of load resistance produces a large dc voltage drop (IEE / 2) RC, so that the collector voltage will be VC=Vcc - (IEE/2) RC and it will be substantially less than the supply voltage Vcc. This will reduce the input voltage range of the differential amplifier. Due to the reasons cited above, an active load is preferred in the differential amplifier configurations.

✓ BJT Differential Amplifier using active loads:

A simple active load circuit for a differential amplifier is the current mirror active load as shown in figure. The active load comprises of transistors Q3 and Q4 with the transistor Q3 connected as a Diode with its base and collector shorted. The circuit is shown to drive a load RL. When an ac input voltage is applied to the differential amplifier, the various currents of the circuit are given by

$I_{C4} = I_{C3} = I_{C1} = g_m V_{id}/2$ where $I_{C4} = I_{C3}$ due to current mirror action.

$I_{C2} = - g_m V_{id}/2$.

We know that the load current I_L entering the next stage is

$I_L = I_{C2} - I_{C4} = - g_m V_{id}/2 - g_m V_{id}/2 = - g_m V_{id}$

Then, the output voltage from the differential amplifier is given by $V_0 = - I_L R_L = g_m R_L V_{id}$.

The ac voltage gain of the circuit is given by

$$A_V = \frac{V_0}{V_{id}} = g_m R_L$$

The amplifier can amplify the differential input signals and it provides single-ended output with a ground reference since the load RL is connected to only one output terminal. This is made possible by the use of the current mirror active load. The output resistance R_0 of the circuit is that offered by the parallel combination of

transistors Q2 (NPN) and Q4 (PNP). It is given by $R_r = r_{02} \| r_{04}$.

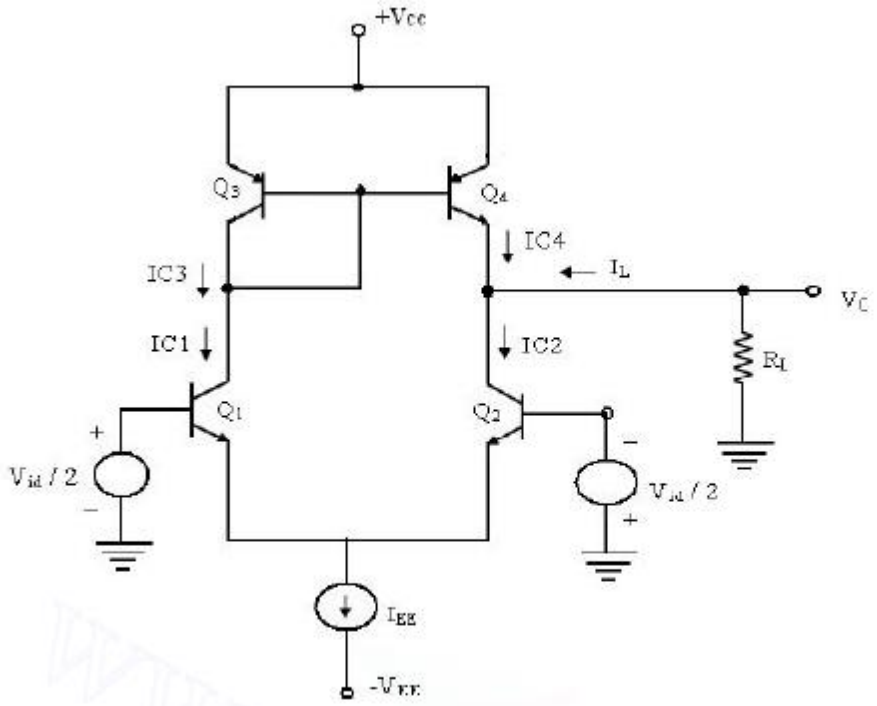


Fig. 1.13 BJT differential amplifier with current mirror active load

Analysis of BJT differential amplifier with active load:

The collector currents of all the transistors are equal.

$$I_{C1} = I_{C2} = I_{C3} = I_{C4} = I_{EE}/2 .$$

The Collector -emitter voltages of Q_1 and Q_2 are given by

$$V_{CE1}\text{-}V_{CE2} = V_C\text{-}V_E = V_{CC} - V_{EB}\text{-}(\text{-}V_{EB}) = V_{CC}$$

Eqn. shows that, the offset is higher than that of a resistive loaded differential amplifier A. This can be reduced by the use of emitter resistors for Q_3 and Q_4, and a transistor Q_5 in the current mirror load.

✓ CMRR of the differential amplifier using active load:

The differential amplifier using active load provides high voltage gain to the differential input signal and a single – ended output that is referenced to the ground is obtained. The differential amplifier which provides conversion for a differential signal to a single ended signal is necessary in differential input signal ended output amplifiers. The op-amp is one such circuit. The changes in the common-mode signal of the bias current source. This induces a change in IC2 and an identical change in IC1. The change in IC1 will then produce a change in the PNP load devices,

and thereby a change in IC4, which is the collector current Q4, The current IC4 is in such a direction as to cancel the change in IC2. As a result of this, any common mode input does not cause a change in output.

The voltage gain of the differential amplifier is independent of the quiescent current IEE. This makes it possible to use very small value of IEE as low as 20μA, while still maintaining a large voltage gain. Small value of IEE is preferred, since it results in a small value of bias current and a large value for the input resistance. A limitation in choosing a small IEE is, however, the fact that, it will result in a poor frequency response of the amplifier.

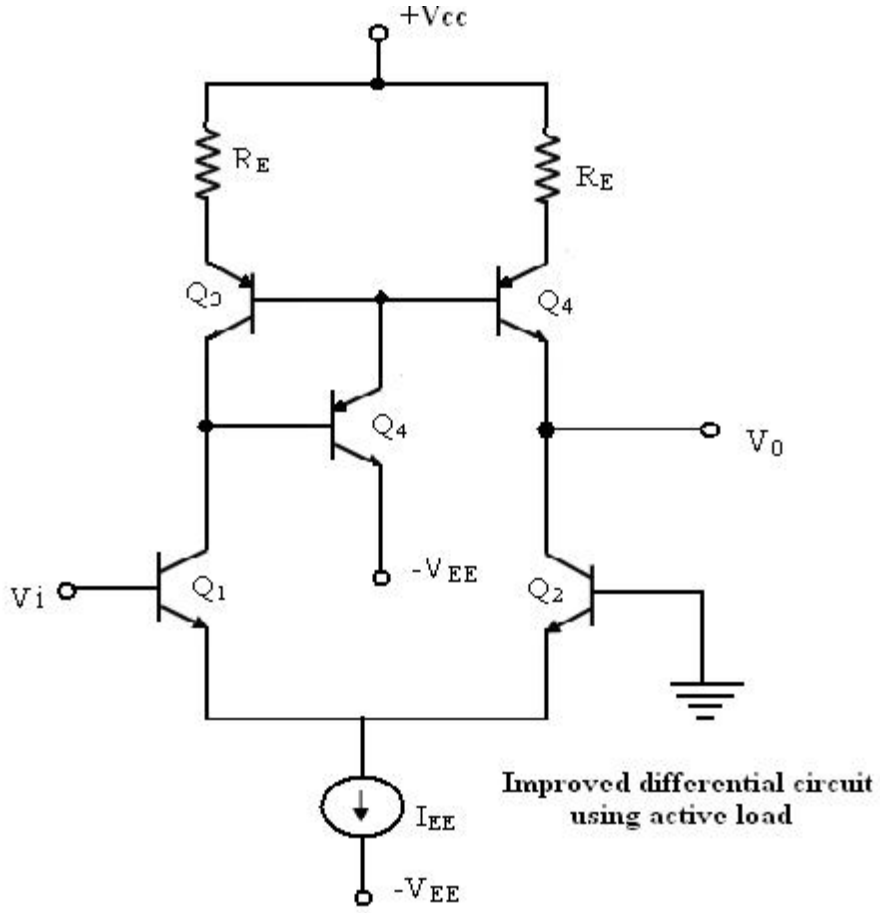


Fig.1.14. Improved differential circuit using active load

Fig.1.14. Improved differential circuit using active load

When a small value of bias current is required, the best approach is to use a JFET or MOSFET differential amplifier that is operated at comparatively higher values of I_{EE}.

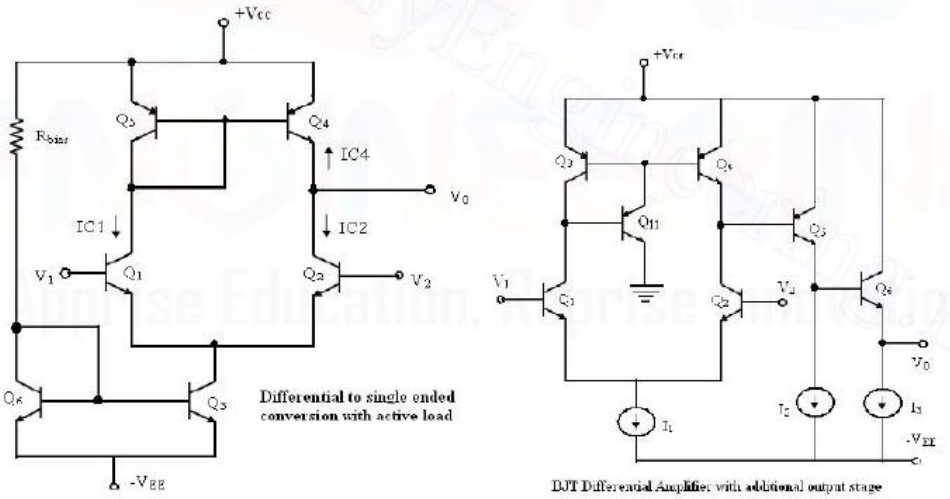


Fig.1.15. Differential to single ended conversion and output stage

Differential Mode signal analysis:

The ac analysis of the differential amplifier can be made using the circuit model as shown below. The differential input transistor pair produces equal and opposite currents whose amplitude us given by gm2 V_{id} /2 at the collector of Q_1 and Q_2. The collector current I_{c1} is fed by the transistor Q3 and it is mirrored at the output of Q_4. Therefore, the total current i0 flowing through the load resistor R_L is given by

$$i_0 = \frac{2g_{m2}V_{id}}{2} = g_{m2}V_{id}.$$

Then the output voltage is $v_0 = i_0 R_L = g_{m2} R_L v_{id}$ and the differential mode gain Ad of differential amplifier is

$$A_{dm} = \frac{v_0}{v_{dm}} = g_{m2} R_L$$

This current mirror provides a single ended output which has a voltage equal to the maximum gain of the common emitter amplifier.

The power of the current mirror can be increased by including additional common collec stages at the o/p of the differential input stage. A bipolar differential amplifier structure w additional stages is shown in figure. The resistance at the output of the differential stage is n given by the parallel combination of transistors Q2 and Q4 and the input resistance is offered Q5. Then, the equivalent resistance is expressed by $R_{eq} = r_{o2} \parallel r_{04} \parallel r_{i5} = r_{i5}$.

The gain of the differential stage then becomes $A_{dm} = g_m 2 R_{eq} = g_{m2} r_{i5} = \beta I_{C2}/I_{C5}$.

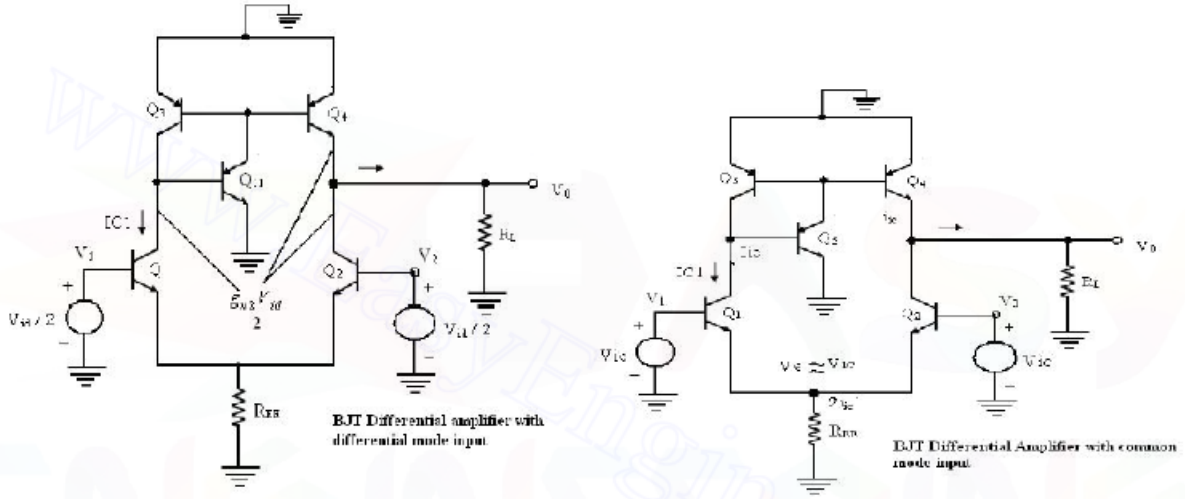


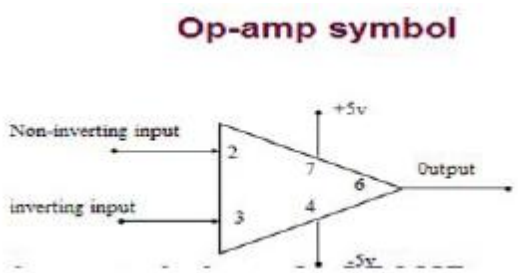
Fig. 1.16 Differentail amplifier with differential mode input and common mode input

1.6 Basic information about operational amplifiers

An operational amplifier is a direct coupled high gain amplifier consisting of one or more differential amplifiers, followed by a level translator and an output stage.

It is a versatile device that can be used to amplify ac as well as dc input signals & designed for computing mathematical functions such as addition, subtraction ,multiplication, integration & differentiation

1.7 Ideal operational Amplifiers



Ideal op-amp characteristics:

✓ Infinite voltage gain A.

✓ Infinite input resistance Ri, so that almost any signal source can drive it and there is no loading of the proceeding stage.

✓ Zero output resistance Ro, so that the output can drive an infinite number of other devices.

✓ Zero output voltage, when input voltage is zero.

✓ Infinite bandwidth, so that any frequency signals from o to ∞ HZ can be amplified with out attenuation.

✓ Infinite common mode rejection ratio, so that the output common mode noise voltage is zero.

✓ Infinite slew rate, so that output voltage changes occur simultaneously with input voltage changes.

Explain the stages of General Operational Amplifier and internal circuit diagrams of IC 741.

Explain the internal circuit diagram of IC 741. Discuss its AC and DC performance characteristics. (16) (May/ June 2014)

1.8 General Operational Amplifier stages and internal circuit diagrams of IC 741

An operational amplifier generally consists of three stages, namely

1. A differential amplifier
2. Additional amplifier stages to provide the required voltage gain and dc level shifting.
3. An emitter-follower or source follower output stage to provide current gain and low output resistance.

A low-frequency or dc gain of approximately 104 is desired for a general purpose op-amp and hence, the use of active load is preferred in the internal circuitry of op-amp.

The output voltage is required to be at ground, when the differential input voltages are zero, and this necessitates the use of dual polarity supply voltage. Since the output resistance of op-amp is required to be low, a complementary push-pull emitter – follower or source follower output stage is employed. Moreover, as the input bias currents are to be very small of the order of pico amperes, an FET input stage is normally preferred.

Input stage:

The input differential amplifier stage uses p-channel JFETs M1 and M2. It employs a three transistor active load formed by Q3, Q4, and Q5. The bias current for the stage is provided by a two-transistor current source using PNP transistors Q6 and Q7. Resistor R1 increases the output resistance seen looking into the collector of Q4 as indicated by R04. This is necessary to provide bias current stability against the transistor parameter variations. Resistor R2 establishes a definite bias current through Q5. A single ended output is taken out at the collector of Q4.

MOSFET‘s are used in place of JFETs with additional devices in the circuit to prevent any damage for the gate oxide due to electrostatic discharges.

Gain stage:

The second stage or the gain stage uses Darlington transistor pair formed by Q8 and Q9 as shown in figure. The transistor Q8 is connected as an emitter follower, providing large input resistance.

Therefore, it minimizes the loading effect on the input differential amplifier stage. The transistor Q9 provides an additional gain and Q10 acts as an active load for this stage. The current mirror formed by Q7 and Q10 establishes the bias current for Q9. The VBE drop across Q9 and drop across R5 constitute the voltage drop across R4, and this voltage sets the current through Q8. It can be set to a small value, such that the base current of Q8 also is very less.

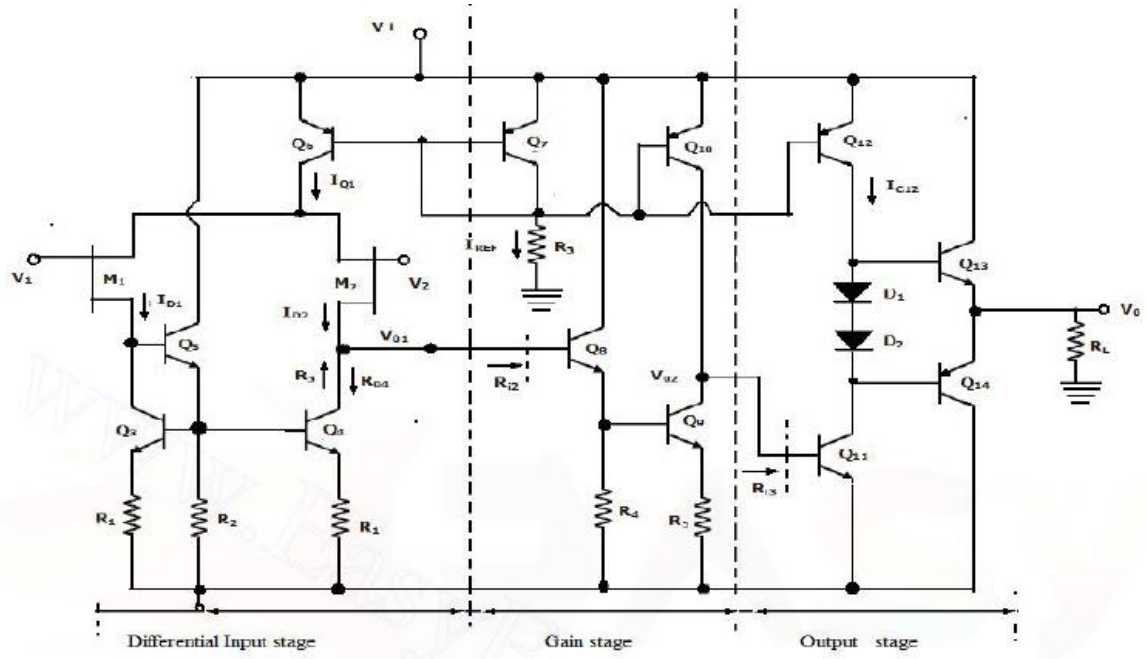


Fig. 1.17 Internal stages of Op-amp

Output stage:

The final stage of the op-amp is a class AB complementary push-pull output stage. Q11 is an emitter follower, providing a large input resistance for minimizing the loading effects on the gain stage. Bias current for Q11 is provided by the current mirror formed by Q7 and Q12, through Q13 and Q14 for minimizing the cross over distortion. Transistors can also be used in place of the two diodes.

The overall voltage gain AV of the op-amp is the product of voltage gain of each stage as given by AV=|Ad| |A2||A3| Where Ad is the gain of the differential amplifier stage, A2 is the gain of the second gain stage and A3 is the gain of the output stage.

IC 741 Bipolar operational amplifier:

The IC 741 produced since 1966 by several manufactures is a widely used general purpose operational amplifier. Figure shows that equivalent circuit of the 741 op-amp, divided into various individual stages. The op-amp circuit consists of three stages.

1. The input differential amplifier
2. The gain stage
3. the output stage.

A bias circuit is used to establish the bias current for whole of the circuit in the IC. The op-amp is supplied with positive and negative supply voltages of value ± 15V and the supply voltages as low as ±5V can also be used.

Bias Circuit:

The reference bias current IREF for the 741 circuit is established by the bias circuit consisting of two diodes-connected transistors Q11 and Q12 and resistor R5. The Widlar current source formed by Q11, Q10 and R4 provide bias current for the differential amplifier stage at the collector of Q10. Transistors Q8 and Q9 form another current mirror providing bias current for the differential amplifier. The reference bias current IREF also provides mirrored and proportional current at the collector of the double –collector lateral PNP transistor Q13. The transistor Q13 and Q12 thus form a two-output current mirror with Q13A providing bias current for

output stage and Q13B providing bias current for Q17. The transistor Q18 and Q19 provide dc bias for the output stage. Formed by Q14 and Q20 and they establish two VBE drops of potential difference between the bases of Q14 and Q18.

Input stage:

The input differential amplifier stage consists of transistors Q1 through Q7 with biasing provided by Q8 through Q12. The transistor Q1 and Q2 form emitter – followers contributing to high differential input resistance, and whose output currents are inputs to the common base amplifier using Q3 and Q4 which offers a large voltage gain. The transistors Q5, Q6 and Q7 along with resistors R1, R2 and R3 from the active load for input stage. The single-ended output is available

at the collector of Q6. The two null terminals in the input stage facilitate the null adjustment. The lateral PNP transistors Q3 and Q4 provide additional protection against voltage breakdown conditions. The emitter-base junction Q3 and Q4 have higher emitter-base breakdown voltages of about 50V. Therefore, placing PNP transistors in series with NPN transistors provide protection against accidental shorting of supply to the input terminals.

Gain Stage:

The Second or the gain stage consists of transistors Q16 and Q17, with Q16 acting as an emitter – follower for achieving high input resistance. The transistor Q17 operates in common emitter configuration with its collector voltage applied as input to the output stage. Level shifting is done for this signal at this stage.

Internal compensation through Miller compensation technique is achieved using the feedback capacitor C1 connected between the output and input terminals of the gain stage.

Output stage:

The output stage is a class AB circuit consisting of complementary emitter follower transistor pair Q14 and Q20. Hence, they provide an effective loss output resistance and current gain. The output of the gain stage is connected at the base of Q22, which is connected as an emitter follower providing a very high input resistance, and it offers no appreciable loading effect on the gain stage. It is biased by transistor Q13A which also drives Q18 and Q19, that are used for establishing a quiescent bias current in the output transistors Q14 and Q20.

Explain the AC characteristics of Operational Amplifier.

Describe the AC performance characteristics of a operational amplifier. (8) (Nov/Dec 2014)

1.9 AC Characteristics:

For small signal sinusoidal (AC) application one has to know the ac characteristics such as frequency response and slew-rate.

1.9.1 Frequency Response:

The variation in operating frequency will cause variations in gain magnitude and its phase angle. The manner in which the gain of the op-amp responds to different frequencies is called the frequency response. Op-amp should have an infinite bandwidth BW =∞ (i.e.) if its open loop gain in 90dB with dc signal its gain should remain the same 90 dB through audio and onto high radio frequency. The op-amp gain decreases (roll-off) at higher frequency what reasons to decrease gain

after a certain frequency reached. There must be a capacitive component in the equivalent circuit of the op-amp. For an op-amp with only one break (corner) frequency all the capacitors

effects can be represented by a single capacitor C. Below fig is a modified variation of the low frequency model with capacitor C at the output.

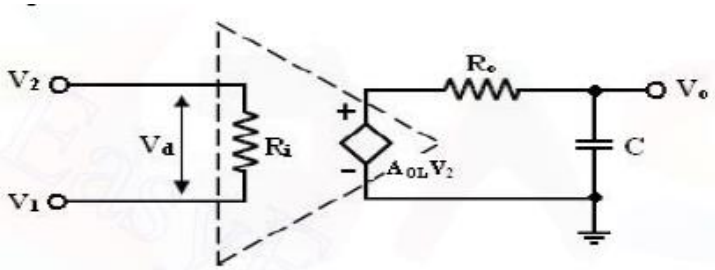


Fig 1.18 Equivalent circuit of practical circuit

There is one pole due to R0 C and one -20dB/decade. The open loop voltage gain of an op-amp with only one corner frequency is obtained from above fig. f1 is the corner frequency or the upper 3 dB frequency of the op-amp. The magnitude and phase angle of the open loop volt gain are f1 of frequency can be written as,

The magnitude and phase angle characteristics:

1. For frequency f<< f_1 the magnitude of the gain is 20 log A_{OL} in db.
2. At frequency f = f_1 the gain in 3 dB down from the dc value of A_{OL} in db. This frequency f_1 is called corner frequency.
3. For f>> f_1 the fain roll-off at the rate off -20dB/decade or -6dB/decade.

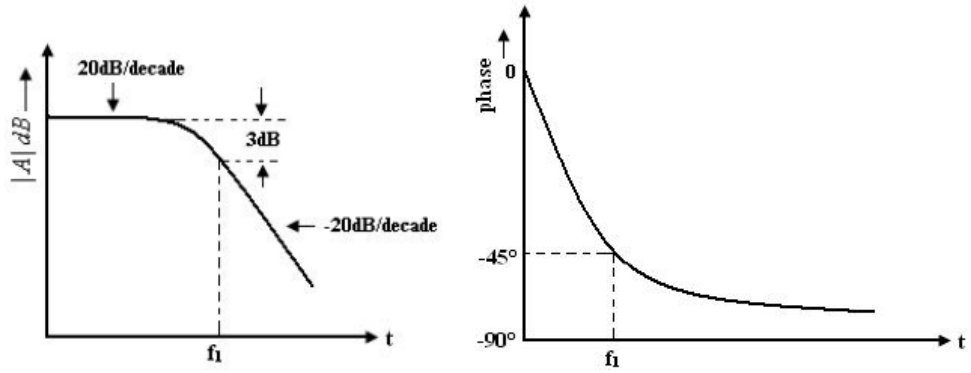


Fig 1.19 Frequency response of op amp

From the phase characteristics that the phase angle is zero at frequency f = 0. At the corner frequency f1 the phase angle is -45 (lagging and an infinite frequency the phase angle is -90 . It shows that a maximum of 90 phase change can occur in an op-amp with a single capacitor C. Zero frequency is taken as the decade below the corner frequency and infinite frequency is one decade above the corner frequency.

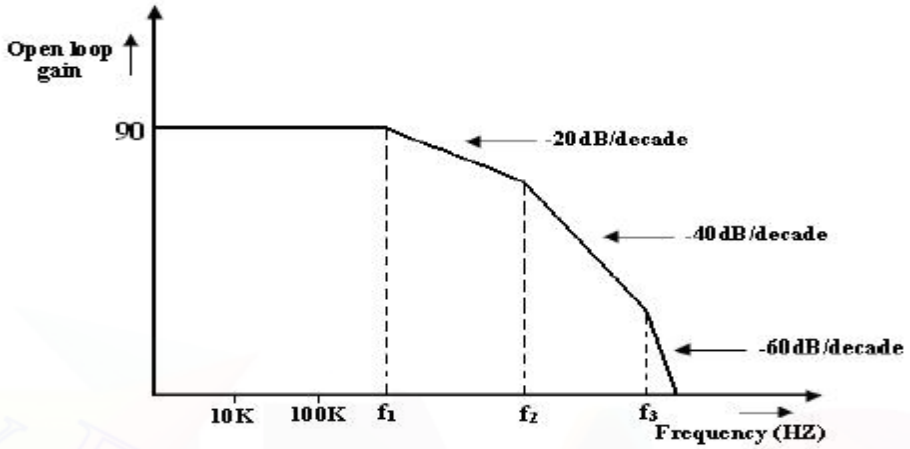


Fig. 1.20 Roll off rate of op amp gain

1.9.2 Circuit Stability:

A circuit or a group of circuit connected together as a system is said to be stable, if its o/p reaches a fixed value in a finite time. A system is said to be unstable, if its o/p increases with time instead of achieving a fixed value. In fact the o/p of an unstable sys keeps on increasing until the system break down. The unstable system is impractical and need be made stable. The criterion gn for stability is used when the system is to be tested practically. In theoretically, always used to test system for stability, ex: Bode plots. Bode plots are compared of magnitude Vs Frequency and phase angle Vs frequency. Any system whose stability is to be determined can represented by the block diagram.

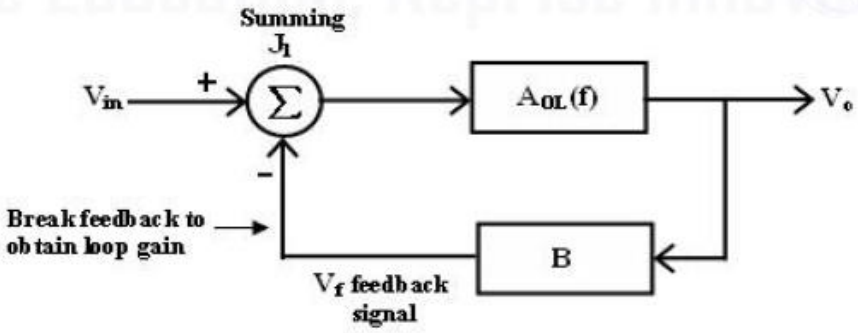


Fig. 1.21 Feedback loop system

Fig. 1.21 Feedback loop system

The block between the output and input is referred to as forward block and the block between the output signal and f/b signal is referred to as feedback block. The content of each block is referred as transfer frequency. From fig. we represented it by AOL (f) which is given by

$$A_{OL}(f) = V_0 / Vin \text{ if } V_f = 0 \text{ ----- (1)}$$

where $A_{OL}(f)$ = open loop volt gain.

The closed loop gain A_f is given by $A_F = V_0 / Vin$

$$= A_{OL} / (1+(A_{OL})(B) \quad \text{----(2)}$$

B = gain of feedback circuit.

B is a constant if the feedback circuit uses only resistive components.

Once the magnitude Vs frequency and phase angle Vs frequency plots are drawn, system stability may be determined as follows

1. Method 1:

Determine the phase angle when the magnitude of (AOL) (B) is 0dB (or) 1.

If phase angle is >-180 , the system is stable. However, the some systems the magnitude may never be 0, in that cases method 2, must be used.

2. Method 2:

Determine the phase angle when the magnitude of (AOL) (B) is 0dB (or) 1.

If phase angle is > - 180 , If the magnitude is –ve decibels then the system is stable. However, the some systems the phase angle of a system may reach -1800, under such conditions method 1 must be used to determine the system stability.

Explain the DC characteristics of Operational Amplifier.

Describe the DC performance characteristics of a operational amplifier. (8) (Nov/Dec 2014)

1.9.3 DC Characteristics of op-amp:

Current is taken from the source into the op-amp inputs respond differently to current and voltage due to mismatch in transistor.

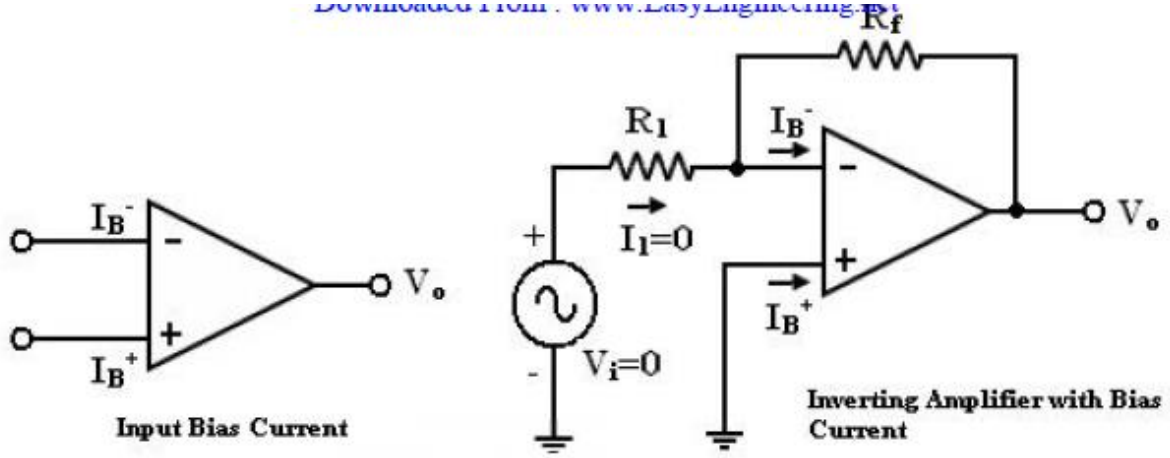
DC output voltages are,

- ✓ Input bias current
- ✓ Input offset current
- ✓ Input offset voltage
- ✓ Thermal drift

Input bias current:

The op-amp‘s input is differential amplifier, which may be made of BJT or FET.

In an ideal op-amp, we assumed that no current is drawn from the input terminals the base currents entering into the inverting and non-inverting terminals (IB- & IB+ respectively). Even though both the transistors are identical, IB- and IB+ are not exactly equal due to internal imbalance between the two inputs. Manufacturers specify the input bias current I_B



$$I_B = \frac{I_B^+ + I_B^-}{2}$$

If input voltage Vi = 0V. The output Voltage Vo should also be (Vo = 0) but for IB = 500Na We find that the output voltage is offset by Op-amp with a 1M feedback resistor Vo = 500nA X 1M = 500mV The output is driven to 500mV with zero input, because of the bias currents.

In application where the signal levels are measured in mV, this is totally unacceptable. This can be compensated by a compensation resistor Rcomp has been added between the non-inverting input terminal and ground as shown in the figure below.

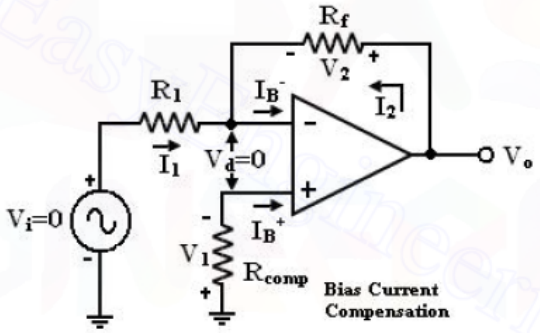


Fig. 1.22 Bias compensated circuit

Current I_B^+ flowing through the compensating resistor R_{comp}, then by KVL we get,

$-V_1+0+V_2-V_o = 0$ (or)

$V_o = V_2 - V_1$ --------- (1)

By selecting proper value of R_{comp}, V_2 can be cancelled with V_1 and the $V_o = 0$. The value of R_{comp} is derived as

$V_1 = I_B^+ R_{comp}$ (or)

$I_B^+ = V_1/R_{comp}$ ..... (2)

The node 'a' is at voltage $(-V_1)$. Because the voltage at the non-inverting input terminal is $(-V_1)$. So with $V_i = 0$ we get,

$I_1 = V_1/R_1$ ---------- (3)

$I_2 = V_2/R_f$ ---------- (4)

For compensation, V_o should equal to zero ($V_o = 0$, $V_i = 0$). i.e. from equation (3) $V_2 = V_1$. So that, $I_2 = V_1/R_f$ ——> (5)

KCL at node 'a' gives,

$$I_B^- = I_2 + I_1 = (V_1/R_f) + (V_1/R_1) = V_1(R_1+R_f)/R_1R_f \text{ ---------- (5)}$$

Assume $I_B^- = I_B^+$ and using equation (2) & (5) we get

$$V_1 (R_1+R_f)/R_1R_f = V_1/R_{comp}$$

$$R_{comp} = R_1 \parallel R_f \text{ ---------- (6)}$$

i.e. to compensate for bias current, the compensating resistor, R_{comp} should be equal to the parallel combination of resistor R_1 and R_f.

Input offset current:

- ✓ Bias current compensation will work if both bias currents I_B^+ and I_B^- are equal.
- ✓ Since the input transistor cannot be made identical. There will always be some small difference between I_B^+ and I_B^-. This difference is called the offset current

$$|I_{os}| = I_B^+ - I_B^- \text{ ---------- (7)}$$

Offset current I_{os} for BJT op-amp is 200nA and for FET op-amp is 10pA. Even with bias current compensation, offset current will produce an output voltage when $V_i = 0$.

$$V_1 = I_B^+ R_{comp} \text{ ---------- (11)}$$

$$\text{And } I_1 = V_1/R_1 \text{ ---------- (12)}$$

KCL at node a gives,

$$I_2 = (I_B^- - I_1) = I_B^- - (I_B^+ \frac{R_{comp}}{R_1})$$

Again $V_0 = I_2 R_f - V_1$

$$V_o = I_2 R_f - I_B^+ R_{comp}$$

$$V_o = 1M\Omega \text{ X } 200nA$$

$$V_o = 200mV \text{ with } V_i = 0$$

Equation (16) the offset current can be minimized by keeping feedback resistance small.

- ✓ Unfortunately to obtain high input impedance, R1 must be kept large.
- ✓ R1 large, the feedback resistor Rf must also be high. So as to obtain reasonable gain. The T-feedback network is a good solution. This will allow large feedback resistance, while keeping the resistance to ground low (in dotted line).
- ✓ The T-network provides a feedback signal as if the network were a single feedback resistor.

By T to Π conversion,

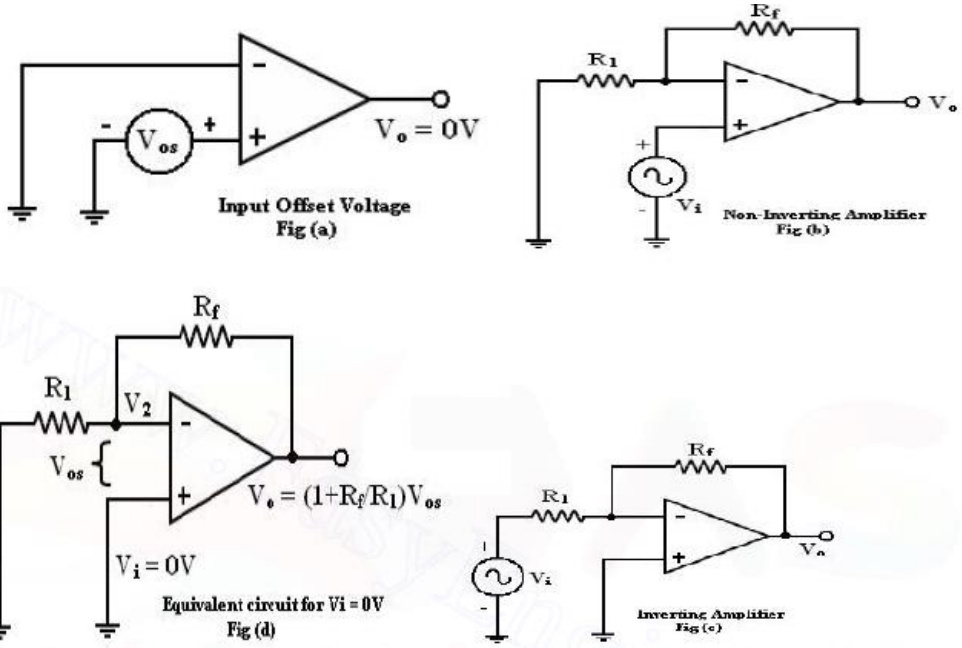
$$R_f = \frac{R_t^2 + 2R_tR_s}{R_s}$$

To design T- network first pick Rt<<Rf/2 and calculate

$$R_s = \frac{R_t^2}{R_f - 2R_t}$$

Input offset voltage:

In spite of the use of the above compensating techniques, it is found that the output voltage may still not be zero with zero input voltage [Vo ≠ 0 with Vi= 0]. This is due to unavoidable imbalances inside the op-amp and one may have to apply a small voltage at the input terminal to make output (Vo) = 0. This voltage is called input offset voltage Vos. This is the voltage required to be applied at the input for making output voltage to zero (Vo = 0).



Let us determine the V_{OS} on the output of inverting and non-inverting amplifier. If Vi = 0 (Fig (b) and (c)) become the same as in figure (d).

Total output offset voltage:

The total output offset voltage VOT could be either more or less than the offset voltage produced at the output due to input bias current (IB) or input offset voltage alone(Vos). This is because IB and Vos could be either positive or negative with respect to ground. Therefore the maximum offset voltage at the output of an inverting and non-inverting amplifier (figure b, c) without any compensation technique used is given by many op amps provide offset compensation pins to nullify the offset voltage. A 10K potentiometer is placed across offset null pins 1&5. The wipes connected to the negative supply at pin 4. The position of the wipes is adjusted to nullify the

offset voltage.

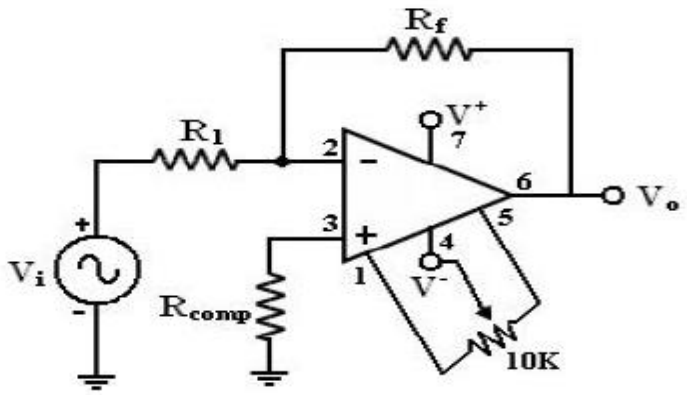


Fig.1.23 Compensation circuit for offset voltage

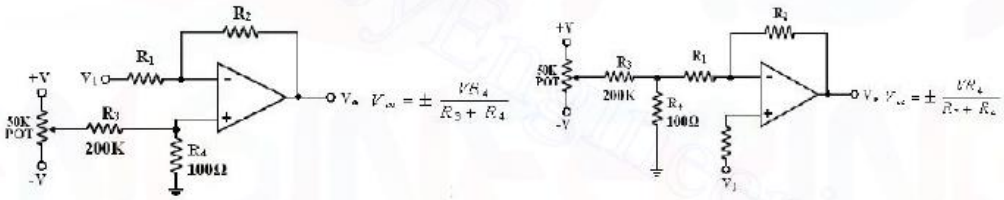
When the given (below) op-amps does not have these offset null pins, external balancing techniques are used.

$$V_{OT} = \left(1 + \frac{R_f}{R_1}\right) V_{OS} + R_f I_B$$

With Rcomp, the total output offset voltage

$$V_{OT} = \left(1 + \frac{R_f}{R_1}\right) V_{OS} + R_f I_{OS}$$

Balancing circuit: Inverting amplifier: **Non-inverting amplifier:**



Thermal drift:

Bias current, offset current, and offset voltage change with temperature. A circuit carefully nulled at 25ºC may not remain. So when the temperature rises to 35ºC. This is called drift. Offset current drift is expressed in nA/ºC. These indicate the change in offset for each degree Celsius change in temperature.

1.10 Slew Rate

Slew rate is the maximum rate of change of output voltage with respect to time. Specified in V/μs.

Reason for Slew rate:

There is usually a capacitor within 0, outside an op-amp oscillation. It is this capacitor which prevents the o/p voltage from fast changing input. The rate at which the volt across the capacitor increases is given by

$$dVc/dt = I/C \text{ --------(1)}$$

I -> Maximum amount furnished by the op-amp to capacitor C.

Op-amp should have the either a higher current or small compensating capacitors.

For 741 IC, the maximum internal capacitor charging current is limited to about 15μA. So the slew rate of 741 IC is

$$SR = dVc/dt\ |max = Imax/C$$

For a sine wave input, the effect of slew rate can be calculated as consider volt follower. The input is large amp, high frequency sine wave.

If Vs =Vm Sinwt then output V0 = Vm sinwt .

The rate of change of output is given by dV0/dt=Vm w coswt.

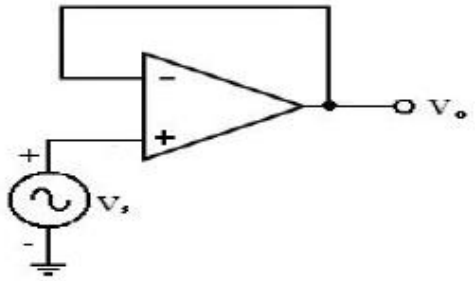


Fig. 1.22 Voltage Follower Circuit

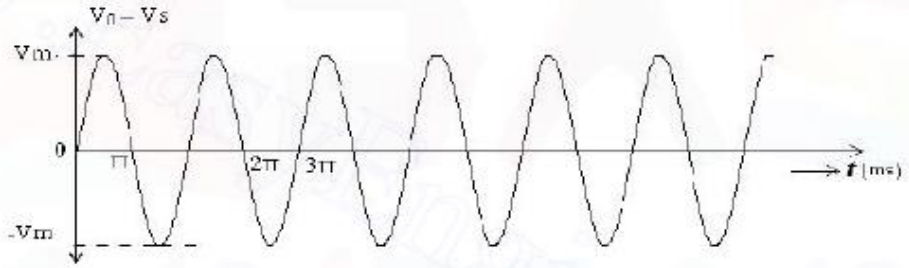


Fig. 1.23 Input and output waveforms of a voltage follower

The max rate of change of output across when coswt =1

(i.e) SR =dV_0/dt |max = wVm.

SR = 2πfVm V/s = 2πfVm v/ms.

Thus the maximum frequency fmax at which undistorted output volt of peak value Vm is given by fmax (Hz) = Slew rate/6.28 * Vm called the full power response. It is maximum frequency of a large amplitude sine wave with which op-amp can have without distortion.

Explain the Open loop configuration and Closed Loop Configuration of operational amplifier in detail.

1.11. Open – loop op-amp Configuration:

The term open-loop indicates that no feedback in any form is fed to the input from the output. When connected in open – loop the op-amp functions as a very high gain amplifier. There are three open – loop configurations of op-amp namely,

1. Differential amplifier
2. Inverting amplifier
3. Non-inverting amplifier

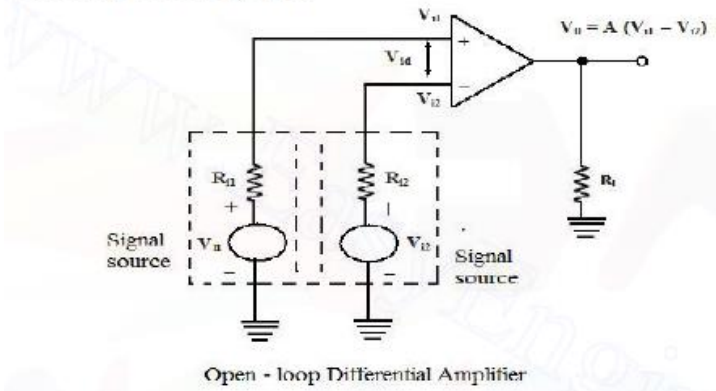
The above classification is made based on the number of inputs used and the terminal to which the input is applied. The op-amp amplifies both ac and dc input signals. Thus, the input signals can be either ac or dc voltage.

1.11.1 Loop Differential Amplifier:

In this configuration, the inputs are applied to both the inverting and the non-inverting input terminals of the op-amp and it amplifies the difference between the two input voltages. Figure shows the open-loop differential amplifier configuration. The input voltages are represented by Vi1 and Vi2. The source resistance Ri1 and Ri2 are negligibly small in comparison with the very high input resistance offered by the op-amp, and thus the voltage drop across these source resistances is assumed to be zero. The output voltage V0 is given by

$V0 = A (Vi1 – Vi2)$

where A is the large signal voltage gain. Thus the output voltage is equal to the voltage gain A times the difference between the two input voltages. This is the reason why this configuration is called a differential amplifier. In open – loop configurations, the large signal voltage gain A is also called open-loop gain A.

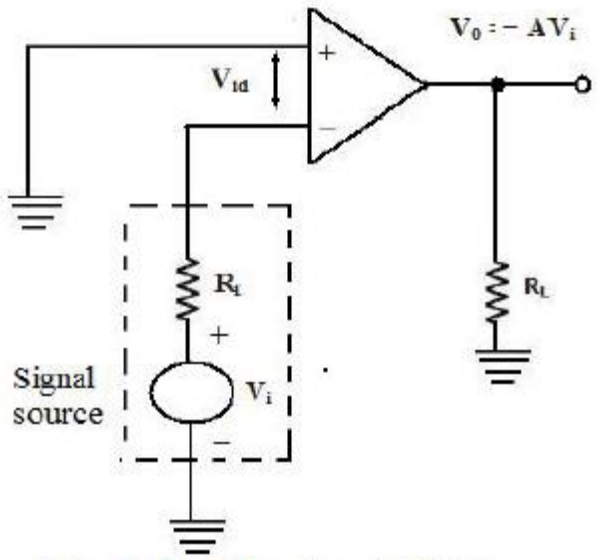


Open - loop Differential Amplifier

Inverting amplifier:

In this configuration the input signal is applied to the inverting input terminal of the op- amp and the non-inverting input terminal is connected to the ground. Figure shows the circuit of an open – loop inverting amplifier. The output voltage is 180 out of phase with respect to the input and hence, the output voltage V0 is given by,

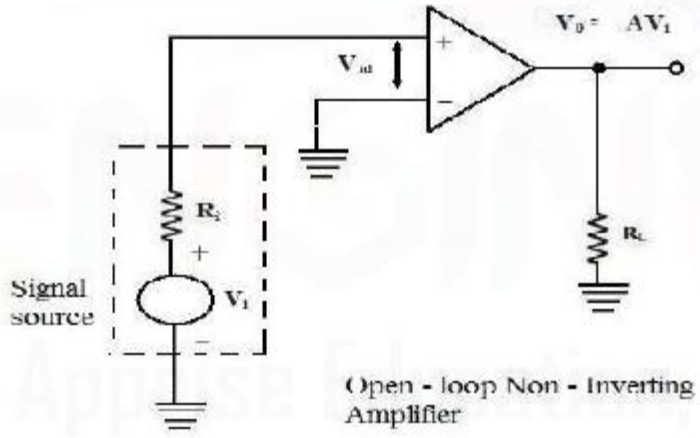
V0 = -AVi. Thus, in an inverting amplifier, the input signal is amplified by the open-loop gain A and in phase shifted by 180^0.



Open - loop Inverting Amplifier

Non-inverting Amplifier:

Figure shows the open – loop non- inverting amplifier. The input signal is applied to the non-inverting input terminal of the op-amp and the inverting input terminal is connected to the ground. The input signal is amplified by the open – loop gain A and the output is in-phase with input signal. V0 = AVi



Open - loop Non - Inverting Amplifier

In all the above open-loop configurations, only very small values of input voltages can be applied. Even for voltages levels slightly greater than zero, the output is driven into saturation, which is observed from the ideal transfer characteristics of op-amp shown in figure. Thus, when operated in the open-loop configuration, the output of the op-amp is either in negative or

positive saturation, or switches between positive and negative saturation levels. This prevents the use of open – loop
configuration of op-amps in linear applications.

Limitations of Open – loop Op – amp configuration:

Firstly, in the open – loop configurations, clipping of the output waveform can occur when the output voltage exceeds the saturation level of op-amp. This is due to the very high open – loop gain of the op-amp. This feature actually makes it possible to amplify very low frequency signal of the order of microvolt or even less, and the amplification can be achieved accurately without any distortion. However, signals of such magnitudes are susceptible to noise and the amplification for that application is almost impossible to obtain in the laboratory. Secondly, the open – loop gain of the op – amp is not a constant and it varies with changing temperature and variations in power supply. Also, the bandwidth of most of the open- loop op amps is negligibly small. This makes the open – loop configuration of op-amp unsuitable for ac
applications. The open – loop bandwidth of the widely used 741 IC is approximately 5Hz. But in almost all ac applications, the bandwidth requirement is much larger than this. For the reason stated, the open – loop op-amp is generally not used in linear applications. However, the open – loop op amp configurations find use in certain non – linear applications such as comparators, square wave generators and astable multivibrators.

1.11.2 Closed – loop op-amp configuration:

The op-amp can be effectively utilized in linear applications by providing a feedback from the output to the input, either directly or through another network. If the signal feedback is out- of phase by 1800 with respect to the input, then the feedback is referred to as negative feedback or degenerative feedback. Conversely, if the feedback signal is in phase with that at the input, then the feedback is referred to as positive feedback or regenerative feedback. An op – amp that uses feedback is called a closed – loop amplifier. The most commonly used closed – loop amplifier configurations are 1. Inverting amplifier (Voltage shunt amplifier) 2. Non- Inverting amplifier (Voltage – series Amplifier)

Inverting Amplifier:

The inverting amplifier is shown in figure and its alternate circuit arrangement is shown in figure, with the circuit redrawn in a different way to illustrate how the voltage shunt feedback is achieved. The input signal drives the inverting input of the op – amp through resistor R1.The op – amp has an open – loop gain of A, so that the output signal is much larger than the error voltage. Because of the phase inversion, the output signal is 1800 out – of – phase with the input signal. This means that the feedback signal opposes the input signal and the feedback is negative or degenerative.

Practical Inverting amplifier:

The practical inverting amplifier has finite value of input resistance and input current, its open voltage gain A0 is less than infinity and its output resistance R0 is not zero, as against the ideal inverting amplifier with finite input resistance, infinite open – loop voltage gain and zero output resistance respectively. Figure shows the low frequency equivalent circuit model of a practical inverting amplifier. This circuit can be simplified using the Thevenin‘s equivalent circuit shown in figure. The signal source Vi and the resistors R1 and Ri are replaced by their Thevenin‘s equivalent values. The closed – loop gain AV and the input impedance Rif are calculated as follows. The input impedance of the op- amp is normally much larger than the input resistance R1. Therefore, we can assume Veq ≈ Vi and Req ≈ R1 . From the figure

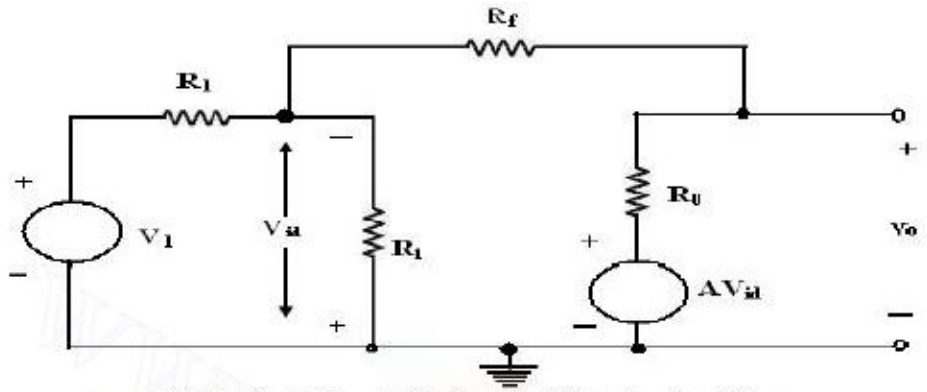
$$V_O = IR_O = AV_{id} \quad \text{and} \quad V_{id} = IR_f = AV_{id}$$

$$V_0 = IR_0 = AV_{id}$$

Substituting the value of I derived from above eqn. and obtaining the closed loop gain. It can be observed from above eqn. that when A>> 1, R0 is negligibly small and the product AR1 >> R0 +Rf , the closed loop gain is given by

$$Av = -\frac{R_f}{R_1}$$

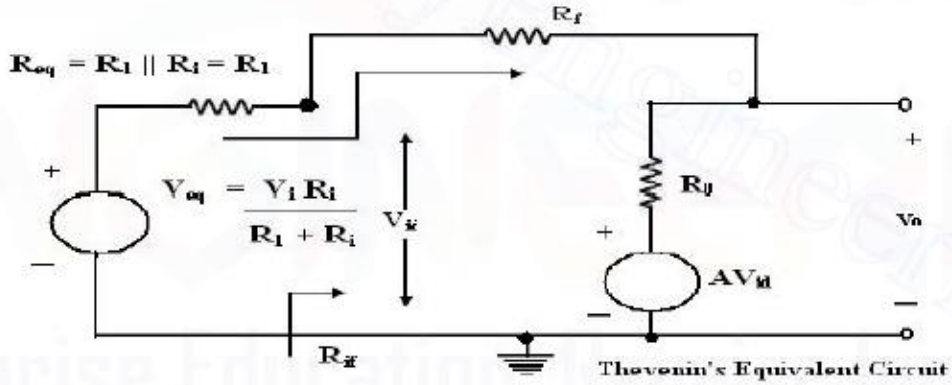
Which as the same form as given in above eqn for an ideal inverter.



Equivalent Circuit of a Practical Inerting Amplifier

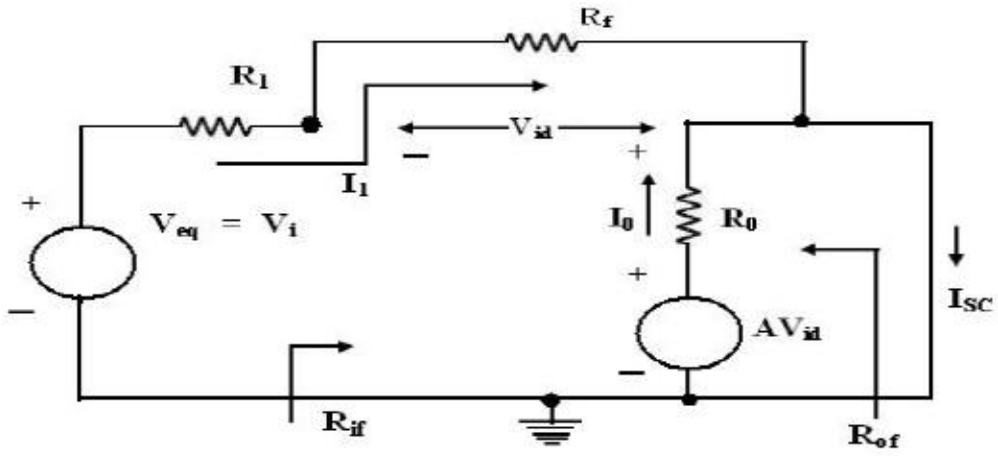
Input Resistance:

$R_{if} = V_{id}/ I_1 = (R_f+R_0)/(1+A)$



Thevenin's Equivalent Circuit

Output Resistance:



Equivalent circuit to determine Rof

Figure shows the equivalent circuit to determine Rof. The output impedance Rof without the load resistance factor RL is calculated from the open circuit output voltage Voc and the short circuit output current Isc.

$$R_{of} = \frac{\frac{R_0(R_1 + R_f)}{R_0 + R_1 + R_F}}{1 + \frac{R_1 A}{R_0 + R_1 + R_f}}$$

Non –Inverting Amplifier:

The non – inverting Amplifier with negative feedback is shown in figure. The input signal drives the non – inverting input of op-amp. The op-amp provides an internal gain A. The external resistors R1 and Rf form the feedback voltage divider circuit with an attenuation factor of β. Since the feedback voltage is at the inverting input, it opposes the input voltage at the non – inverting input terminals, and hence the feedback is negative or degenerative. The differential voltage Vid at the input of the op-amp is zero, because node A is at the same voltage as that of the non- inverting input terminal. As shown in figure, Rf and R1 form a potential divider. Therefore,

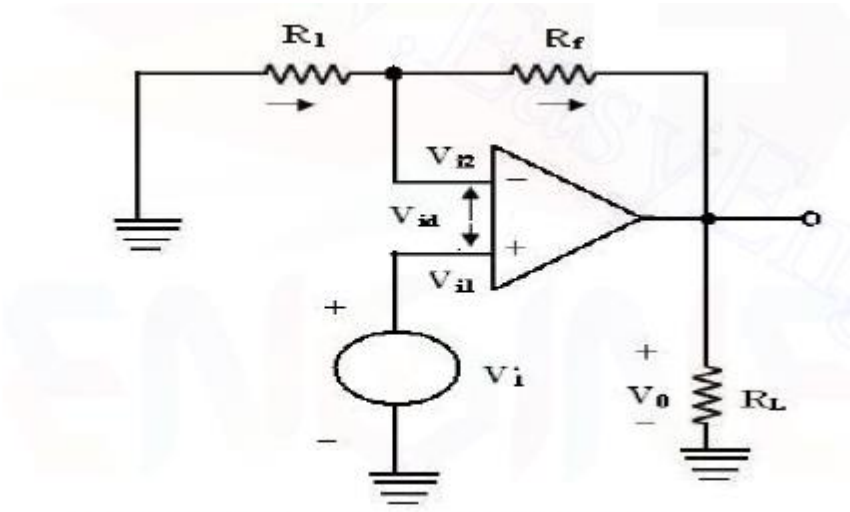


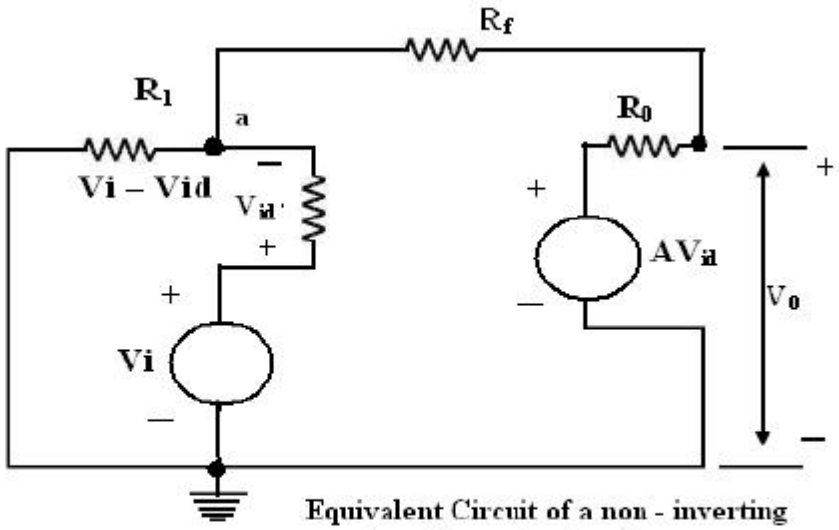
Fig. 1.24 Non –Inverting Amplifier:

Closed Loop Non – Inverting Amplifier

The input resistance of the op – amp is extremely large (approximately infinity,) since the op – amp draws negligible current from the input signal.

Practical Non –inverting amplifier:

The equivalent circuit of a non- inverting amplifier using the low frequency model is shown below in figure. Using Kirchhoff's current law at node a,



Equivalent Circuit of a non - inverting Amplifier using low frequency

$$Av = 1 + \frac{R_f}{R_1}$$

The difference volt is equal to the input volt minus the f/b volt. (or) The feedback volt always opposes the input volt (or out of phase by 1800 with respect to the input voltage) hence the feedback is said to be negative.

It will be performed by computing

1. Closed loop volt gain
2. Input and output resistance
3. Bandwidth

1. Closed loop volt gain:

The closed loop volt gain is AF = V0 /Vin

V0 = Avid =A(V1 –V2)

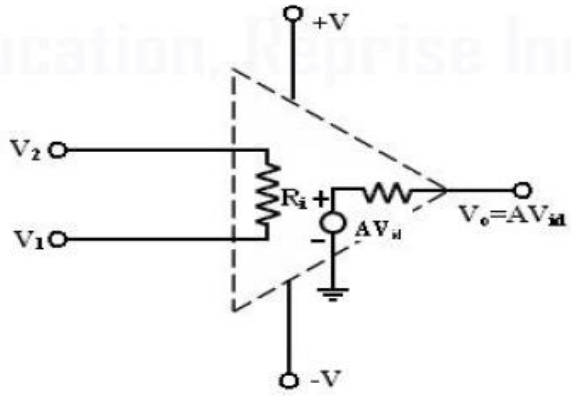


Fig.1.25 equivalent circuit of practical op amp

A = large signal voltage gain.

From the above eqn.

V0 = A(V1 – V2)

Refer fig, we see that, $V_1 = Vin$

$V_2 = V_f = \frac{R_1}{R_1+R_f} V_0$ Since Ri >> R1

$V_0 = AVin - \frac{R_1 V_0}{R_1 + R_f}$

$V_0 + \frac{R_1}{R_1+R_f} V_0 = AVin$

PART-A

1. What is an integrated circuit? [APR 10]

The Integrated Circuit or IC is a miniature, low cost electronic circuit

consisting of active and passive components that are irreparably joined together on a single crystal chip of silicon.

2. State the limitations of discrete circuits. [APR 13]

i. Large size.

ii. ICs operate at high voltages

iii. High cost

iv. High power consumption.

3. State the advantages of integrated circuits over discrete components. [DEC 13, APR 14, DEC 14]

i. Practically size of an IC is thousands of times smaller than the discrete circuits.

ii. ICs operate at low voltages

iii. Low cost

iv. Low power consumption.

4. What is current mirror? [APR 10]

OR

Define current mirror with magnification. [DEC 11]

The circuit in which the output current is forced to equal to the input current is called current mirror circuit. In a current mirror circuit, the output current is the mirror image of input current.

5. Define slew rate. [MAY16,May15]

The slew rate is defined as the maximum rate of change of output voltage caused by a step input voltage. An ideal slew rate is infinite which means that op-amp‘s output voltage should change instantaneously in response to input step voltage.

$$SR = \left.\frac{dv_c}{dt}\right|_{max} = \frac{I_{max}}{C}$$

6. Why are active loads preferred than passive loads in the input stage of an operational amplifier? [DEC 10, Dec 16]

The active loads are realized using current source in place of the passive load in the collector arm of differential amplifier to make it possible to achieve high

voltage gain without requiring large power supply voltage.

7. Compare the performance of inverting and non-inverting operational amplifier configurations. [DEC 10]

Compared to the inverting amplifier, the input resistance of the non-inverting amplifier is extremely large (=∞) as the op-amp draws negligible current from the signal source.

8. Why is frequency compensation required in operational amplifier? [DEC 10]

Frequency compensation is required, when we need

1. Large bandwidth
2. Low closed loop gain

9. Define CMRR of an OP-AMP. [APR 11, DEC 10, APR 13, May15]

The ratio of differential gain and the common mode gain is termed as Common Mode Rejection Ratio.

$$CMRR = \frac{A_d}{A_c}$$

A_d = differential gain

A_c = common mode gain

10. What are the two requirements to be met for a good current source? [APR 12]

i. Output current I_o should not be dependent upon β

ii. Output resistance should be very high

11. List the various methods of realizing high i/p resistance in a differential amplifier. [APR 12]

i. Darlington pair

ii. Fabricate a FET differential pair as input stage

12. Define offset voltage of an operational amplifier. [DEC 13]

A small voltage applied to the input terminals to make the output voltage as zero when the two input terminals are grounded is called input offset voltage.

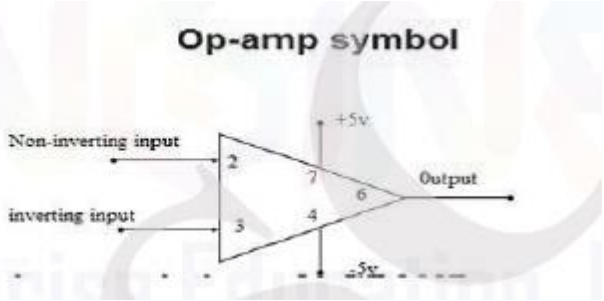
13. What is meant by Monolithic IC? [DEC 14]

A monolithic circuit means a circuit fabricated from a single stone or a single crystal. Monolithic is from a Greek word _Monos‘ meaning _Single‘&_lithos‘ meaning _stone‘. Monolithic ICs are made in a single piece of single crystal silicon.

14. List the characteristics of ideal op-amp and draw its equivalent circuit?

[MAY 15, Nov 16, MAY 2016]

Ideal op-amp:



Characteristics of ideal op-amp:

Open loop voltage gain $A_{OL} = \infty$

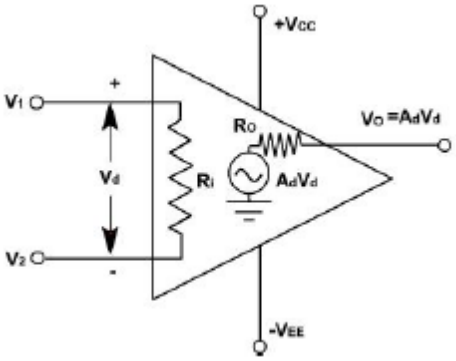
Input impedance $R_i = \infty$

Output impedance $R_o = 0$

Bandwidth BW = ∞

Zero offset $V_o = 0$ When $V_1 = V_2 = 0$

Equivalent circuit:



15. Define the following parameters as applied to an op-amp: (Dec15)

i) Input bias current

Input bias current IB is the average of the currents that flow into the inverting and non-inverting input erminals of the op-amp.

i.e. IB = (IB1+IB2)/2

ii) Input offset current

The algebraic difference between the current into the inverting and non-inverting terminals is referred to as input offset current Iio. Mathematically it is represented as

Iio = |IB - IB |

Where

I B+is the current into the non-inverting input terminals. IB- is the current into the inverting input terminals.

iii) Input offset voltage

This is the voltage required to be amplified at the input for making output voltage to zero volts.

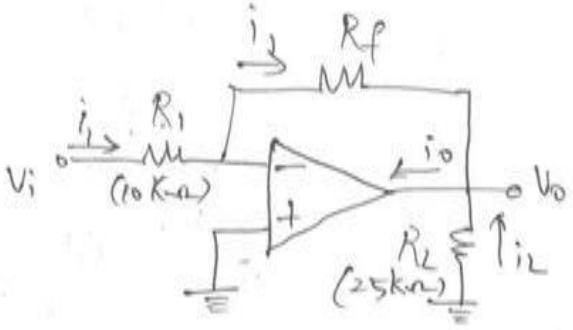
iv) P.S.R.R

Power Supply Rejection Ratio (PSRR) is the ability of an amplifier to maintain its output voltage as its

DC power-supply voltage is varied. PSRR = (change in Vcc)/(change in Vout)

Part-C.

1) In figure, $R_1 = 10k\Omega$, $R_f = 100k\Omega$, $v_i = 1V$. A load of $25k\Omega$ is connected to the output terminal. Calculate (i) i_1 (ii) V_o (iii) i_L and (iv) total current i into the output pin.



Given:

$R_1 = 10k\Omega$, $R_f = 100k\Omega$, $v_i = 1V$, $R_L = 25k\Omega$

To find: i_1, V_o, i_L, i_o

(i) $i_1 = \frac{V_i}{R_1} = \frac{1V}{10K\Omega} = \frac{1V}{10\times10^3\Omega} = 0.1mA$

$\boxed{i_1 = 0.1mA}$

(ii) $V_o = -\frac{R_f}{R_1} v_i = -\frac{100K\Omega}{10k\Omega} \times 1V = -10V$

$\boxed{V_o = -10V}$

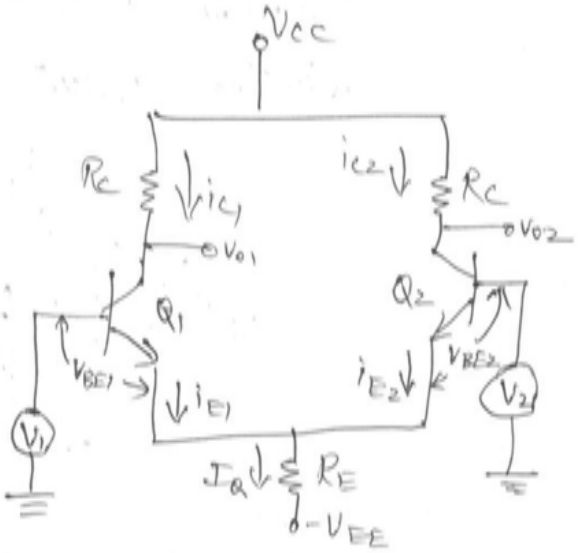
(iii) $i_L = \frac{V_o}{R_L} = \frac{10V}{25k\Omega} = 0.4mA$

$\boxed{i_L = 0.4mA}$

(iv) $i_o = i_1 + i_L = 0.1mA + 0.4mA = 0.5mA$.

$\boxed{i_o = 0.5mA}$ flowing into the output pin.

(I) (b) Differential amplifier shown in Fig, uses a transistor with $\beta = 200$ and is biased at $I_{CQ} = 100\mu A$. Determine the value of R_C and R_E if $|A_{DM}| = 500$ and CMRR = 80dB.



Given:

$\beta = 200$, $I_{CQ} = 100\mu A$

$|A_{DM}| = 500$, CMRR = 80dB

To find:

R_C, R_E

Soln:

$$g_m = \frac{I_{CQ}}{V_T} = \frac{100 \times 10^{-6}}{25 \times 10^{-3}} \mho$$

$$= 4m\mho \quad [\text{for } V_T = 25mV]$$

$$A_{DM} = -g_m R_C$$

$$R_C = \frac{-A_{DM}}{g_m} = \frac{500}{4m\mho} = 125 K\Omega$$

$$\boxed{R_C = 125 K\Omega}$$

$$CMRR = 80dB$$

$$= \log^{-1}\left(\frac{80}{20}\right) = 10^4$$

$$CMRR = 1+2g_m R_E = 1+2\times4\times R_E$$

$$\boxed{R_E = 1.25 M\Omega}$$

2)(a) In the basic differential amplifier, given $R_C = 2\,K\Omega$, $R_E = 4.3K\Omega$, $V_{CC} = |V_{EE}| = 5V$; $\beta_0 = 200$, $V_{BE} = 0.7V$.

Determine

(i) For $V_1 = V_2 = 0$; find the values of quiescent currents and voltages I_{BQ}, I_{CQ}, V_{O1}, V_{O2}, V_{CEQ}

(ii) A_{DM}, A_{CM} and CMRR

Soln:

(i) Apply KVL for the base emitter loop,

$$V_{BE} + 2(1+\beta)I_{BQ}R_E - V_{EE} = 0$$

$$I_{BQ} = \frac{V_{EE} - V_{BE}}{2(1+\beta)R_E} = \frac{5V - 0.7V}{2(1+200)4.3K\Omega} = \boxed{2.4\mu A = I_{BQ}}$$

$$I_{CQ} = \beta I_{BQ} = 200 \times 2.4\mu A = \boxed{0.48mA = I_{CQ}}$$

$$V_{O1} = V_{O2} = V_{CC} - I_{CQ}R_C$$

$$= 5V - 2K\Omega \times 0.48mA = 4.04V$$

$$\boxed{V_{O1} = V_{O2} = 4.04V}$$, due to symmetry

$$V_{CEQ} = V_C - V_E$$

$$= V_{O1} - (-V_{BE}) = V_{O1} + V_{BE}$$

$$= 4.04V + 0.7V = \boxed{4.74V = V_{CEQ}}$$

(ii) $$g_m = \frac{I_{CQ}}{V_T} = \frac{0.48mA}{25mV} = 0.0192\,\mho = 19.2\,m\mho$$

$$r_\pi = \frac{\beta_0}{g_m} = \frac{200}{19.2m\mho} = 10.4\,K\Omega$$

$$A_{DM} = -g_m R_C = -19.2\,m\mho \times 2K\Omega = \boxed{-38.4 = A_{DM}}$$

$$A_{CM} = \frac{-\beta_0 R_C}{r_\pi + 2(1+\beta_0)R_E} = \frac{-200 \times 2K\Omega}{10.4K\Omega + 2(1+200)4.3K\Omega} = \boxed{A_{CM} = -0.23}$$

$$CMRR = \frac{A_{DM}}{A_{CM}} = \frac{-38.4}{-0.23} = 166.9 = \boxed{44.44dB = CMRR}$$

2(b) In the basic differential amplifier, the following inputs are applied,

$V_1 = 15 \sin 2\pi(60)t + 5 \sin 2\pi(1000)t$ mV

$V_2 = 15 \sin 2\pi(60)t - 5 \sin 2\pi(1000)t$ mV

Here, the signal at 60Hz is the interference signal and the signal to be processed is at 1KHz. Determine the output voltages V_{o1} and V_{o2}.

Given: V_1, V_2

To find: V_{o1}, V_{o2}

Soln: From pb ①;

$g_m = 4mV$, $R_C = 125k\Omega$, $R_E = 1.25k\Omega$.

and $r_\pi = \frac{\beta_0}{g_m} = \frac{200}{4mV} = 50k\Omega$; $A_{DM} = -500$

$$A_{CM} = \frac{-\beta_0 R_C}{2(1+\beta_0)R_E + r_\pi} = \frac{-200 \times 125k\Omega}{2(1+200)1250k\Omega + 50k\Omega}$$

$$= -0.05$$

$$V_{DM} = \frac{V_1 - V_2}{2} = 5 \sin 2\pi(1000)t$$

$$V_{CM} = \frac{V_1 + V_2}{2} = 15 \sin 2\pi(60)t$$

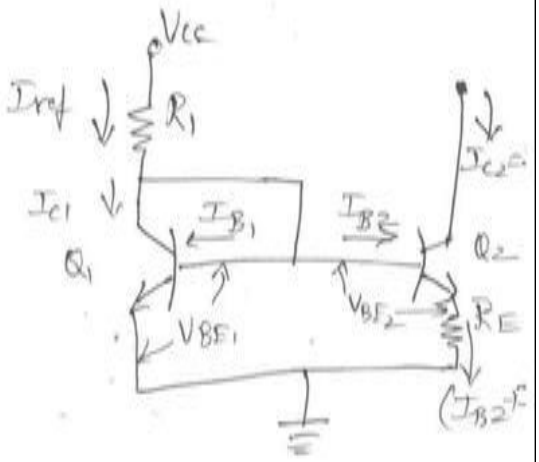
$$V_{o1} = -500[5 \sin(2\pi 1000t)] - 0.05[15 \sin 2\pi 60t]$$

$$\boxed{V_{o1} = -2500 \sin 2\pi 1000t - 0.75 \sin 2\pi 60t}$$

$$V_{o2} = -(-500)[5 \sin 2\pi 1000t] - 0.05[15 \sin 2\pi 60t]$$

$$= 2500 \sin 2\pi 1000t - 0.75 \sin 2\pi 60t$$

3) a) Design a Widlar current source for generating a constant current $I_o = 10\mu A$. Assume $V_{cc} = 10V$, $V_{BE} = 0.7V$, $\beta = 125$. Use $V_T = 25mV$.



Given:

$I_o = 10\mu A$,

$V_{cc} = 10V$

$V_{BE} = 0.7V$

$\beta = 125$

$V_T = 25mV$

To find:

R_1, R_E

Soln:

$$R_1 = \frac{V_{cc} - V_{BE}}{I_{ref}} = \frac{10V - 0.7V}{1mA} = 9.3K\Omega$$

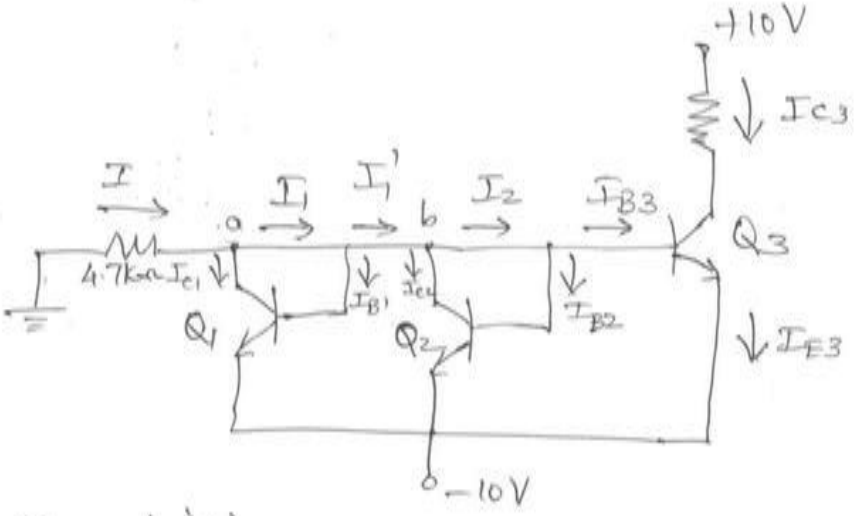
$\boxed{R_1 = 9.3K\Omega}$ (Take $I_{ref} = 1mA$)

$$R_E = \frac{V_T}{\left(1+\frac{1}{\beta}\right)I_{C2}} \ln\left(\frac{I_{C1}}{I_{C2}}\right)$$

$$= \frac{0.025V}{\left(1+\frac{1}{125}\right)10\times10^{-6}} \cdot \ln\left(\frac{1\times10^{-3}}{10\times10^{-6}}\right)$$

$\boxed{R_E = 11.5K\Omega}$

3b) Figure shows a modified current mirror circuit. Determine the emitter current in transistor Q_3 if $\beta = 100$ and $V_{BE} = 0.75V$



At node 'a';

$$I = I_1 + I_{C1}$$
$$= I_{C1} + I_{B1} + I_1'$$
$$= I_{C1}\left(1 + \frac{1}{\beta}\right) + I_1' \simeq I_{C1} + I_1' \quad (\text{as } \beta >> 1).$$

At node 'b';

$$I_1' = I_{C2} + I_2$$
$$= I_{C2} + I_{B2} + I_{B3}$$
$$= I_{C2}\left(1 + \frac{1}{\beta}\right) + I_{B3} \simeq I_{C2} + I_{B3}$$

Sub value of I_1';

$$I = I_{C1} + I_{C2} + I_{B3}$$
$$= 2I_C + I_{B3} \quad [\text{as } I_{C1} = I_{C2}]$$
$$= I_C\left[2 + \frac{1}{\beta}\right] \simeq 2I_C.$$

$$I = \frac{10 - 0.75}{4.7k\Omega} = \frac{9.25}{4.7k\Omega} = 1.97\,mA$$

$$I_{E3} \simeq I_{C3} = I_C = \frac{I}{2} = \boxed{0.98mA = I_{E3}}$$

JFET OPERATIONAL AMPLIFIERS

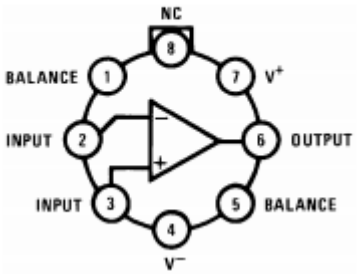
JFET operational amplifiers are very popular because of its advantages over BJT or MOSFET operational amplifiers. In this type of op-amps, Junction field effect transistors are used at the input terminals. This is to distinguish from BJT or MOSFET inputs. JFET inputs provide lower input currents than BJT's, and are not as sensitive to damage by electrostatic discharge (ESD) as are MOSFET's. The general JFET input operational amplifier series by Texas Instruments was named as LF x5x. The series includes LF 155, LF 156, LF 256, LF 257, LF 355, LF 356 and LF 357 with two Xs taking different digits. These devices are excellent choice for low noise applications with either high or low source impedance.

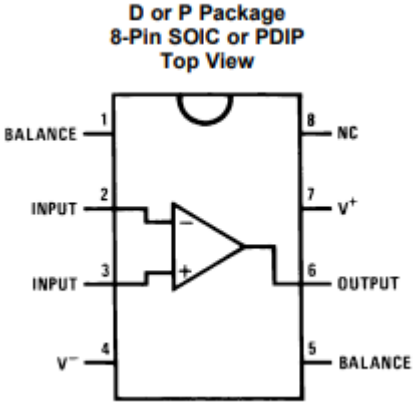
LF 155

The LFx5x devices are the first monolithic JFET input monolithic operational amplifiers to incorporate well-matched high-voltage JFETs on the same chip with standard bipolar transistors. These amplifiers feature low input bias and offset currents/low offset voltage and offset voltage drift, coupled with offset adjust, which does not degrade drift or common-mode rejection. The devices are also designed for high slew rate, wide bandwidth, extremely fast settling time and low voltage and current noise.

PIN DIAGRAM

The two available IC packages were shown here for LF x5x series. Both contains 8 - pins and the table shows the pin description of each pin.

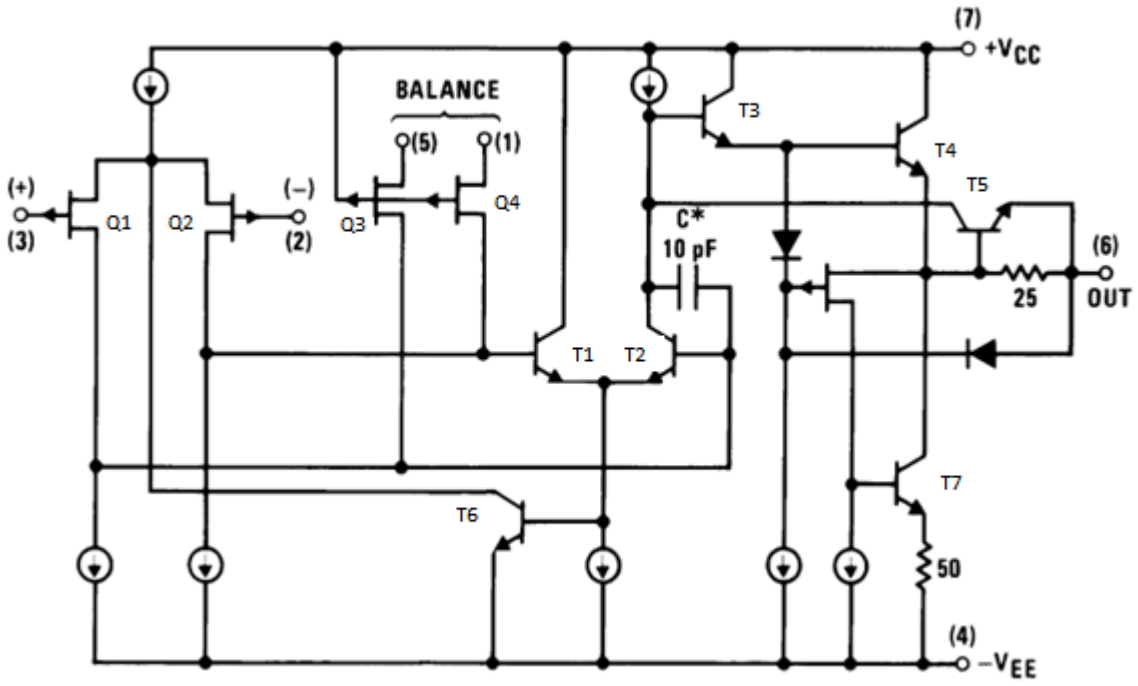




Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
BALANCE	1, 5	I	Balance for input offset voltage
+INPUT	3	I	Noninverting input
–INPUT	2	I	Inverting input
NC	8	—	No connection
OUTPUT	6	O	Output
V+	7	—	Positive power supply
V–	4	—	Negative power supply

SIMPLIFIED INTERNAL CIRCUIT



These JFETs have large reverse breakdown voltages from gate to source and drain eliminating the need for clamps across the inputs. Therefore large differential input voltages can easily be accommodated without a large increase in input current. The maximum differential input voltage between pin 2 and 3 is independent of the supply voltages $+V_{CC}$ and $-V_{EE}$. However, neither of the input voltages should be allowed to exceed the negative supply as this will cause large currents to flow which can result in destruction of device.

Exceeding the negative common-mode limit on either input will force the output to a high state, potentially causing a reversal of phase to the output. Exceeding the negative common-mode limit on both inputs will force the amplifier output to a high state. In neither case does a latch occur, since raising the input back within the common-mode range again puts the input stage and thus the amplifier in a normal operating mode.

Exceeding the positive common-mode limit on a single input will not change the phase of the output however, if both inputs exceed the limit, the output of the amplifier will be forced to a high state. These amplifiers will operate with the common-mode input voltage equal to the positive supply. In fact, the common-mode voltage can exceed the positive supply by approximately 100 mV independent of supply voltage and over the full operating temperature range. The positive supply can therefore be used as a reference on an input as, for example, in a supply current monitor and/or limiter. Precautions should be taken to ensure that the power supply for the integrated circuit never becomes reversed in polarity or that the device is not inadvertently installed backwards in a socket as an unlimited current surge through the resulting forward diode within the IC could cause fusing of the internal conductors and result in destruction.

All of the bias currents in these amplifiers are set by FET current sources formed by Q1 and Q2. The drain currents for the amplifiers are independent of supply voltage. Q3 and Q4 are another pair of JFET used along with the balance input pins 1 and 5 to nullify the positive or negative offset at output of op-amp. T1 and T2 forms the intermediate differential amplifier pair and transistor T6 limits the excess current flow from coupled emitters of T1 and T2. Transistors T3 and T4 forms the darlington pair responsible for high current gain and good output voltage drive. The value of capacitor C varies according to the different IC series number.

FEATURES

- Common Features
  - Low Input Bias Current: 30 pA
  - Low Input Offset Current: 3 pA
  - High Input Impedance: 10^{12} Ω
  - Low Input Noise Current: 0.01 pA/$\sqrt{Hz}$
  - High Common-Mode Rejection Ratio: 100 dB
  - Large DC Voltage Gain: 106 dB

- Uncommon Features
  - Extremely Fast Settling Time to 0.01%:
    - 4 µs for the LFx55 devices
    - 1.5 µs for the LFx56
    - 1.5 µs for the LFx57 (A_V = 5)
  - Fast Slew Rate:
    - 5 V/µs for the LFx55
    - 12 V/µs for the LFx56
    - 50 V/µs for the LFx57 (A_V = 5)
  - Wide Gain Bandwidth:
    - 2.5 MHz for the LFx55 devices
    - 5 MHz for the LFx56
    - 20 MHz for the LFx57 (A_V = 5)
  - Low Input Noise Voltage:
    - 20 nV/$\sqrt{Hz}$ for the LFx55
    - 12 nV/$\sqrt{Hz}$ for the LFx56
    - 12 nV/$\sqrt{Hz}$ for the LFx57 (A_V = 5)

ADVANTAGES

- Replace Expensive Hybrid and Module FET Op Amps
- Rugged JFETs Allow Blow-Out Free Handling Compared With MOSFET Input Devices
- Excellent for Low Noise Applications Using Either High or Low Source Impedance-
- Offset Adjust Does Not Degrade Drift or Common-Mode Rejection as in Most Monolithic Amplifiers
- New Output Stage Allows Use of Large Capacitive Loads (5,000 pF) Without Stability Problems
- Internal Compensation and Large Differential Input Voltage Capability

APPLICATIONS

- Precision High-Speed Integrators
- Fast D/A and A/D Converters
- High Impedance Buffers
- Wideband, Low Noise, Low Drift Amplifiers
- Logarithmic Amplifiers
- Photocell Amplifiers
- Sample and Hold Circuits

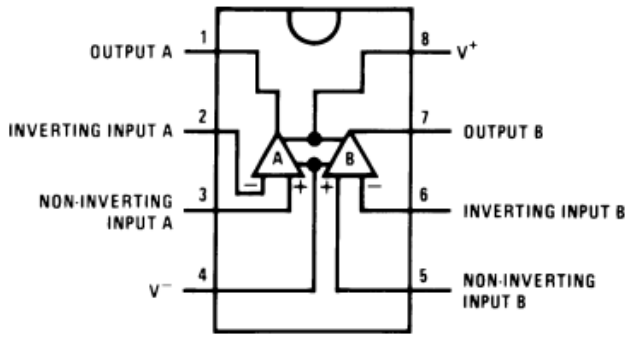
TL 082

TL 082 is a wide band dual JFET input operational amplifier manufactured by Texas Instruments in PDIP (plastic DIP) and SOIC (Small Outline Integrated Circuits) packages and by ST Microelectronics in SO8 and TSSOP8 (Thi Small Outline package) packages.

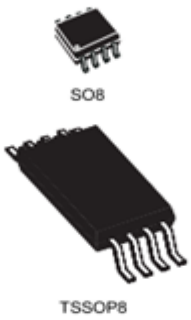
These devices are low cost, high speed, dual JFET input operational amplifiers with an internally trimmed input offset voltage (BI-FET II technology). They require low supply current yet maintain a large gain bandwidth product and fast slew rate. In addition, well matched high voltage JFET input devices provide very low input bias and offset currents. The applications are high speed integrators, fast D/A converters, sample and hold circuits and many other circuits requiring low input offset voltage, low input bias current, high input impedance, high slew rate and wide bandwidth. The devices also exhibit low noise and offset voltage drift. The pin diagram below shows the dual op-amp configured on either side of the IC and each op-amp is named a A and B inside the IC. The next figure shows the typical connection of one op-amp (A or B) inside the IC. These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

PIN DIAGRAM

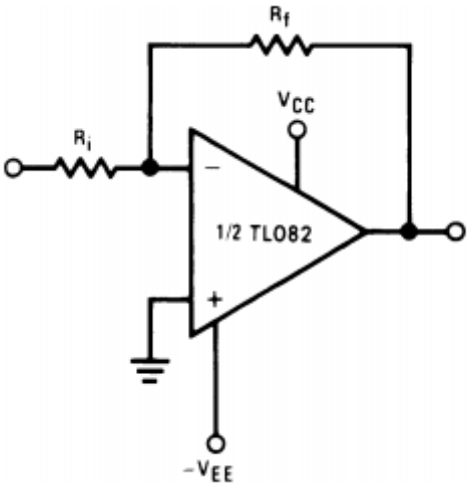
PDIP/SOIC Package (Top View)



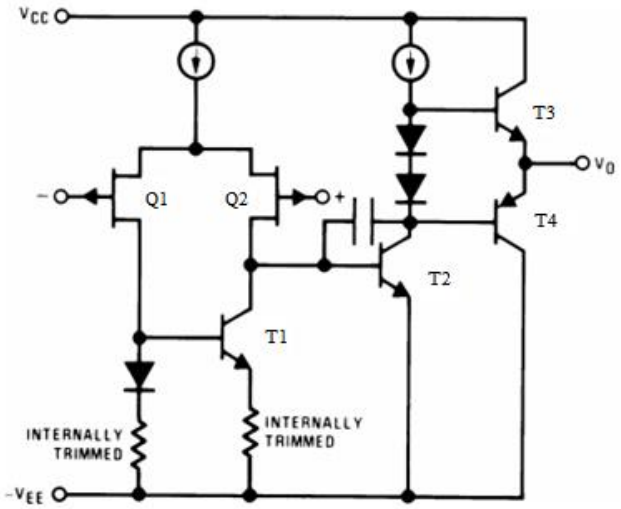
SO8 and TSSOP8



TYPICAL CONNECTION



INTERNAL CIRCUIT



This device is an op amp with an internally trimmed input offset voltage and JFET input devices (BI-FET II). These JFETs have large reverse breakdown voltages from gate to source and drain eliminating the need for clamps across the inputs. It contains a JFET pair formed by Q1 and Q2, acting as single differential amplifier stage and a cascaded BJT amplifier section formed by tansistors T1 and T2. Transistor T3 and T4 in the output stage acts as a complimentary push-pull amplifier. The voltage difference applied across the JFET input terminals, controls the voltage source by allowing a limited current from the source to drain of the JFETs from $+V_{CC}$ to $-V_{EE}$.

Large differential input voltages can easily be accommodated without a large increase in input current. The maximum differential input voltage is independent of the supply voltages.

However, neither of the input voltages should be allowed to exceed the negative supply as this will cause large currents to flow which can result in a destroyed unit. Exceeding the negative common-mode limit on either input will cause a reversal of the phase to the output and force the amplifier output to the corresponding high or low state. Exceeding the negative common-mode limit on both inputs will force the amplifier output to a high state. In neither case does a latch occur since raising the input back within the common-mode range again puts the input stage and thus the amplifier in a normal operating mode.

Exceeding the positive common-mode limit on a single input will not change the phase of the output; however, if both inputs exceed the limit, the output of the amplifier will be forced to a high state. The amplifiers will operate with a common-mode input voltage equal to the positive supply; however, the gain bandwidth and slew rate may be decreased in this condition. When the negative common-mode voltage swings to within 3V of the negative supply, an increase in input offset voltage may occur. Each amplifier is individually biased by a zener reference which allows normal circuit operation on ±6V power supplies. Supply voltages less than these may result in lower gain bandwidth and slew rate. The amplifiers will drive a 2 kΩ load resistance to ±10V over the full temperature range of 0°C to +70°C.

If the amplifier is forced to drive heavier load currents, however, an increase in input offset voltage may occur on the negative voltage swing and finally reach an active current limit on both positive and negative swings. Precautions should be taken to ensure that the power supply for the integrated circuit never becomes reversed in polarity or that the unit is not inadvertently installed backwards in a socket as an unlimited current surge through the resulting forward diode within the IC could cause fusing of the internal conductors and result in a destroyed unit. Because these amplifiers are JFET rather than MOSFET input op amps they do not require special handling.

As with most amplifiers, care should be taken with lead dress, component placement and supply decoupling in order to ensure stability. For example, resistors from the output to an input should be placed with the body close to the input to minimize “pick-up” and maximize the frequency of the feedback pole by minimizing the capacitance from the input to ground. A feedback pole is created when the feedback around any amplifier is resistive. The parallel resistance and capacitance from the input of the device (usually the inverting input) to AC ground set the frequency of the pole.

FEATURES

- **Internally Trimmed Offset Voltage: 15 mV**
- **Low Input Bias Current: 50 pA**
- **Low Input Noise Voltage: 16nV/√Hz**
- **Low Input Noise Current: 0.01 pA/√Hz**
- **Wide Gain Bandwidth: 4 MHz**
- **High Slew Rate: 13 V/μs**
- **Low Supply Current: 3.6 mA**
- **High Input Impedance: $10^{12}\Omega$**
- **Low Total Harmonic Distortion: ≤0.02%**
- **Fast Settling Time to 0.01%: 2 μs**

APPLICATIONS

These amplifiers may be used in applications such as high-speed integrators, fast D/A converters, sample and hold circuits and many other circuits requiring low input offset voltage, low input offset voltage, low input bias current, high input impedance, high slew rate and wide bandwidth. The devices also exhibit low noise and offset voltage drift.